PIC18-Q20 Family Product Brief

Introduction

The PIC18-Q20 microcontroller family is one of the smallest PIC18 product families available in 14/20-pin devices for sensor-interfacing, real-time control and communication applications.

The family showcases a Multi-Voltage I/O (MVIO) interface with multiple pins powered by V_{DD2} and V_{DD3} that allows for these pins to operate at a different voltage domain than the rest of the microcontroller. This family features the I3C Client module with a higher communication rate and a 10-bit 300 ksps ADC with Computation for responsive sensor designs. The family also features the 8-bit Virtual Port module to interconnect digital peripherals without using external pins.

Additional features include vectored interrupt controller with fixed latency for handling interrupts, system bus arbiter, Direct Memory Access (DMA) capabilities, UART with support for asynchronous, DMX, DALI and LIN protocols, SPI, I^2C, and a programmable 32-bit CRC with memory scan. This family also includes memory features such as Memory Access Partition (MAP) and Enhanced Code Protect to support users in data protection and bootloader applications. The Device Information Area (DIA) stores factory calibration values to help improve temperature sensor accuracy.

PIC18-Q20 Family Types

Table 1. Memory Overview

Devices	PIC18F04Q20 PIC18F14Q20	PIC18F05Q20 PIC18F15Q20	PIC18F06Q20 PIC18F16Q20
Program Flash Memory	16 KB	32 KB	64 KB
Data SRAM	1 KB	2 KB	4 KB
Data EEPROM	256B	256B	256B
Memory Access Partition (MAP)	Yes	Yes	Yes
Device Information Area (DIA)	Yes	Yes	Yes
Enhanced Code Protection	Yes	Yes	Yes

Table 2. Peripheral Overview

Feature	PIC18F04Q20 PIC18F05Q20 PIC18F06Q20	PIC18F14Q20 PIC18F15Q20 PIC18F16Q20
Pins	14	20
I/O Pins	11	16
Peripheral Pin Select (PPS)	Yes	Yes
Multi-Voltage I/O (MVIO) Pins	2 (on V_{DD2})	4 (2 on V_{DD2} and V_{DD3} each)

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Feature	PIC18F04Q20 PIC18F05Q20 PIC18F06Q20	PIC18F14Q20 PIC18F15Q20 PIC18F16Q20
Virtual Port (8-Pin)	1	1
8-Bit Timer with HLT (TMR2)	2	2
16-Bit Timers (TMR0/1)	2	2
16-Bit Universal Timer (UTMR)	2	2
16-Bit Dual PWM	2	2
Capture/Compare/PWM (CCP)	2	2
Complimentary Waveform Generator (CWG)	1	1
Configurable Logic Cell (CLC)	4	4
10-Bit Analog-to-Digital Converter with Computation (ADCC) External Channels	8	11
High-Low Voltage Detect (HLVD)	1	1
Serial Peripheral Interface (SPI)	1	1
Inter-Integrated Circuit (I^2C)	1	1
Improved Inter-Integrated Circuit (I3C)	1	2
Universal Asynchronous Receiver Transmitter (UART)	1	1
UART with Protocol Support	1	1
Direct Memory Access (DMA)	4	4
Windowed Watchdog Timer (WWDT)	Yes	Yes
32-Bit CRC with Scanner	Yes	Yes
Vectored Interrupts	Yes	Yes
Interrupt-on-Change (IOC)	Yes	Yes
Peripheral Module Disable (PMD)	Yes	Yes
Temperature Indicator	Yes	Yes

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Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
  - DC – 64 MHz clock input
  - 62.5 ns minimum instruction cycle
- Four Direct Memory Access (DMA) Controllers:
  - Data transfers to SFR/GPR spaces from either Program Flash Memory, Data EEPROM or SFR/GPR spaces
  - User-programmable source and destination sizes
  - Hardware and software-triggered data transfers
- Vectored Interrupt Capability:
  - Selectable high/low priority
  - Fixed interrupt latency of three instruction cycles
  - Programmable vector table base address
  - Backwards compatible with previous interrupt capabilities
- 128-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Low-Power BOR (LPBOR) Option
- Windowed Watchdog Timer (WWDT):
  - Watchdog Reset on too long or too short interval between watchdog clear events
  - Variable prescaler selection
  - Variable window size selection

Memory

- Up to 64 KB of Program Flash Memory
- Up to 4 KB of Data SRAM Memory
- 256 Bytes Data EEPROM
- Memory Access Partition: The Program Flash Memory Can Be Partitioned into:
  - Application Block
  - Boot Block
  - Storage Area Flash (SAF) Block
- Programmable Code Protection and Write Protection
- Enhanced Code Protection
  - Permanent ICSP Disable through Configuration bit
- Device Information Area (DIA) Stores:
  - Temperature indicator factory calibrated data
  - Fixed Voltage Reference measurement data
  - Microchip Unique Identifier
- Device Characteristics Information (DCI) Area Stores:
  - Program/erase row sizes
  - Pin count details
  - EEPROM size
- Direct, Indirect and Relative Addressing Modes

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Operating Characteristics

- Operating Voltage Range (V_{DD}):
  - 1.8V to 5.5V
- Multi-Voltage I/O (MVIO) Range (V_{DD2} and V_{DD3}):
  - 1.62V to 5.5V
  - MVIO-powered pins support I3C communication down to 1.0V
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

Power-Saving Functionality

- Doze: CPU and Peripherals Running at Different Cycle Rates (CPU Is Typically Slower)
- Idle: CPU Halted While Peripherals Operate
- Sleep: Lowest Power Consumption
- Peripheral Module Disable (PMD):
  - Ability to selectively disable hardware module to minimize active power consumption of unused peripherals
- Low Power Mode Features:
  - Sleep: < 1 µA typical @ 3V
  - Operating Current:
    - 48 µA @ 32 kHz, 3V, typical

Digital Peripherals

- Two 16-Bit Pulse-Width Modulators (PWM):
  - Dual outputs for each PWM module
  - Integrated 16-bit timer/counter
  - Double-buffered user registers for duty cycles
  - Right/Left/Center/Variable Aligned modes of operation
  - Multiple clock and Reset signal selections
- Two 16-Bit Timers (TMR0/1)
- Two 8-Bit Timers (TMR2/4) with Hardware Limit Timer (HLT)
- Two 16-Bit Universal Timers (TU16A/16B):
  - New Timer module that combines most of the operations of all legacy timers (TMR0/1/2, SMT, CCP) into one single timer
  - Two 16-bit timers can be chained together to create a combined 32-bit timer
- Four Configurable Logic Cells (CLC):
  - Integrated combinational and sequential logic
- One Complimentary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Multiple signal sources
  - Programmable dead band
  - Fault-shutdown input
- Two Capture/Compare/PWM (CCP) Modules:
  - 16-bit resolution for Capture/Compare modes
  - 10-bit resolution for PWM mode
- Programmable CRC with Memory Scan:

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  - Reliable data/program memory monitoring for Fail-Safe operation (e.g., Class B)
  - Calculate 32-bit CRC over any portion of Program Flash Memory
- Two UART Modules:
  - One module (UART1) supports LIN host and client, DMX mode, DALI gear and device protocols
  - Asynchronous UART, RS-232, RS-485 compatible
  - Automatic and user timed BREAK period generation
  - Automatic checksums
  - Programmable Stop bits (1, 1.5 and 2 Stop bits)
  - Wake-up on BREAK reception
  - DMA compatible
- One SPI Module:
  - Configurable length bytes
  - Arbitrary length data packets
  - Transmit-without-receive and receive-without-transmit options
  - Transfer byte counter
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
- One I^2C Module, SMBus, PMBus™ Compatible:
  - Supports Standard mode (100 kHz), Fast mode (400 kHz) and Fast mode Plus (1 MHz) modes of operation
  - 7-bit and 10-bit Addressing modes with Address Masking modes
  - Dedicated address, transmit and receive buffers and DMA capabilities
  - Bus collision detection with arbitration
  - Bus time-out detection and handling
  - I^2C, SMBus 2.0 and SMBus 3.0, and 1.8V input level selections
  - Separate transmit and receive buffers with 2-byte FIFO and DMA capabilities
  - Multi-Host mode, including self-addressing
  - Built-in Error Detection and Recovery
- Two I3C Modules:
  - Supports I3C client device mode only
  - Adheres to MIPI I3C Basic Specification 1.0
  - Supports Dynamic Address Assignment, Common Command Codes (CCC), Direct and Broadcast addressing
  - Transfer speeds up to 12.5 Mbps in SDR mode
  - Recognizes HDR Exit pattern
  - Support for In-Band Interrupt (IBI) and Hot-Join
  - Supports 7-bit configurable client address
  - Supports Client Reset Action (RSTACT) CCC from MIPI I3C Specification 1.1
  - I^2C backward-compatible with static addressing for I^2C transfers
  - Built-in Error Detection and Recovery
- Device I/O Port Features:
  - 11 I/O pins including two Multi-Voltage I/O (MVIO) pins powered by V_{DD2} (PIC18F04/05/06Q20)
  - 16 I/O pins including two Multi-Voltage I/O (MVIO) pins powered by V_{DD2} and two MVIO pins powered by V_{DD3} (PIC18F14/15/16Q20)
  - MVIO pins support a voltage range of 1.62V through 5.5V
  - Support for 1.0-3.6V I3C communication at up to 12.5 MHz on MVIO pins
  - Individually programmable I/O direction, open-drain, slew rate and weak pull-up control
  - Interrupt-on-change on most pins
  - Three programmable external interrupt pins
- Peripheral Pin Select (PPS):
  - Enables pin mapping of digital I/O (except I3C signals)

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Analog Peripherals

- 10-Bit Analog-to-Digital Converter with Computation (ADCC):
  - Up to 11 external channels and 5 internal channels
  - Supports grouping of external channels
  - Up to 300 ksps
  - Automated math functions on input signals:
    - Averaging, filter calculations, oversampling and threshold comparison
  - Operates in Sleep
  - Five internal analog channels
  - Hardware Capacitive Voltage Divider (CVD) Support:
    - Adjustable Sample-and-Hold capacitor array
    - Guard ring digital output drive
    - Automates touch sampling and reduces software size and CPU usage when touch or proximity sensing is required
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels
  - Internal connections to ADC

Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
  - Selectable frequencies up to 64 MHz
  - ±1% at calibration
  - Active Clock Tuning of HFINTOSC for better accuracy
- 32 kHz Low-Power Internal Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOSC)
- External High-Frequency Oscillator Block:
  - Configurable HS Crystal mode up to 32 MHz
  - Digital Clock Input mode
  - 4x PLL with external sources
- Fail-Safe Clock Monitor:
  - Allows for operational recovery if external clock stops
- Oscillator Start-up Timer (OST):
  - Ensures stability of crystal oscillator sources

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip

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1. Packages

Table 1-1. Packages

Device	14-Pin SOIC	14-Pin TSSOP	20-Pin PDIP	20-Pin SOIC	20-Pin SSOP	20-Pin VQFN
PIC18F04Q20	●	●				
PIC18F05Q20	●	●				
PIC18F06Q20	●	●				
PIC18F14Q20			●	●	●	●
PIC18F15Q20			●	●	●	●
PIC18F16Q20			●	●	●	●

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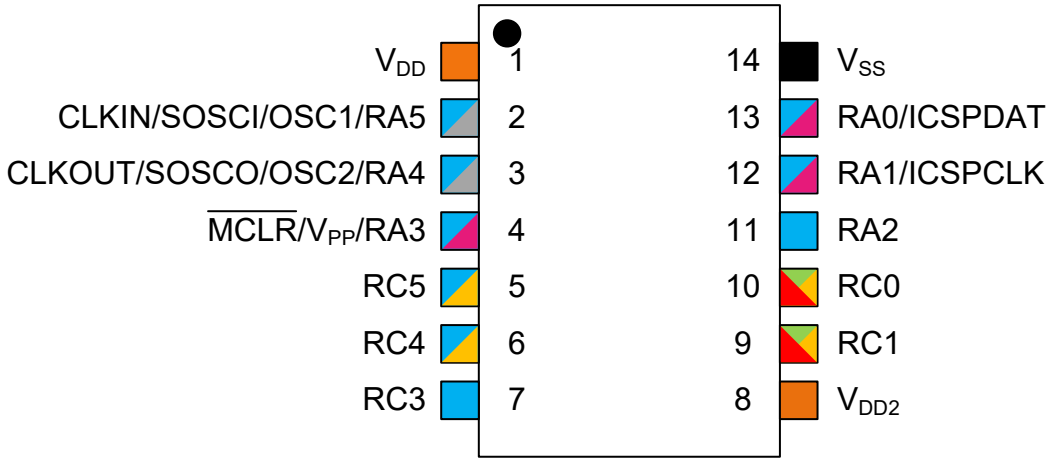
2. Pin Diagrams

Figure 2-1.
14-Pin SOIC
14-Pin TSSOP



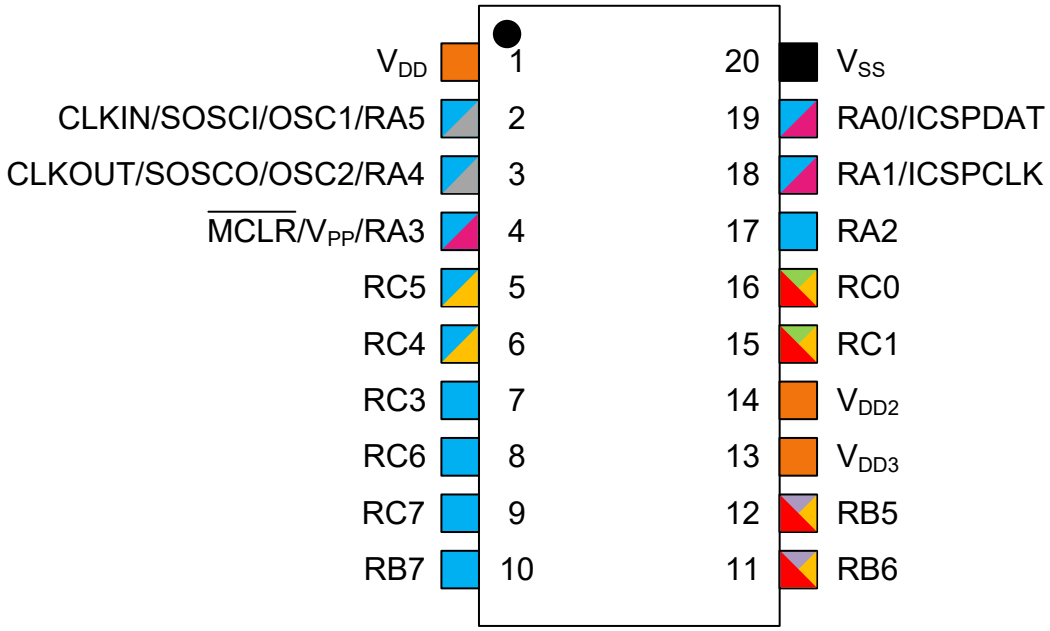
Power

- Power Supply
- Ground
- Pin on V_{DD} Power Domain
- Pin on V_{DD2} Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- I^2C/SMBus-compatible
- I3C-compatible

Figure 2-2.
20-Pin PDIP
20-Pin SOIC
20-Pin SSOP



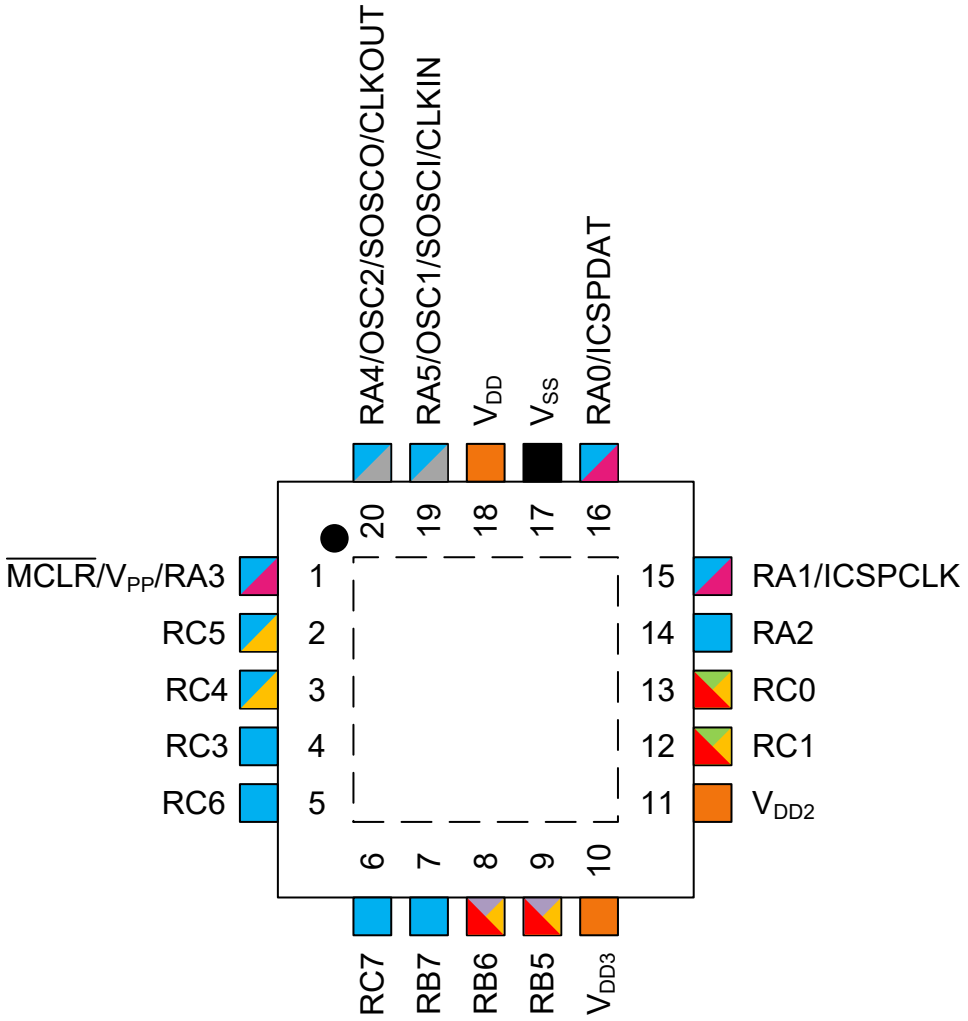
Power

- Power Supply
- Ground
- Pin on V_{DD} Power Domain
- Pin on V_{DD2} Power Domain
- Pin on V_{DD3} Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- I^2C/SMBus-compatible
- I3C-compatible

Figure 2-3.
20-Pin VQFN



Power

- Power Supply
- Ground
- Pin on V_{DD} Power Domain
- Pin on V_{DD2} Power Domain
- Pin on V_{DD3} Power Domain

Functionality

- Programming/Debug
- Clock/Crystal
- I^2C/SMBus-compatible
- I3C-compatible

Note: It is recommended that the exposed bottom pad be connected to V_{SS}; however, it must not be the only V_{SS} connection to the device.

3. Pin Allocation Tables

Table 3-1. 14-Pin Allocation Table

I/O	14-Pin SOIC/ TSSOP	A/D	Reference	Timers	16-Bit PWM/CCP	CWG	CLC	SPI	I^2C	I3C	UART	IOC	Interrupts	Basic
RA0	13	ANA0	—	—	—	—	—	—	—	—	—	IOCA0	—	ICDDAT ICSPDAT
RA1	12	ANA1	VREF+ (ADC)	TUIN0(1)	—	—	—	—	—	—	—	IOCA1	—	ICDCLK ICSPCLK
RA2	11	ANA2	VREF- (ADC)	T0CKI(1)	—	CWG1IN(1)	—	—	—	—	—	IOCA2	INT0(1)	—
RA3	4	—	—	—	—	—	—	—	—	—	—	IOCA3	—	$\overline{MCLR}$ V_{PP}
RA4	3	ANA4	—	T1G(1)	—	—	—	—	—	—	—	IOCA4	INT1(1)	CLKOUT SOSCO OSC2
RA5	2	ANA5	—	T1CKI(1) T2IN(1)	PWM1ERS(1)	—	CLCIN3(1)	—	—	—	—	IOCA5	INT2(1)	CLKIN SOSCI OSC1
RC0(7)	10	—	—	TUIN1(1)	—	—	—	SCK1(1)	SCL1(3,4)	I3C1_SCL(5)	CTS2(1)	IOCC0	—	—
RC1(7)	9	—	—	T4IN(1)	PWM2ERS(1)	—	CLCIN2(1)	SDI1(1)	SDA1(3,4)	I3C1_SDA(5)	RX2(1)	IOCC1	—	—
RC3	7	ANC3 ADACT(1)	—	—	CCP2IN(1) PWMIN1(1)	—	CLCIN0(1)	SS1(1)	—	—	—	IOCC3	—	—
RC4	6	ANC4	—	—	—	—	CLCIN1(1)		—	—	CTS1(1)	IOCC4	—	—
RC5	5	ANC5	—	—	CCP1IN(1) PWMIN0(1)	—	—	—	—	—	RX1(1)	IOCC5	—	—
V_{DD}	1	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{DD2}	8	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD2}
V_{SS}	14	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	ADCGRDA ADCGRDB	—	TMR0 TU16A TU16B	PWM11 PWM12 PWM21 PWM22 CCP1 CCP2	CWG1A CWG1B CWG1C CWG1D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	SS1 SCK1 SDO1	SDA1 SCL1	—	DTR1 RTS1 TX1 DTR2 RTS2 TX2	—	—	—

Notes:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All digital output signals shown in these rows are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options.
3. This is a bidirectional signal. For normal module operation, the firmware will map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins are configured for I^2C logic levels; the SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RB1) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.
5. These pins are configured for I3C logic levels and are not PPS remappable. MVIO must be enabled on these pins to be compliant with the I3C bus standards.
6. A 0.1 uF bypass capacitor to V_{SS} is required on the V_{DD} pin.
7. MVIO pins, powered by V_{DD2}.

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Table 3-2. 20-Pin Allocation Table

I/O	20-Pin PDIP/ SOIC/ TSSOP	20-Pin VQFN	A/D	Reference	Timers	16-Bit PWM/CCP	CWG	CLC	SPI	I^2C	I3C	UART	IOC	Interrupts	Basic
RA0	19	16	ANA0		—	—	—	—	—	—	—	—	IOCA0	—	ICDDAT ICSPDAT
RA1	18	15	ANA1	VREF+ (ADC)	TUIN0(1)	—	—	—	—	—	—	—	IOCA1	—	ICDCLK ICSPCLK
RA2	17	14	ANA2	VREF- (ADC)	T0CKI(1)	—	CWG1IN(1)	CLCIN0(1)	—	—	—	—	IOCA2	INT0(1)	—
RA3	4	1	—	—	—	—	—	—	—	—	—	—	IOCA3	—	$\overline{MCLR}$ V_{PP}
RA4	3	20	ANA4	—	T1G(1)	—	—	—	—	—	—	—	IOCA4	INT1(1)	CLKOUT SOSCO OSC2
RA5	2	19	ANA5	—	T2IN(1) T1CKI(1)	PWM1ERS (1)	—	—	—	—	—	—	IOCA5	INT2(1)	CLKIN SOSCI OSC1
RB5(8)	12	9	—	—	—	—	—	CLCIN3(1)	SDI1(1)	SDA1(3,4)	I3C2_SDA(5)	RX1(1)	IOCB5	—	—
RB6(8)	11	8	—	—	—	—	—	CLCIN2(1)	SCK1(1)	SCL1(3,4)	I3C2_SCL(5)	—	IOCB6	—	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	CTS1(1)	IOCB7	—	—
RC0(7)	16	13	—	—	TUIN1(1)	—	—	—	—	—	I3C1_SCL(5)	CTS2(1)	IOCC0	—	—
RC1(7)	15	12	—	—	T4IN(1)	PWM2ERS (1)	—	—	—	—	I3C1_SDA(5)	RX2(1)	IOCC1	—	—
RC3	7	4	ANC3 ADACT(1)	—	—	CCP2IN(1) PWMIN1(1)	—	CLCIN1(1)	—	—	—	—	IOCC3	—	—
RC4	6	3	ANC4	—	T3G(1)	—	—	—	—	—	—	—	IOCC4	—	—
RC5	5	2	ANC5	—	T3CKI(1)	CCP1IN(1) PWMIN0(1)	—	—	—	—	—	—	IOCC5	—	—
RC6	8	5	ANC6	—	—	—	—	—	SS1(1)	—	—	—	IOCC6	—	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	IOCC7	—	—
V_{DD}	1	18	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD}
V_{DD2}	14	11	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD2}
V_{DD3}	13	10	—	—	—	—	—	—	—	—	—	—	—	—	V_{DD3}
V_{SS}	20	17	—	—	—	—	—	—	—	—	—	—	—	—	V_{SS}
OUT(2)	—	—	ADCGRDA ADCGRDB	—	TMR0 TU16A TU16B	PWM11 PWM12 PWM21 PWM22 CCP1 CCP2	CWG1A CWG1B CWG1C CWG1D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	SS1 SCK1 SDO1	SDA1 SCL1	—	DTR1 RTS1 TX1 DTR2 RTS2 TX2	—	—	—

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.....continued

I/O	20-Pin PDIP/ SOIC/ TSSOP	20-Pin VQFN	A/D	Reference	Timers	16-Bit PWM/CCP	CWG	CLC	SPI	I^2C	I3C	UART	IOC	Interrupts	Basic

Notes:

1. This is a PPS remappable input signal. The input function may be moved from the default location shown to one of several other PORTx pins.
2. All digital output signals shown in these rows are PPS remappable. These signals may be mapped to output onto one of several PORTx pin options.
3. This is a bidirectional signal. For normal module operation, the firmware will map this signal to the same pin in both the PPS input and PPS output registers.
4. These pins are configured for I^2C logic levels; the SCLx/SDAx signals may be assigned to any of these pins. PPS assignments to the other pins (e.g., RB1) will operate, but input logic levels will be standard TTL/ST as selected by the INLVL register, instead of the I^2C specific or SMBus input buffer thresholds.
5. These pins are configured for I3C logic levels and are not PPS remappable. MVIO must be enabled on these pins to be compliant with the I3C bus standards.
6. A 0.1 uF bypass capacitor to V_{SS} is required on the V_{DD} pin.
7. MVIO pins, powered by V_{DD2}.
8. MVIO pins, powered by V_{DD3}.

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- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
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