NEW 8-BIT MICROCONTROLLER ARCHITECTURE FEATURES COMPLETE SOFTWARE, HARDWARE DESIGN REUSABILITY

- Larger Code Memory
- C Compiler Efficiency
- Seamless Code Migration
- SOC, System Partitioning Applications

CHANDLER, Ariz., July 6, 1999 [NASDAQ: MCHP] — Microchip Technology Inc. today introduced the world’s first 8-bit RISC microcontroller architecture to provide complete software and hardware design reusability for embedded control engineers.

Microchip’s new PIC18CXXX architecture allows the thousands of existing PICmicro® 8-bit RISC microcontroller users to seamlessly migrate their designs to higher integration while maintaining their code investment, engineering knowledge and hardware investment via socket compatibility with existing printed-circuit boards. Microchip will continue to support its current PICmicro architecture along with the new PIC18CXXX architecture.

“With larger code memory and C compiler friendly tools, the PIC18CXXX extends the reach of the PICmicro 8-bit core to new customers and market segments,” said Steve Sanghi, president and CEO of Microchip. “Any organization using microcontrollers today can help solve their business problems with the flexible PICmicro architecture and maximum design reusability. Delivering the whole product solution is Microchip’s biggest competitive advantage: competitive price/performance, consistent delivery, sophisticated development systems, worldwide field-application support, wide market acceptance, and more than 110 devices with one-time-programmable (OTP), Flash and ROM variants for the most appropriate stage of the product lifecycle.”

- MORE -
ADD ONE – NEW PIC18CXXX ARCHITECTURE

The PIC18CXXX architecture offers up to two million bytes of program memory address space, a C compiler friendly development environment and 8-bit microcontroller industry-leading 10 MIPS performance at 40 MHz. In separate announcements today, Microchip debuted the first four PIC18CXXX devices, the PIC18C242, PIC18C442, PIC18C252 and PIC18C452 8-bit microcontrollers, and MPLAB™-C18 C Compiler. Microchip plans a suite of new PIC18CXXX devices in the next two years featuring Flash, OTP and ROM memories.

PIC18CXXX Architecture: Technical Specifications

The PIC18CXXX architecture is an enhanced RISC core that is upward compatible from Microchip’s Mid-Range PIC12C6XX and PIC16CXXX core and High-End PIC17CXXX core. The PIC18CXXX architecture features:

- **Linear address space.** The on-chip memory addressing of the PIC18CXXX architecture is expanded to accommodate up to two million bytes of program memory and 4K bytes of data memory. As 8-bit microcontroller applications increase in complexity, memory requirements have grown rapidly.

- **Additional instructions.** The PIC18CXXX combines the bit-manipulation instructions from the existing Mid-Range and byte manipulation instructions from the High-End PICmicro CPUs, including the 8x8 single cycle hardware multiply and table read/write. The PIC18CXXX is a 16-bit instruction and 8-bit data ALU architecture, offering higher performance at an attractive price.

- MORE -
ADD TWO – NEW PIC18CXXX ARCHITECTURE

• **Designed for C compiler efficiency.** As the microcontroller memory size has increased, so has the use of high-level language compilers. Systems using 4K words of program memory and greater usually write code in a high-level language such as ANSI C. Microcontrollers have traditionally been programmed in assembly code so the compiler target was not ideal.

  Linear program memory removes all paging-related overhead. Data memory is highly linear as well. There are 128 bytes of “Access RAM” highly suitable for global variable allocation. Three 12-bit-wide data pointer registers with pre-increment, post-increment, post-decrement and offset-addressing modes make it possible to implement the run-time parameter stack efficiently. The top of the hardware PC stack is readable and writable, making it possible to manage the stack entirely in software. This also makes the PIC18CXXX very suitable for RTOS implementation.

• **Modular emulation tool.** Microchip’s new modular emulator technology features a two-chip design which enhances system validation and overall productivity. A standard PICmicro device is used in the emulator featuring a special “emulation mode” (see attached diagram).

  A combination of Master-Slave emulator chips emulate the actual part. The Master chip emulates the CPU and the program memory access. The Slave chip emulates all the peripherals. The Slave emulator is simply a standard production part in a special emulation mode. The result is exact emulation of complex peripherals. Sensitive modules such as analog-to-digital converters and voltage references are emulated with no differences from the actual product. All peripherals with complex timing input and output are also the same as the real product. This provides easier system validation with a higher degree of emulation accuracy.

  - MORE -
ADD THREE – NEW PIC18CXXX ARCHITECTURE

- **Code compatible.** The PIC18CXXX architecture is source code compatible with existing PIC12C6XX and PIC16CXXX microcontrollers. Any assembly or C source code written for the PIC12C6XX and PIC16CXXX will transfer to the PIC18CXXX architecture. Source code written for the PIC17CXXX will transfer with minor modification.

**Flexible Programming**

Microchip’s PICmicro OTP and Flash microcontrollers feature In-Circuit Serial Programming™ (ICSP™), which allows the microcontroller to be programmed after being placed in a circuit board. This offers tremendous flexibility, reduces development time and manufacturing cycles, and improves time to market. ICSP also enables reduced cost of field upgrades, system calibration during manufacturing, the addition of unique identification codes to the system and calibration of system in the field. Requiring only two I/O pins for most devices, Microchip offers the most non-intrusive programming available today.

**Targeting New Markets and Applications**

The PIC18CXXX enables system partitioning and low-cost system-on-a-chip (SOC) capability in embedded systems designs. Leading engineers are carefully partitioning the embedded hardware into digital logic that can take advantage of high integration and flexible non-volatile memory that can meet demands for user interfaces which can change rapidly. The PIC18CXXX provides designers with a single-chip system solution that complements the digital logic by merging the flexibility of OTP memory with advanced analog functionality at a competitive 8-bit microcontroller price. This optimizes the performance of a 32-bit microprocessor, digital signal processor or SOC.

Applications for PIC18CXXX devices are wide ranging and may include any of the thousands of existing applications in the automotive, communications, consumer, industrial control and office automation markets currently served by PICmicro devices.

- MORE -
ADD FOUR – NEW PIC18CXXX ARCHITECTURE

PIC18CXXX Development Systems

The PIC18CXXX is supported by the MPLAB-C18 C Compiler, a complete high-level language compiler for the company’s new PIC18CXXX 8-bit RISC microcontroller architecture. MPLAB-C18 is expected to be available August 1999 for $495 each. A 30-day full-featured demo of MPLAB-C18 can be downloaded from Microchip’s web site www.microchip.com at no cost starting in July.

The MPLAB-ICE 2000 Universal In-Circuit Emulator provides high-performance real-time emulation for the PIC18CXXX. The system features the sophisticated MPLAB Integrated Development Environment. Interchangeable processor modules and device adapters allow the emulator system to be easily configured to emulate different processors. MPLAB-ICE 2000 emulates voltages as low as 2.0 volts and can emulate at full speed. Operating in the Microsoft Windows environment, MPLAB gives users the flexibility to edit, simulate, compile, and emulate all from a single user interface—at no additional cost. Pricing for MPLAB-ICE 2000 starts at $1,995. Microchip offers additional support, including development and programming tools.

PIC18CXXX Devices

The PIC18CXXX architecture is initially being implemented in four microcontroller devices. Current PIC18CXXX microcontrollers feature 16K to 32K bytes of on-chip EPROM (OTP) program memory and 512 bytes to 1536 bytes of data SRAM. Available in 28- and 40-pin configurations, these devices provide various feature sets of 10-bit analog-to-digital converters; capture, compare and pulse-width modulation; and I2C, SPI, and high performance USART communications capability. Future implementations are expected to support the CAN 2.0B specification in 28- to 84-pin devices and support USB in 28- to 40-pin devices. Other planned microcontrollers will feature Flash memory. Contact any Microchip sales representative or authorized worldwide distributor for more information.

- MORE -
ADD FIVE – NEW PIC18CXXX ARCHITECTURE

Microchip Technology Inc. manufactures the PICmicro® family of 8-bit RISC-based microcontrollers—with OTP, Flash, and ROM memory technologies; serial EEPROMs and related specialty memory products; microID™ family of RFID products and KEELOQ® code hopping devices. These products target thousands of embedded control applications in the consumer, automotive, office automation, communications and industrial markets. Microchip’s quality systems are ISO 9001 certified. Headquartered near Phoenix in Chandler, Ariz., Microchip employs approximately 1,865 people worldwide and has sales offices throughout Asia, Europe, Japan and the Americas.

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Feature sets of the PICmicro 8-bit microcontroller core and the new PIC18CXXX architecture.

<table>
<thead>
<tr>
<th>Family</th>
<th>PIC12C5XX</th>
<th>PIC12C6XX</th>
<th>PIC16C6X</th>
<th>PIC16C62X</th>
<th>PIC16C7X</th>
<th>PIC16F8XX</th>
<th>PIC16C92X</th>
<th>PIC16F92X</th>
<th>PIC17C4X</th>
<th>PIC17C7XX</th>
<th>PIC18CXXX</th>
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<tbody>
<tr>
<td>Instruction Width</td>
<td>12 bits</td>
<td>14 Bits</td>
<td>16 Bits</td>
<td>16 Bits</td>
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<tr>
<td>Number of</td>
<td>33</td>
<td>35</td>
<td>58</td>
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<td>Instructions</td>
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<tr>
<td>Program Memory</td>
<td>Up to 4K Bytes</td>
<td>Up to 16K Bytes</td>
<td>Up to 128K Bytes</td>
<td>Up to 2M Bytes</td>
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<tr>
<td>Data Memory</td>
<td>Up to 80 Bytes</td>
<td>Up to 368 Bytes</td>
<td>Up to 902 Bytes</td>
<td>Up to 4K Bytes</td>
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<td>Pin Counts</td>
<td>8-28</td>
<td>8-68</td>
<td>40-84</td>
<td>28-84</td>
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<tr>
<td>Interrupts</td>
<td>None</td>
<td>Up to 12 single vectored</td>
<td>Up to 18 vectored</td>
<td>Up to 14 vectored, prioritized, with fast interrupt</td>
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<td>Peripherals</td>
<td>Timer/counter, on-chip 4 MHz clock oscillator</td>
<td>Timer/counter, on-chip 4 MHz clock oscillator, USART, capture, compare, pulse width modulation, 8- to 12-bit analog-to-digital converter (A/D), comparators, LCD driver, on-chip temperature sensor, digital-to-analog converter, high-resolution 16-bit slope A/D</td>
<td>Timer/counter, USART, capture, pulse width modulation, 10-bit A/D</td>
<td>Timer/counter, USART, capture, compare, pulse width modulation, 10-bit A/D, comparators, voltage reference</td>
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<td>Special MCU</td>
<td>Power-down mode, watchdog timer, power-on reset, internal 4 MHz oscillator</td>
<td>Power-down mode, watchdog timer, power-on reset, programmable brown-out detect, programmable low-voltage detect</td>
<td>Power-down mode, watchdog timer, power-on reset, brown-out detect</td>
<td>Power-down mode, watchdog timer, power-on reset, programmable brown-out detect, low-voltage detect</td>
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<td>Features</td>
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NOTE: Microchip plans to implement all Mid-Range/ PIC16CXXX peripherals on the PIC18CXXX.