Highlights

- Non-blocking wire-speed Ethernet switching fabric
- Full-featured forwarding and filtering control, including Access Control List (ACL) filtering
- Full VLAN and QoS support
- Two ports with integrated 10/100/1000BASE-T PHYs
- One port with 10/100/1000 Ethernet MAC and configurable RGMII/MII/RMII interface
- EtherSynch® IEEE 1588v2 Precision Time Protocol (PTP) and IEEE 802.1AS/Qav Audio Video Bridging (AVB) support
- IEEE 802.1X port-based authentication support
- EtherGreen™ power management features, including low power standby and IEEE 802.3az
- Flexible management interface options: SPI, I²C, MII, and in-band management via any port
- Commercial/Industrial temperature range support
- 64-pin VQFN (8 x 8mm) lead-free package

Target Applications

- Industrial Ethernet (Profinet, MODBUS, Ethernet/IP)
- Real-time Ethernet networks
- Industrial control/automation switches
- Networked measurement and control systems
- Test and measurement equipment

Features

Switch Management Capabilities

- 10/100/1000Mbps Ethernet switch basic functions: frame buffer management, address look-up table, queue management, MIB counters
- Non-blocking store-and-forward switch fabric assures fast packet delivery by utilizing 4096 entry forwarding table with 128KByte frame buffer
- Jumbo packet support up to 9000 bytes
- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port
- Rapid spanning tree protocol (RSTP) support for topology management and ring/linear recovery
- Multiple spanning tree protocol (MSTP) support

One Configurable External MAC Port

- Reduced Gigabit Media Independent Interface (RGMII) v2.0
- Reduced Media Independent Interface (RMII) v1.2 with 50MHz reference clock input/output option
- Media Independent Interface (MII) in PHY/MAC mode

Advanced Switch Capabilities

- IEEE 802.1Q VLAN support for 128 active VLAN groups and the full range of 4096 VLAN IDs
- IEEE 802.1p/Q tag insertion/removal on per port basis
- VLAN ID tag/untag options on per port or VLAN basis
- IEEE 802.3x full-duplex flow control and half-duplex back pressure collision control
- IEEE 802.1X (Port-Based Network Access Control)
- IGMP v1/v2/v3 snooping for multicast packet filtering
- IPv6 multicast listener discovery (MLD) snooping
- IPv4/IPv6 QoS support, QoS/CoS packet prioritization
- 802.1p QoS packet classification with 4 priority queues
- Programmable rate limiting at ingress/egress ports

EtherSynch® IEEE 1588v2 PTP

- Transparent Clock (TC) with auto correction update
- Master and slave Ordinary Clock (OC) support
- End-to-end (E2E) or peer-to-peer (P2P)
- PTP multicast and unicast message support
- PTP message transport over IPv4/IPv6 and IEEE 802.3
- IEEE 1588v2 PTP packet filtering
- Synchronous Ethernet support via recovered clock

EtherSynch® Audio Video Bridging (AVB)

- Compliant with IEEE 802.1BA/AS/Qat/Qav standards
- gPTP time synchronization, credit-based traffic shaper

Comprehensive Configuration Registers Access

- High-speed 4-wire SPI (up to 50MHz), I²C interfaces provide access to all internal registers
- MII Management (MII/MDC/MDCI 2-wire) Interface provides access to all PHY registers
- In-band management via any of the three ports
- I/O pin strapping facility to set certain register bits from I/O pins at reset time

Power Management

- IEEE 802.3az Energy Efficient Ethernet (EEE)
- Energy detect power-down mode on cable disconnect
- Dynamic clock tree control
- Unused ports can be individually powered down
- Full-chip software power-down
- Wake-on-LAN (WoL) standby power mode
TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at docerrors@microchip.com. We welcome your feedback.

Most Current Documentation

To obtain the most up-to-date version of this documentation, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

• Microchip’s Worldwide Web site; http://www.microchip.com
• Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include -literature number) you are using.

Customer Notification System

Register on our web site at www.microchip.com to receive the most current information on all of our products.
1.0 INTRODUCTION

1.1 General Description

The KSZ9563RNX is a highly-integrated, IEEE 802.3 compliant networking device that incorporates a layer-2+ managed Gigabit Ethernet switch, two 10BASE-T/100BASE-TX/1000BASE-T physical layer transceivers (PHYs) and associated MAC units, and one MAC port with a configurable RGMII/MII/RMII interface for direct connection to a host processor/controller, another Ethernet switch, or an Ethernet PHY transceiver.

The KSZ9563RNX is built upon industry-leading Ethernet technology, with features designed to offload host processing and streamline the overall design:

- Non-blocking wire-speed Ethernet switch fabric
- Full-featured forwarding and filtering control, including port-based Access Control List (ACL) filtering
- Full VLAN and QoS support
- Traffic prioritization with per-port ingress/egress queues and by traffic classification
- Spanning Tree support for RSTP and MSTP
- IEEE 802.1X port-based authentication support

The KSZ9563RNX incorporates full hardware support for the IEEE 1588v2 Precision Time Protocol (PTP), including hardware time-stamping at all PHY-MAC interfaces, and a high-resolution hardware "PTP clock". IEEE 1588 provides sub-microsecond synchronization for a range of industrial Ethernet applications.

The KSZ9563RNX fully supports the IEEE family of Audio Video Bridging (AVB) standards, which provides high Quality of Service (QoS) for latency sensitive traffic streams over Ethernet. Time-stamping and time-keeping features support IEEE 802.1AS time synchronization. All ports feature credit based traffic shapers for IEEE 802.1Qav.

A host processor can access all KSZ9563RNX registers for control over all PHY, MAC, and switch functions. Full register access is available via the integrated SPI or I2C interfaces, and by in-band management via any one of the data ports. PHY register access is provided by a MIIM interface. Flexible digital I/O voltage allows the MAC port to interface directly with a 1.8/2.5/3.3V host processor/controller/FPGA.

Additionally, a robust assortment of power-management features including IEEE 802.3az Energy-Efficient Ethernet (EEE) for power savings with idle link, and Wake-on-LAN (WoL) for low power standby operation, have been designed to satisfy energy-efficient system requirements.

The KSZ9563RNX is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature ranges. An internal block diagram of the KSZ9563RNX is shown in Figure 1-1.

**FIGURE 1-1: INTERNAL BLOCK DIAGRAM**
2.0 PACKAGE INFORMATION

2.1 Package Drawings

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

FIGURE 2-1: PACKAGE (DRAWING)

64-Lead Very Thin Plastic Quad Flat, No Lead Package (JXX) - 8x8 mm Body [VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
FIGURE 2-2: PACKAGE (DIMENSIONS)

64-Lead Very Thin Plastic Quad Flat, No Lead Package (JXX) - 8x8 mm Body [VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Terminals</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Terminal Thickness</td>
<td>A3</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
</tr>
<tr>
<td>Terminal Width</td>
<td>b</td>
</tr>
<tr>
<td>Terminal Length</td>
<td>L</td>
</tr>
<tr>
<td>Terminal-to-Exposed-Pad</td>
<td>K</td>
</tr>
</tbody>
</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
### FIGURE 2-3: PACKAGE (LAND PATTERN)

64-Lead Very Thin Plastic Quad Flat, No Lead Package (JXX) - 8x8 mm Body [VQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

#### RECOMMENDED LAND PATTERN

<table>
<thead>
<tr>
<th>Dimension Limits</th>
<th>Units</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contact Pitch</td>
<td>E</td>
<td>0.40 BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Optional Center Pad Width</td>
<td>X2</td>
<td>6.60</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Optional Center Pad Length</td>
<td>Y2</td>
<td>6.60</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
<td>7.90</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C2</td>
<td>7.90</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pad Width (X64)</td>
<td>X1</td>
<td>0.20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pad Length (X64)</td>
<td>Y1</td>
<td>0.20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Contact Pad to Center Pad (X64)</td>
<td>G1</td>
<td>0.20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Via Diameter</td>
<td>V</td>
<td>0.33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Via Pitch</td>
<td>EV</td>
<td>1.20</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process
### APPENDIX A: PRODUCT BRIEF REVISION HISTORY

#### TABLE A-1: REVISION HISTORY

<table>
<thead>
<tr>
<th>Revision</th>
<th>Section/Figure/Entry</th>
<th>Correction</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS00002319A (12-16-16)</td>
<td>Initial Document Release</td>
<td></td>
</tr>
</tbody>
</table>
THE MICROCHIP WEB SITE

Microchip provides online support via our WWW site at www.microchip.com. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user’s guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

CUSTOMER CHANGE NOTIFICATION SERVICE

Microchip’s customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.

To register, access the Microchip web site at www.microchip.com. Under “Support”, click on “Customer Change Notification” and follow the registration instructions.

CUSTOMER SUPPORT

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

**Technical support is available through the web site at:** http://www.microchip.com/support
## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>XX</th>
<th>X</th>
<th>(XX)</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temp. Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tape &amp; Reel Option</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Examples:**

a) KSZ9563RNXC
   64-pin VQFN package,
   Commercial temperature,
   Standard packaging

b) KSZ9563RNXI-TR
   64-pin VQFN package,
   Industrial temperature,
   Tape and reel

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

**Examples:**

a) KSZ9563RNXC
   64-pin VQFN package,
   Commercial temperature,
   Standard packaging

b) KSZ9563RNXI-TR
   64-pin VQFN package,
   Industrial temperature,
   Tape and reel

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks
The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Heido, JukeBlox, KeeLoq, KeeLoq logo, Kleer, LANcheck, LINK MD, mAStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.


SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2016, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 9781522411147

QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV — ISO/TS 16949 —

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company’s quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001:2000 certified.