Improving Linear Regulator
Power Supply Ripple Rejection (PSRR) and Output Noise

Qi Deng
Senior Product Marketing Engineer, Analog and Interface Products Division
Microchip Technology Inc.

In this article, we focus on two key application-oriented parameters of the linear regulator: Power Supply Ripple Rejection (PSRR) and output noise. These parameters have been discussed before (see “References”). This article provides a practical and straightforward approach that is useful to design engineers of many experience and education levels.

Before moving forward, it is necessary to review the five main types of linear regulators. These include the standard NPN, NPN pass transistor, PNP pass transistor, P-channel FET, and N-channel FET regulators. All linear regulators consist of three important elements:

1. A pass element
2. A bandgap voltage reference (bandgap)
3. An error amplifier

**PSRR**

PSRR is defined as the linear regulator’s ability to eliminate output ripple caused by input variations. High PSRR values are desirable over the frequency range that is critical to the linear regulator, typically 10 Hz to 10 MHz. Mathematically, PSRR is the reverse gain of the output ripple over the input ripple at a particular frequency. For LDOs, specifically, the PSRR is given as:

$$PSRR = 20\log(|A_V/A_{VO}|), \text{ expressed in dB}$$  \hspace{1cm} (Equation 1)

*where $A_V$ is the open-loop gain of the feedback loop, and $A_{VO}$ is the gain from $V_{IN}$ to $V_{OUT}$ when feedback loop is open.*

The PSRR of a linear regulator is determined by three factors:

1. The PSRR of the bandgap voltage reference, whose output ripple affects the output ripple of the linear regulator up to the roll-off frequency of the bandgap.
2. The open-loop gain of the feedback loop ($A_V$), which is roughly equal to the open-loop gain of the error amplifier, up to the 0dB (unity gain) crossover frequency of the linear regulator (Equation 1).
3. The open-loop gain from $V_{IN}$ to $V_{OUT}$ ($A_{VO}$), which is determined by the parasitic parameters of the pass element and values of external components (especially the output capacitor) along the $V_{IN}$ to $V_{OUT}$ path, starting from the 0dB crossover frequency (Equation 1).

The PSRR of the bandgap is a critical contributor to the PSRR of the linear regulator up to the bandgap’s roll-off frequency, since any bandgap output ripple is amplified by the error amplifier, which in turn propagates the amplified ripple through the pass element to $V_{OUT}$. In practice, bandgap PSRR values for all five types of linear regulators are comparable.

In addition to having a bandgap with high intrinsic PSRR, it is a common practice to “bypass” its output ripple to the ground through a low-pass filter before it reaches the error amplifier input. The low-pass filter is typically constructed with an internal resistor and an external capacitor. Its roll-off frequency should be as low as possible (100Hz typical), which enables it to filter out high frequency output ripple. This means the value of the RC should be high. Typically, the internal resistor has a very high value -- in the hundreds of KΩ range. The external capacitor usually has a relatively low value -- in the nF or even hundreds of pF range. This is because too large a capacitor negatively impacts the start-up response of the linear regulator (Figure 1, using a P-channel FET regulator as example).
The open-loop gain of the feedback loop ($A_v$) is the critical contributor to the PSRR of the linear regulator above the roll-off frequency of the bandgap low-pass filter and up to the 0dB crossover frequency. There are two determining parameters:

1. The open-loop gain of the error amplifier, which is roughly equal to the open-loop gain of the feedback loop, up to the 0dB crossover frequency. As Equation 1 shows, the higher the open-loop gain of the error amplifier, the better the PSRR.

2. The 0dB crossover frequency, which is determined by either the unity-gain (0dB) frequency of the error amplifier, or the structure of the pass element (standard NPN, NPN pass transistor, PNP pass transistor, P-channel, N-channel). Typically, a very high unity-gain error amplifier is used, so usually the structure of the pass element determines the 0dB crossover frequency.

Therefore, in order to achieve a high open-loop gain for the feedback loop, a high open-loop gain error amplifier (with high unity-gain frequency) should be used. In addition, a pass element with reasonably low intrinsic capacitance, and therefore a high 0dB crossover frequency, is desirable. In this article, we assume that both the open-loop gain of the error amplifier and the intrinsic capacitance of the pass element are fixed. Therefore, the only practical way to improve the PSRR, at least from external of the linear regulator, is through decreasing the capacitance of the output capacitor.

Beyond the 0dB crossover frequency, the parasitic parameters of the internal and external components along the $V_{IN}$ to $V_{OUT}$ path, including the pass element and the output capacitor, start to dominate, with the capacitance of the output capacitor being most significant. Improving the PSRR in this frequency range is typically accomplished by increasing the capacitance of the output capacitor.

With the above knowledge, we now examine the PSRR characteristics and methods of improvement for each of the five types of linear regulators.

The standard NPN regulator uses dominant pole compensation to keep the loop stable. The frequency of the dominant pole is given by:

$$f(P_{INT}) = 1/(2\pi R_{INT}C_{INT})$$  \hspace{1cm} (Equation 2)

*where $R_{INT}$ and $C_{INT}$ are the regulator’s intrinsic resistance and capacitance*
The addition of an output capacitor, which is not required for loop stability, effectively “increases” the regulator’s intrinsic capacitance $C_{\text{INT}}$. Equation 2 shows that the increased intrinsic capacitor moves the dominant pole to a lower frequency, which decreases the 0dB crossover frequency, and reduces the PSRR between the new and old 0dB crossover points. As a result, although the added output capacitor filters out more ripple and therefore improves the PSRR beyond the old 0dB crossover point, its impact on the overall PSRR below the old 0dB crossover frequency is negative. As such, it is not practical to increase the overall PSRR of a standard NPN regulator through external means of improvement. Rather, its intrinsic capacitance needs to be reduced, to the point that the regulator can still maintain stable operation (Figure 2).

Figure 2. Standard NPN Regulator PSRR and Output Noise
Things are a little more complicated for the NPN pass transistor regulator, which also has an intrinsic dominant pole but requires an output capacitor for stability. Again, from Equation 2, we can see that increasing the capacitance of the output capacitor moves the dominant pole to a lower frequency, which decreases the 0dB crossover frequency.

However, one of the functions of the output capacitor is to add a ZERO to keep the loop stable. The frequency of the ZERO is given by:

$$f(Z_{COMP}) = \frac{1}{2\pi \times ESR \times C_{OUT}}$$

(Equation 3)

As seen in Equation 3, decreasing the capacitance of the output capacitor increases the frequency of the ZERO, which actually decreases the 0dB crossover frequency.

Therefore, in theory, whether the added capacitance increases or decreases the 0dB crossover frequency for the NPN pass transistor regulator cannot easily be determined, at least on first-order approximation. In practice, the added capacitance typically decreases the 0dB crossover frequency because $f(P_{IN})$ drops faster than $f(ZERO)$ with an increase in the output capacitor. This effectively reduces the PSRR between the old and new 0dB crossover points. If improving the PSRR at a high frequency and reducing overall output noise are not critical, the common practice is to decrease the output capacitance in order to improve the PSRR (Figure 3).

The same conclusion is applicable to the N-channel FET regulator (Figure 3).
Figure 3. NPN Pass Transistor Regulator & N-Channel FET Regulator PSRR and Output Noise
The PNP pass transistor regulator is different from the NPN-type regulators. The impedance of the load adds a low frequency first-order load pole ($P_L$) to the Bode Plot of the PNP pass transistor regulator, the frequency of which is given by:

$$f(P_L) = \frac{1}{2\pi R_{\text{LOAD}}C_{\text{OUT}}}$$  \hspace{1cm} \text{(Equation 4)}$$

As one can see from Equation 4, increasing the capacitance of the output capacitor decreases the frequency of the load pole, which effectively lowers the 0dB crossover frequency and decreases the PSRR between the old and new 0dB crossover point. Therefore, one way to improve the PSRR of the PNP pass transistor regulator is to do just the opposite – to actually decrease the capacitance of the output capacitor. However, this does increase the overall output noise (Figure 4).

The same analysis is applicable to the P-channel FET regulator (see Figure 4).
Figure 4. PNP Pass Transistor Regulator & P-Channel FET Regulator PSRR and Output Noise
Output Noise
The output noise of a linear regulator is illustrated by a “noise density” curve that shows the noise density [in the unit of μV/√(Hz)] vs. frequency. On most linear regulator datasheets, an overall output noise, expressed in μVrms or mVrms, is included. The overall output noise is the noise density integrated over a frequency range at which the linear regulator is sensitive.

The output noise of a linear regulator is amplified, self-generated noise, as opposed to the output ripple, which is induced by input disturbances. There are two primary sources of self-generated noise: the resistor divider and the bandgap. Both are inputs to the error amplifier. This means that the output noise is directly related to the open-loop gain of the error amplifier, which is essentially the open-loop gain of the feedback loop. Because of this, the output noise density curve looks very much like the loop gain curve of the Bode Plot developed in Part II of this article series. This is also the reason why the pass element is not a primary source of output noise, because its self-generated noise is not amplified through the feedback loop (see Figure 1).

The resistor divider generates thermal related noise – the so called 4kTR noise, where k is the Boltzmann’s constant, T is the temperature expressed in Kelvin, and R is the impedance of the resistor pair. It is obvious that, in order to reduce this noise, the R1 and R2 need to be small. However, smaller R1 and R2 values make the resistor divider consume more current, which reduces the efficiency of the linear regulator. Design trade-offs need to be made for each application.

One should always use a bandgap with low output noise below its roll-off frequency. Again, there is no universally accepted theory to prove that one processing technology is superior to another for designing low-noise bandgap voltage references. In practice, the output noise of bandgap designs, based upon both bipolar and CMOS technology, are comparable.

Since both the bandgap’s input-induced output ripple and self-generated output noise manifest as output fluctuations with the same bandgap roll-off frequency, the same low-pass filter used to reduce its output ripple (to improve its PSRR) can also be utilized to reduce its output noise. The low-pass filter “bypasses” both the output ripple and output noise to the ground, to prevent them from propagating to the output of the linear regulator, down to its roll-off frequency.

Unfortunately, the similarity between improving the PSRR and reducing the output noise of a linear regulator stops here.

Because the noise density curve behaves like the loop gain curve and the overall output noise is an integral of the noise density over a certain frequency range, it is easy to see that, in order to reduce the overall output noise, it is desirable to have a lower open-loop gain and lower 0dB crossover frequency -- just the opposite to what is required to improve the PSRR!

Because of the standard NPN regulator’s high 0dB crossover frequency, its intrinsic output noise performance is not good. As discussed in the PSRR section of this article, adding an output capacitor lowers the 0dB crossover frequency. As a result, although the added output capacitor does not improve the PSRR below the 0dB crossover frequency, it decreases the output noise below the 0dB crossover frequency, as well as above it. Therefore, if reducing the output noise is critical to the application, an output capacitor should be used (see Figure 2).

For the NPN pass transistor regulator, the intrinsic output noise is lower than that of the standard NPN regulator since its 0dB crossover frequency is not as high. Again, as discussed in the PSRR section of this article, more output capacitance typically decreases the 0dB crossover frequency, which worsens the PSRR but reduces the overall output noise (see Figure 3).

The same conclusion is also applicable to the N-channel FET regulator (see Figure 3).
For the PNP pass transistor regulator, however, the opposite is true. First of all, it has lower 0dB crossover frequency than NPN-type regulators, which gives it low output noise. In addition, as we concluded from Equation 4, increasing the output capacitor decreases the 0dB crossover frequency, resulting in reduced overall output noise (Figure 4).

The same analysis is applicable to the P-channel FET regulator (Figure 4).

**Conclusion**

In a linear regulator, the PSRR and output noise performance of the bandgap voltage reference can be improved by adding a low-pass filter on its output to the error amplifier.

However, changing the capacitance of the output capacitor, which is the most effective way to improve the PSRR and overall output noise performance, produces opposite results for each of these application-oriented parameters. Basically, the higher the output capacitor, the lower the 0dB crossover frequency. A higher 0dB crossover frequency improves the PSRR but increases the overall output noise, and a lower 0dB crossover frequency reduces the overall output noise but decreases the PSRR. Of course, the output capacitor must be sized for the resistive load, so there are limits in changing its capacitance value. Good design trade-offs need to be made on a case-by-case basis at particular frequencies or frequency ranges, based upon application requirements.

Additionally, changing the error amplifier’s gain and unity-gain frequency, as well as changing the intrinsic capacitance of the pass element, also impact PSRR and output noise. These methods are, however, internal to the design of the linear regulator, rather than application-oriented. This places them outside the scope of this article.

**References**


## Linear Regulator PSRR and Output Noise Comparison

<table>
<thead>
<tr>
<th>Regulator Type</th>
<th>Standard NPN (Darlington)</th>
<th>NPN Pass Transistor</th>
<th>PNP Pass Transistor</th>
<th>P-channel FET</th>
<th>N-channel FET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap PSRR</td>
<td>Comparable</td>
<td>Comparable</td>
<td>Comparable</td>
<td>Comparable</td>
<td>Comparable</td>
</tr>
<tr>
<td>Bandgap Noise</td>
<td>Comparable</td>
<td>Comparable</td>
<td>Comparable</td>
<td>Comparable</td>
<td>Comparable</td>
</tr>
<tr>
<td>Method to increase PSRR and reduce output noise for the bandgap</td>
<td>Low-pass filter on bandgap output</td>
<td>Low-pass filter on bandgap output</td>
<td>Low-pass filter on bandgap output</td>
<td>Low-pass filter on bandgap output</td>
<td>Low-pass filter on bandgap output</td>
</tr>
<tr>
<td>Intrinsic PSRR without bandgap (over frequency range)</td>
<td>High</td>
<td>Somewhat high</td>
<td>Fair</td>
<td>Fair</td>
<td>Somewhat high</td>
</tr>
<tr>
<td>Method to increase overall PSRR (minus bandgap)</td>
<td>Internal</td>
<td>Decrease the capacitance of the output capacitor</td>
<td>Decrease the capacitance of the output capacitor</td>
<td>Decrease the capacitance of the output capacitor</td>
<td>Decrease the capacitance of the output capacitor</td>
</tr>
<tr>
<td>Intrinsic Output Noise without bandgap (over frequency range)</td>
<td>High</td>
<td>Somewhat high</td>
<td>Fair</td>
<td>Fair</td>
<td>Somewhat high</td>
</tr>
<tr>
<td>Method to reduce overall output Noise (minus bandgap)</td>
<td>Add output capacitor</td>
<td>Increase the capacitance of the output capacitor</td>
<td>Increase the capacitance of the output capacitor</td>
<td>Increase the capacitance of the output capacitor</td>
<td>Increase the capacitance of the output capacitor</td>
</tr>
</tbody>
</table>