Features

- **Packet Network Frequency and Phase Sync**
  - Frequency accuracy for GSM, WCDMA-FDD, LTE-FDD basestations and small cells
  - Frequency performance for ITU-T G.823 and G.824 synchronization interface, G.8261 PNT PEC and CES interfaces and G.8263 PEC-S-F
  - Phase synchronization performance for WCDMA-TDD, TD-SCDMA, CDMA2000, LTE-TDD and LTE-A applications
  - Client holdover and reference switching between multiple servers
  - Support for new ITU-T packet clock drafts or recs: G.8263 PEC, G.8273.2 T-BC & T-TSC w/o SyncE, and G.8273.4 T-BC-P & T-TSC-P
  - Hybrid mode for mixing SyncE and IEEEl588

- **Physical Layer Clock Synchronization**
  - ITU-T G.8262 SyncE EEC options 1 and 2

- **Low-Bandwidth DPLL**
  - Low-jitter operation from any \( \geq 10 \text{MHz} \) TCXO
  - Master clock jitter attenuator reduces cost by removing TCXO/OCXO low-jitter requirement
  - Hitless reference switching
  - High-resolution holdover averaging
  - Numerically controlled oscillator mode

- **Input Clocks**
  - Up to 3 inputs, 2 differential/CMOS, one CMOS
  - Any input frequency from 8kHz to 1250MHz (8kHz to 300MHz for CMOS)
  - Per-input activity and frequency monitoring

- **Low-Jitter Fractional-N APLL and 3 Outputs**
  - Any output frequency from \(< 1 \text{Hz} \) to 1035MHz
  - High-resolution fractional frequency conversion with 0ppm error
  - Encapsulated design requires no external VCXO or loop filter components
  - Output jitter as low as 0.25ps RMS (12kHz-20MHz integration band)
  - Outputs are CML or 2xCMOS, can interface to LVDS, LVPECL, HSTL, SSTL and HCSL
  - Per-output supply pin with CMOS output voltages from 1.5V to 3.3V
  - Precise output alignment circuitry and per-output phase adjustment
  - Per-output enable/disable and glitchless start/stop (stop high or low)

- **General Features**
  - Automatic self-configuration at power-up from internal EEPROM; up to four configurations
  - Input-to-output alignment with external feedback
  - SPI or I2C processor Interface
  - Easy-to-use evaluation software

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**Figure 1 - Functional Block Diagram**

**Ordering Information**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Pin Count</th>
<th>Package</th>
<th>Lead Finish</th>
<th>Temp Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZL30721LFG7</td>
<td>64</td>
<td>LGA</td>
<td>Ni Au</td>
<td>-40°C to +85°C</td>
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<tr>
<td>ZL30721LFF7</td>
<td>64</td>
<td>LGA</td>
<td>Ni Au</td>
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</tbody>
</table>
1. Application Examples

From line cards and other clock sources

<table>
<thead>
<tr>
<th>ZL30721</th>
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</thead>
<tbody>
<tr>
<td>TCXO or OCXO</td>
</tr>
</tbody>
</table>

2x 156.25MHz differential
125MHz CMOS
25MHz CMOS

G.813/G.8262 compliance, input clock monitoring, hitless switching, frequency conversion.

Output jitter dependent on xtal or XO, not on TCXO or OCXO, which reduces TCXO/OCXO cost.

Figure 2 – Telecom Timing Card Application, TCXO + Crystal/XO for Lowest Jitter

From line cards and other clock sources

<table>
<thead>
<tr>
<th>ZL30721</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCXO or OCXO</td>
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</table>

2x 156.25MHz differential
125MHz CMOS
25MHz CMOS

G.813/G.8262 compliance, input clock monitoring, hitless switching, frequency conversion.

Output jitter dependent on TCXO or OCXO jitter.

Figure 3 – Telecom Timing Card Application, TCXO Only

2. Detailed Features

2.1 Time Synchronization Algorithm

- External algorithm controls software digital PLL to adjust frequency and phase alignment
- Frequency, phase and time synchronization over IP, MPLS and Ethernet packet networks
- Frequency accuracy performance for GSM, WCDMA-FDD, LTE-FDD femtocell, small cell (residential, urban, rural, enterprise), picocell and macrocell applications, with target performance less than ±15 ppb
- Frequency performance for ITU-T G.8263 for PEC-S-F (Packet Equipment Clock - Slave - Frequency)
- Frequency performance for ITU-T G.823 and G.824 synchronization interface, as well as G.8261 PNT EEC, PNT PEC and CES interface specifications
- Phase synchronization performance for WCDMA-TDD, Mobile WiMAX, TD-SCDMA, CDMA2000, LTE-TDD and LTE-A femtocell, small cell (residential, urban, rural, enterprise), picocell and macrocell applications with target performance less than ± 1µs phase alignment.
- Phase performance for ITU-T packet clock drafts or recommendations in development
  - ITU-T G.8273.2 T-BC & T-TSC, when not using SyncE input
  - ITU-T G.8273.4 T-BC-P & T-TSC-P
- Supports hybrid mode for mixing SyncE and IEEE1588 inputs
- Time Synchronization for TAI, UTC-traceability and GNSS/GPS replacement.
- Client reference switching between multiple servers
- Client holdover when server packet connectivity is lost
- Client synchronization to best server with monitoring of secondary server references

2.2 Master Clock Jitter Attenuator and Multiplier

- Enables the DPLL to operate from any TCXO or OCXO ≥ 10MHz regardless of jitter
- When a low-cost crystal or XO is used, output jitter depends on crystal/XO, not on TCXO/OCXO jitter
- Reduces cost by removing tight jitter requirement from TCXO or OCXO

2.3 Input Block Features

- Up to three input clocks, two differential or single-ended, one single-ended
- Input clocks can be any frequency from 8kHz up to 1250MHz (differential) or 300MHz (single-ended)
Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN, wireless
Inputs constantly monitored by programmable activity monitors and frequency monitors
Fast activity monitor can disqualify the selected reference after a few missing clock cycles
Frequency measurement and monitoring with 1ppm resolution and accept/reject hysteresis
Optional input clock invalidation on GPIO assertion to react to LOS signals from PHYs

2.4 Electrical Clock Engine Features
- Very high-resolution DPLL architecture
- State machine automatically transitions between tracking and freerun/holdover states
- Revertive or nonrevertive reference selection algorithm
- Programmable bandwidth from 0.1Hz to 10Hz
- Less than 0.1dB gain peaking
- Programmable phase-slope limiting
- Programmable tracking range (i.e. hold-in range)
- Truly hitless reference switching with <200ps output clock phase transient
  - Physical-clock-to-physical-clock reference switching
  - Physical-clock-to-packet-timing reference switching
  - Packet-timing-to-physical-clock reference switching
  - Packet-timing-to-packet-timing reference switching
- Support for SyncE and SONET/SDH equipment clock specifications
  - ITU-T G.8262 option 1 EEC
  - ITU-T G.8262 option 2 EEC
  - ITU-T G.813 option 1 SEC
  - ITU-T G.813 option 2 SEC
- Output phase adjustment in 10ps steps
- High-resolution frequency and phase measurement
- Fast detection of input clock failure and transition to holdover mode
- Holdover frequency averaging with programmable averaging time and delay time

2.5 APLL Features
- Very high-resolution fractional scaling (i.e. non-integer multiplication)
- Any-to-any frequency conversion with 0ppm error
- Two high-speed dividers (integers 4 to 15, half divides 4.5 to 7.5)
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter components

2.6 Output Clock Features
- Three low-jitter output clocks
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 1Hz to 1035MHz (250MHz max for CMOS and HSTL outputs)
- Output jitter as low as 0.25ps RMS (12kHz to 20MHz)
- In CMOS mode, an additional divider allows the OCxn pin to be an integer divisor of the OCxp pin
  (Example 1: OC3P 125MHz, OC3N 25MHz. Example 2: OC2P 25MHz, OC2N 1Hz)
- Outputs easily interface with CML, LVDS, LVPECL, HSTL, SSTL, HCSL and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Sophisticated output-to-output phase alignment
- Per-output phase adjustment with high resolution and unlimited range
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

2.7 General Features
- SPI or I²C serial microprocessor interface
- Automatic self-configuration at power-up from internal EEPROM memory; pin control to specify one of four stored configurations
- Numerically controlled oscillator (NCO) mode allows system software to steer DPLL frequency with resolution better than 0.01ppb
• Input-to-output alignment with external feedback
• Up to eight general-purpose I/O pins each with many possible status and control options
• Output frame sync signals: 2kHz or 8kHz (SONET/SDH), 1Hz (IEEE 1588) or other frequency
• Internal compensation for local oscillator frequency error

2.8 API Software
• Interfaces to 1588-capable PHYs and switches with integrated timestamping
• Abstraction layer for independence from OS and CPU, from embedded SoC to home-grown
• Fits into centralized, highly integrated “pizza box” architectures as well as distributed architectures with multiple line cards and timing cards

3. Applications
• ITU-T G.8262 system timing cards for Synchronous Ethernet systems
• System timing cards which support ITU-T G.781 SETS (SDH Equipment Timing Source)
• Integrated base station reference synchronization for air interfaces for
  o GSM, WCDMA, TD-SCDMA, LTE and LTE-A
  o FDD or TDD mobile technology
  o Femtocells, small cells (residential, urban, rural, enterprise), picocells and macrocells
• Mobile Backhaul NID, cell-site router, edge switch/router, microwave or access aggregation node
• EPON/GPON OLT and ONU/ONT
• DSLAM and RT-DSLAM
• 10G, 40G and 100G line cards
• SONET/SDH, Fibre Channel, XAUI

4. Pin Diagram
The device is packaged in a 5x10mm 64-pin LGA.
5. Mechanical Drawing

### SYMBOL

<table>
<thead>
<tr>
<th>DIMENSION</th>
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<th>TYP</th>
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<td>REF</td>
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<td>SUBSTRATE THICKNESS</td>
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<td>REF</td>
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<tr>
<td>MOLD THICKNESS</td>
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<td>REF</td>
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<tr>
<td>BODY SIZE</td>
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<tr>
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<tr>
<td>LEAD LENGTH</td>
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<tr>
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<td>LEAD COUNT</td>
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<td>EDGE LEAD CENTER TO CENTER</td>
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<td>BODY CENTER TO LEAD</td>
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<tr>
<td>COPLANARITY</td>
<td>ddd</td>
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Dimensions in mm.
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