Mentor Graphics and SMSC
USB 2.0 Reference Design

Product Features

- High speed operation, up to 480Mbits per sec
- Inventra MUSBHSFC, USB 2.0 function controller
  - 16-bit VCI interface to microcontroller
  - 8-bit UTMI interface to USB transceiver
  - 2 Bulk Endpoints with 1024byte synchronous FIFOs
  - Firmware included
- SMSC Technology GT3200 USB 2.0 Transceiver
  - USB-IF "Hi-Speed" Fully Certified to USB 2.0 Specification
  - Typical Current Consumption of 60mA in HS Mode - Ideal for Bus Powered Functions
  - Interface Compliant with the UTMI Specification (60MHz 8-bit Unidirectional Interface and 30MHz 16-bit Bidirectional Interface)
  - Integrated 1.5kΩ DP pull-up resistor and 45Ω termination resistors save 3 external components
  - 5.25V short circuit protection of DP & DM lines
  - Available in a 64-Pin TQFP
- Inventra M8051EW Microcontroller
  - 2 clocks per cycle, running at 16MHz
  - 16-bit asynchronous interface to SCSI bus
  - 64K bytes external program memory (<15K used)
  - 64K bytes external data memory
  - On-Chip debug with JTAG interface
- FPGA Implementation
  - Xilinx Virtex FPGA
  - 60MHz Operating Frequency
  - Density up to 56K system gates
  - Block RAM up to 20Kbytes
  - Reprogrammable

This application overview describes a USB 2.0 Transfer System board, which provides a reference design for applications that use the USB 2.0 Universal Serial Bus.

The board comprises a Mentor Graphics® Inventra™ USB 2.0-compliant function controller, 8051-compatible microcontroller and DMA controller implemented in a single Xilinx® Virtex™ FPGA, together with the SMSC Technology™ GT3200 Hi-Speed USB Transceiver.

It provides an interface for high-speed data transfer between a PC and a SCSI disk drive.
Figure 1 - USB 2.0 Reference Design System Architecture
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**System Overview**

The figure below shows the board block diagram.

The principal constituents of the board are a USB 2.0 function controller and a 8051 microcontroller. These two devices are provided by reusable and configurable soft cores from the Mentor Graphics Inventra Intellectual Property (IP) catalog, implemented in a single Xilinx Virtex FPGA. The USB 2.0 function controller is provided by the Inventra MUSBHSFC soft core; the 8051 microcontroller is provided by the Inventra M8051EW soft core.

The other main component of the board is the GT3200 USB 2.0 Transceiver from SMSC which provides the connection between the USB serial bus and the UTMI bus for both high-speed and full-speed operation.

The MUSBHSFC uses an internal 60MHz clock and the data transfer to the transceiver is executed over a uni-directional 8-bit bus. The bus on the USB 2.0 transceiver side is UTMI compliant; the bus on the microcontroller side is VCI compliant.

![USB 2.0 Reference Design Block Diagram](image)

**Figure 2 - USB 2.0 Reference Design Block Diagram**

**USB Device Software**

The software controlling the USB device implements Universal Serial Bus Mass Storage Class, Bulk-Only Transport (Specification Revision 1.0).

The device code occupies less than 15K of program memory. It also uses a DMA controller to transfer data directly between the SCSI interface and the VCI interface, using wide SCSI data transfers. This helps sustain the high-bandwidth data transfers supported by USB 2.0.
The USB 2.0 Function Controller

The MUSBHSFC core provides a USB function controller that complies with the USB 2.0 specification for high/full-speed (480/12 Mbits/s) functions. It is user-configurable for up to 15 IN endpoints and up to 15 OUT endpoints in addition to Endpoint 0. These additional endpoints can be individually programmed for Bulk/Interrupt or Isochronous transfers.

FIFOs for the endpoints are provided by a single block of synchronous single-port RAM, added by the user. The size of the FIFO for Endpoint 0 is fixed at 64 bytes and can buffer 1 packet. The other endpoint FIFOs may be from 8 to 8192 bytes in size and can buffer either 1 or 2 packets. Separate FIFOs may be associated with each endpoint: alternatively an IN endpoint and the OUT endpoint with the same Endpoint number can be configured to use the same FIFO, for example to reduce the size of RAM block needed.

The MUSBHSFC provides a USB 2.0 Transceiver Macrocell Interface (UTMI Specification version 1.05) to connect to an 8/16-bit high/full-speed transceiver. The design also features a 16/32-bit VCI-compatible interface to connect to a processor bus. Access to the FIFOs and the internal control/status registers is via the 16/32-bit VCI-compatible interface. The device also offers DMA access to the Endpoint FIFOs.

The MUSBHSFC provides all the USB packet encoding, decoding, checking and handshaking – interrupting the CPU only when endpoint data has been successfully transferred.

A graphical user interface script is provided for configuring the core to the user’s requirements.

Figure 3 - The Mentor Graphics Inventra MUSBHSFC
The USB 2.0 Transceiver

Designed specifically to address the need for high performance, low-power USB systems, SMSC’s GT3200 discrete PHY IC provides best-in-class power dissipation. It is the leading solution available today for running high-speed (480 Mbps) systems using only the power provided on the USB bus cable. For peripheral designers targeting applications such as broadband modems, web cameras, and portable digital systems, this capability provides clear market differentiation. In addition, GT3200-based designs allow for extremely cost effective applications, requiring only a small number of low cost external components. The GT3200 supports both 8 and 16-bit UTMI operation and has been tested and USB-IF Hi-Speed certified with USB controllers from a number of third parties.

![The SMSC GT3200](image)

Figure 4 - The SMSC GT3200

8051- Compatible Microcontroller

The Mentor Graphics Inventra M8051EW

The M8051EW offers a complete, high performance 8051 core and development kit.

The M8051EW is the only 8051-compatible soft core to surpass 50Mips performance reliably. It is also the lowest power core available today. Power control mechanisms are built into the state machine, CPU and peripherals.

The M8051EW is also 100% legacy compatible, preserving the user's investment in industry-standard 8051 tool suites. It does not use instruction set extensions and exotic clocking mechanisms that require expert hand-editing of design tools.

The M8051EW can be configured to suit a wide range of user requirements. For example, it can be configured to work with either synchronous or asynchronous memory; it can have separate Program and External Data Memory interfaces or a single multiplexed interface; and it can offer either one, two or eight data pointers and two or four levels of interrupt priority. Wait state support is provided for slow memory devices.
Debug Environment

The M8051EW offers a Debug Mode together with an On-Chip Instrumentation (OCI™) interface. This interface offers a set of dedicated Debug signals, which may be used by external debug hardware to provide a range of debugging facilities.

These facilities are intended to be used in conjunction with the ISA-WARP 8051 In-Target System Analyzer from First Silicon Solutions (FS2).

The OCI™ interface, working in conjunction with in-circuit emulation tools, enables in-situ, at-speed validation of the board application program. The ISA-WARP 8051 In-Target Analyzer provides a PC-based validation platform for the USB 2.0 board.

The debug interface provides a range of debugging features from basic stop/start or single-step execution and breakpoint support to reconstruction of execution history and capture of data memory, program memory and SFR accesses.

A graphical, source level debugger program supplied with the ISA-WARP 8051 provides an easy to use interface. The debugger runs on a PC over a high-speed parallel port.

The ISA-WARP 8051 is contained in a compact chassis that connects to the board using a standard 20 pin AMP debug connector. It requires access to just 6 of the M8051EW’s pins.