In this presentation we will examine the causes and effects of the different kinds of resets that can be used in PICmicro® microcontrollers.

There are several possible events that can cause a reset, and the effect of the reset depends to some degree on what caused the reset.
Resets can be caused by a signal on the MCLR pin, by powering up the device, by a Watchdog timer timeout, by a Brown-Out voltage Reset (BOR), by a software reset instruction, or by a stack overflow or underflow reset.

Not all of these reset mechanisms are available on all devices. For example, the reset instruction and stack resets are only available on Micrchip’s PIC18CXXX family of devices. Please consult the appropriate device datasheet for device-specific information.

We will deal with the causes and effects of each kind of reset individually.
The MCLR pin can be used to generate a reset.

On most PICmicro® devices the MCLR pin is always active. However, on some devices, such as the small 8-pin microcontrollers, the MCLR signal can be internally tied to VDD and the pin can then be used as a general purpose input.

When the MCLR function of the pin is enabled, it is an active low Schmitt trigger input. This means that to insure a reset, the voltage on the pin must be lower than the maximum input low voltage specified in the relevant datasheet in the electrical characteristics section. This is usually 1 volt for operation at 5 volts.

To insure that the device does not get reset unintentionally during normal operation, the voltage on the MCLR pin must be kept higher than the minimum input high voltage specified in the datasheet. This is usually 4 volts for operation at 5 volts. The designer must take care that this specification is met even when noise causes fluctuations in the MCLR and VDD voltages.

In addition to the reset function, MCLR can also be used to place the device in programming mode with a VPP voltage, usually 13V, on the pin. Because the MCLR pin needs to be driven to a high voltage, there is no upper protection diode on this pin, although there is a voltage clamp circuit for protection.

The MCLR pin has no internal pull-up and must not be left unconnected.
Since the MCLR pin is an input, it must be driven by an external circuit of some kind.

This can be as simple as connecting MCLR directly to $V_{DD}$, and in this case, the MCLR pin will not be used to generate a reset. The device must then rely on the Power-On Reset (POR) to provide a reset when it powers up.

An RC circuit can be used to keep the MCLR voltage low for some time after power-on. This can be useful to provide a longer reset if the power supply does not rise fast enough. The $V_{DD}$ rise rate required for proper Power-On Reset is specified in the electrical characteristics section of the data sheet.

A supervisor (reset) chip such as the Microchip MCP100 or MCP809, can be used to generate a reset signal on the MCLR pin. These devices drive their output low when the supply voltage is below a specified level. They can be used to insure that the microcontroller is reset until $V_{DD}$ is at a valid operating voltage. Supervisors are particularly useful for devices that do not have a built in Brown-Out Reset function.

Many circuits have a system reset signal that is used for multiple devices in the system. This type of logic level signal can also be used to provide a signal to MCLR to reset the microcontroller when the rest of the system is reset.
After a device has received an MCLR reset it will start executing code from the reset vector.

When MCLR is brought low, the device will be held in a reset state until MCLR is brought high. During this time the oscillator will run.

If the device was reset from sleep and a crystal oscillator mode is used, then the oscillator startup timer will keep the device reset to give the oscillator time to start up, even if the MCLR signal is only held low for a short period.

When an RC oscillator is used the oscillator will run during reset but the output on the OSC2 pin will be stopped.

An MCLR reset will not change the state of any general purpose RAM locations, but some of the special function registers will be initialized. This applies to most types of reset, and the initialized state of the special function registers are specified in the applicable data sheet.

An MCLR reset will not affect the TO, POR and BOR bits and can be detected by the absence of other reset causes indicated by these bits, if they were set appropriately before the reset.

The PD bit can be used to determine whether an MCLR reset occurred during normal operation or sleep because the PD bit is cleared by execution of the sleep instruction.
All PICmicro® devices have a built-in Power-On Reset circuit. This insures that when the device powers up within specifications, it will be reset and start operation in a properly initialized way. The critical requirements are that the device powers up from zero volts and that the VDD rise rate is fast enough.

On some devices, the Power-On Reset can start a Power-On Reset timer which will hold the device in reset for an extra delay to allow more time for the power to stabilize. This option can be selected in the configuration bits for the device.
After a device has received a Power-On Reset, it will start executing code from the reset vector.

If a crystal oscillator mode is used, then the oscillator startup timer will give the oscillator time to start up after the Power-On Reset. The device will be held in the reset state for an additional delay if the Power-On Reset timer is enabled.

The state of all general purpose RAM locations will be unknown after a Power-On Reset but some of the special function registers will be initialized.

A Power-On Reset will clear the POR bit and set the TO and PD bits. If a brown-out reset was enabled the BOR bit will be unknown.
All PICmicro® devices have a Watchdog timer which gives the code developer a way to reset the device in the event of unexpected code operation. The Watchdog timer must be periodically cleared in software to prevent a reset. If the code fails to clear the Watchdog timer, a reset will occur. It is only effective if used properly. Too many “clear Watchdog timer” instructions can potentially allow the device to get stuck in a loop that clears the Watchdog.

The Watchdog timer can be enabled in the configuration bits for the device when it is programmed. When enabled, it can never be deactivated in software, even during sleep. In the PIC18CXXX family, the Watchdog timer can be disabled in the configuration bits but still be enabled by software. This has a disadvantage -- it can be accidentally disabled, but allows the device to be placed in sleep without the Watchdog timer waking it up.

The Watchdog timer is implemented with a very simple internal RC oscillator. The timeout period can vary greatly from device to device and with voltage and temperature. The user should always design with this variation in mind. There is a postscaler that can be used to generate longer timeout periods.

The Watchdog timer circuit draws additional current when it is enabled, which should be taken into account when designing for low power applications.
Reset - WDT Effects

- Effect of a Watchdog Timer time-out on parts
  - 12 bit core and standard 16 bit core
    - Resets part
  - 14 bit core and enhanced 16 bit core
    - Resets part if part was running
    - Wakes part if part was in sleep

A time-out of the Watchdog timer will cause a reset if the part is running. On devices that are in sleep, the effect of the timeout depends on the device family being used.

Baseline devices such as the PIC16C5X, have a 12-bit core. On these devices a Watchdog timeout causes a reset during sleep. The PIC17CXXX devices have the standard 16-bit core. These devices are also reset by a Watchdog timeout during sleep.

Mid-range devices such as the PIC16C7X, have a 14-bit core and will wake up from sleep and resume normal operation when a Watchdog timeout occurs.

The high-performance PIC18CXXX devices have an enhanced 16-bit core and will also wake from sleep when a timeout occurs.
After a device has received a Watchdog timer reset it will start executing code from the reset vector.

A Watchdog timer reset will not change the state of any general purpose RAM locations, but some of the special function registers will be initialized.

A Watchdog timer reset will clear the TO bit and leave the PD, POR and BOR bits unchanged.
If the device is in SLEEP when a Watchdog timer time-out occurs, it will wake up and continue executing code after the sleep instruction - this is true for all devices except those based on the 12-bit core.

If a crystal oscillator mode is used, the oscillator startup timer will give the oscillator time to start up after the wake-up.

A Watchdog timer wakeup will not change the state of any general purpose RAM locations or special function registers except for the TO and PD bits in the STATUS register.

The PD bit is cleared when the device is put to sleep. A Watchdog timer wakeup will clear the TO bit. The POR and BOR bits remain unchanged.
Many PICmicro® devices have a built-in Brown-Out Reset (BOR) feature that resets the device when the supply voltage drops too low. This is used to insure that the device will not try to run at a voltage that is too low for correct operation. The designer should insure that the device normally operates above the Brown-Out Reset trip point with some margin for error. The Brown-Out Reset is not a substitute for a proper Power-On Reset.

The Brown-Out Reset can be enabled in the configuration bits. Once enabled, it is always active, even during sleep. On some devices, the Brown-Out Reset voltage is fixed, but on others it can be selected from several different voltages.

Usually the Brown-Out Reset can be made to start the power-up reset timer to insure a longer reset time for reliability.

The Brown-Out Reset circuit draws extra current when it is enabled. This should be taken into account when designing for low power applications.
A device will be held in reset by the Brown-Out Reset until the voltage rises back above the trip point. Some devices will be held in reset by the power-up timer for an additional delay, while on other devices this is selectable in configuration bits. After the reset, the device will start executing code from the reset vector.

The state of all general purpose RAM locations will be unknown after a Brown-Out Reset, but some of the special function registers will be initialized. In some cases RAM locations will be unchanged. In cases where the supply voltage drops low enough, the RAM will be corrupted.

A Brown-Out Reset will clear the BOR bit and leave the POR bit unchanged. The TO and PD bits will be set unless the device was in sleep when the brown-out reset occurred. In this case the PD bit will be cleared.
The PIC18CXXX devices have some additional reset capabilities.

A reset instruction allows the device to be reset in software as though a pulse was generated on the MCLR pin.

The stack full reset can be enabled in the configuration bits and causes a reset when the stack becomes full. The STKFUL bit in the STKPTR register will be set to indicate the cause of the reset.

A stack underflow loads the program counter with zero which causes an immediate branch to the reset vector. Although it starts the code executing from the beginning, it does not cause a reset and will not affect any registers except the STKUNF bit in the STKPTR register.
The cause of a reset can be determined by testing bits in several special function registers. Not all devices and device families have all the reset functions implemented.

On most devices, the STATUS and PCON registers contain the relevant bits. On PIC17CXXX devices, these bits are in the CPUSTA register, however, the PIC17C4X devices do not have POR or BOR bits. On PIC18CXXX devices these bits are in the RCON register with additional bits in the STKPTR register.

The POR bit indicates a Power-On Reset. The BOR bit indicates a Brown-Out Reset, although this bit may also be asserted when a Power-On Reset occurs. These bits are active low and must be set in software after the reset to ensure that the next reset can be correctly identified.

The TO bit indicates that a Watchdog time-out occurred and the PD bit indicates that the device was in SLEEP when a reset occurred. These two bits are active low and are read only and do not need to be set in software.

The STKFUL and STKUNF bits indicate whether a stack full reset or a stack underflow occurred.
For further information on Resets, please refer to specific device datasheets.

This concludes a brief examination of the causes and effects of Resets in PICmicro MCUs.

For additional information, please see the datasheet for the specific device being used. Datasheets, Application Notes, Seminar and Workshop schedules, and other helpful information can be found on the Microchip website.