General Description

The MIC5164 is a dual regulator controller designed for high speed bus termination. It offers a simple, low-cost JEDEC-compliant solution for terminating high-speed, low-voltage digital buses (i.e. DDR, DDR2, DDR3, SCSI, GML, SSTL, HSTL, LV-TTL, Rambus, LV-PECL, LV-ECL, etc) with a Power Good (PG) signal.

The MIC5164 controls two external N-Channel MOSFETs to form two separate regulators. It operates by switching between either the high-side MOSFET or the low-side MOSFET depending on whether the current is being sourced to the load or sunk by the regulator.

Designed to provide a universal solution for bus termination regardless of input voltage, output voltage, or load current, the desired MIC5164 output voltage can be programmed by forcing the reference voltage externally to the desired voltage.

The MIC5164 operates from an input of 1.35V to 6V, with a second bias supply input required for operation. It is available in the tiny MSOP-10 package with an operating junction temperature range of −40°C to +125°C.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- Input voltage range: 1.35V to 6V
- Up to 7A V\textsubscript{TT} Current
- Tracking programmable output
- Power Good (PG) signal
- Wide bandwidth
- Logic controlled enable input
- Requires minimal external components
- DDR, DDR2, DDR3, memory termination
- −40°C < T\textsubscript{J} < +125°C
- JEDEC-compliant bus termination for SCSI, GML, SSTL, HSTL, LV-TTL, Rambus, LV-PECL, LV-ECL, etc
- Tiny MSOP-10 package

Applications

- Desktop computers
- Notebook computers
- Communication systems
- Video cards
- DDR/DDR2/DDR3 memory termination

Typical Application

Typical Application

Typical SSTL-2 Application

(Two MOSFETs Support a 3.5A Application)
Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Temperature Range</th>
<th>Package</th>
<th>Lead Finish</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIC5164YMM</td>
<td>-40° to +125°C</td>
<td>10-Pin MSOP</td>
<td>Pb-Free</td>
</tr>
</tbody>
</table>

Note: MSOP is a Green RoHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Pin Configuration

```
VCC  1
EN   2
VDDQ 3
VREF 4
GND  5
FB   6
PG  10
HD  9
LD  8
COMP 7
```

10-Pin MSOP (MM)

Pin Description

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>Bias Supply (Input): Apply 3V-6V to this input for internal bias to the controller.</td>
</tr>
<tr>
<td>2</td>
<td>EN</td>
<td>Enable (Input): CMOS compatible input. Logic high = enable, logic low = shutdown. The EN pin can be tied directly to VDDQ or VCC for functionality. Do not float the EN pin. Floating this pin causes the enable to be in an undetermined state.</td>
</tr>
<tr>
<td>3</td>
<td>VDDQ</td>
<td>Input Supply Voltage.</td>
</tr>
<tr>
<td>4</td>
<td>VREF</td>
<td>Reference voltage equal to half of VDDQ. For internal use only.</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Ground.</td>
</tr>
<tr>
<td>6</td>
<td>FB</td>
<td>Feedback (Input): Input to the internal error amplifier.</td>
</tr>
<tr>
<td>7</td>
<td>COMP</td>
<td>Compensation (Output): Connect a capacitor and resistor from COMP pin to FB pin for compensation of the internal control loop.</td>
</tr>
<tr>
<td>8</td>
<td>LD</td>
<td>Low-side drive (Output): Connects to the Gate of the external low-side MOSFET.</td>
</tr>
<tr>
<td>9</td>
<td>HD</td>
<td>High-side drive (Output): Connects to the Gate of the external high-side MOSFET.</td>
</tr>
<tr>
<td>10</td>
<td>PG</td>
<td>Power Good (Output): Open drain output.</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings\(^{(1)}\)

- **VCC to GND**: \(-0.3\) V to +7 V
- **VDDQ to GND**: \(-0.3\) V to +7 V
- **EN to GND**: \(-0.3\) V to \(V_{CC}\)
- **FB to GND**: \(-0.3\) V to \(V_{CC}\)
- **VREF to GND**: \(-0.3\) V to \(V_{DDQ}\)
- **COMP to GND**: \(-0.3\) V to \(V_{CC}\)
- **HD, LD to GND**: \(-0.3\) V to \(V_{CC}\)
- **PG to GND**: \(-0.3\) V to \(V_{CC}\)

**Lead Temperature (Soldering 10sec.)**: 260°C

**Storage Temperature (TS)**: \(-65\)°C to +150°C

**ESD Rating\(^{(3)}\)** (HBM): +2kV (MM): +300V

Operating Ratings\(^{(2)}\)

- **Supply Voltage (\(V_{CC}\))**: 3V to 6V
- **Supply Voltage (\(V_{DDQ}\))**: 1.35V to 6V
- **Enable Input Voltage (\(V_{EN}\))**: 0V to \(V_{IN}\)
- **Junction Temperature Range (\(T_J\))**: \(-40°C < T_J < +125°C\)
- **Junction Thermal Resistance MSOP-10 (\(\theta_J\))**: 130.5°C/W
- **MSOP-10 (\(\theta_C\))**: 42.6°C/W

Electrical Characteristics\(^{(4)}\)

**Parameter**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VREF Voltage Accuracy</strong></td>
<td>Sourcing; 100mA to 3A</td>
<td>-1%</td>
<td>0.5(V_{DDQ})</td>
<td>+1%</td>
<td>V</td>
</tr>
<tr>
<td><strong>V_{TT} Voltage Accuracy</strong> (Note 5)</td>
<td>Sinking; -100mA to -3A</td>
<td>-10</td>
<td>0.4</td>
<td>+10</td>
<td>mV</td>
</tr>
<tr>
<td><strong>Supply Current ((I_{DDQ}))</strong></td>
<td>(EN = 1.2V) (controller ON) No Load</td>
<td>25</td>
<td>140</td>
<td>200</td>
<td>(\mu A)</td>
</tr>
<tr>
<td><strong>Supply Current ((I_{CC}))</strong></td>
<td>No Load</td>
<td>15</td>
<td>22</td>
<td>27</td>
<td>mA</td>
</tr>
<tr>
<td><strong>(I_{CC}) Shutdown Current</strong> (Note 6)</td>
<td>(EN = 0.2V) (controller OFF); No PG pull-up</td>
<td>0.1</td>
<td>5</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td><strong>Start-Up Time</strong> (Note 7)</td>
<td>(VCC = 5V) external bias; (EN = V_{IN})</td>
<td>8</td>
<td>15</td>
<td>30</td>
<td>(\mu s)</td>
</tr>
</tbody>
</table>

**Enable Input**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Enable Input Threshold</strong></td>
<td>Regulator Enabled</td>
<td>1.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Regulator Shutdown</td>
<td>0.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Enable Hysteresis</strong></td>
<td></td>
<td>50</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>EN Pin Input Current</strong></td>
<td>(V_{IL} &lt; 0.2V) (controller shutdown)</td>
<td>0.01</td>
<td>(\mu A)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(V_{IH} &gt; 1.2V) (controller enable)</td>
<td>5.75</td>
<td>(\mu A)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Power Good Output**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Good Window</strong></td>
<td>Threshold, (\pm)% of (V_{TT}) from Nominal</td>
<td>(\pm 5)</td>
<td>(\pm 10)</td>
<td>(\pm 15)</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td>2</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Power Good Output Low Voltage</strong></td>
<td>(I_{PG} = 2mA) (sinking)</td>
<td>100</td>
<td>300</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td><strong>Power Good Leakage Current</strong></td>
<td>(PG = EN = 5V), (FB = VREF); Switch Leakage Current to Ground</td>
<td>0.01</td>
<td>1.0</td>
<td>(\mu A)</td>
<td></td>
</tr>
<tr>
<td><strong>Power Good Startup Delay Time</strong> (Note 8)</td>
<td></td>
<td>1</td>
<td>2.4</td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

\(T_A = 25°C = VDDQ = 1.5V; VCC = EN = 5V\), **bold** values indicate \(-40°C \leq T_J \leq +125°C\), unless otherwise specified. See test circuit 1 for test circuit configuration.
Electrical Characteristics\(^{(4)}\) (Continued)

\(T_A = 25^\circ C = VDDQ = 1.5V; VCC = 5V, V_{EN} = V_{CC}\), **bold** values indicate \(-40^\circ C \leq T_J \leq +125^\circ C\), unless otherwise specified. See test circuit 1 for test circuit configuration.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Good Output</td>
<td>Time after (V_{FB}) voltage has gone outside of PG window</td>
<td>5</td>
<td>10</td>
<td></td>
<td>(\mu s)</td>
</tr>
</tbody>
</table>

**Driver**

| High-Side Gate Drive Voltage  | High-Side MOSFET Fully ON                                                 | 4.8  | 4.97 |      | V     |
|                               | High-Side MOSFET Fully OFF                                                | 0.03 | 0.2  |      | V     |

| Low-Side Gate Drive Voltage   | Low-Side MOSFET Fully ON                                                 | 4.8  | 4.97 |      | V     |
|                               | Low-Side MOSFET Fully OFF                                                 | 0.03 | 0.2  |      | V     |

**Notes:**

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model 1.5\(k\Omega\) in series with 100\(pF\).
4. Specification for packaged product only.
5. The \(V_{TT}\) voltage accuracy is measured as a delta voltage from the reference output (\(V_{TT} - V_{REF}\)).
6. Shutdown current is measured only on the VCC pin. The VDDQ pin will always draw a minimum amount of current when voltage is applied.
7. Start-up time is defined as the amount of time from \(EN = V_{CC}\) to \(V_{HD} = 90\%\) of \(V_{CC}\).
8. Power Good startup delay is defined as the amount of time from \(EN = V_{CC}\) and \(V_{FB}\) is within \(\pm10\%\) of \(\frac{1}{2}V_{DDQ}\) to \(V_{PG} = 90\%\) of \(V_{CC}\) (\(V_{FB} = V_{REF}\)), during startup (\(V_{FB}\) is the sense of \(V_{TT}\)).
9. Power Good deglitch is defined as the amount of time from the voltage at \(FB\) node going out of PG window (with 10mV overdrive voltage) to \(PG = LOW\).
Test Circuit

Figure 1. Test Circuit
Typical Characteristics

- $V_{TH} - V_{REF}$ vs. Output Current
- $V_{TH} - V_{REF}$ vs. Temperature
- $V_{TH} - V_{REF}$ vs. Temperature
- $I_{cc}$ Current vs. $V_{cc}$
- $I_{cc}$ Current vs. Temperature

Micrel, Inc.

June 2010
Functional Diagram

Figure 2. MIC5164 Block Diagram
**Functional Description**

The MIC5164 is a high-performance linear controller, utilizing scalable N-Channel MOSFETs to provide JEDEC-compliant bus termination. Termination is achieved by dividing down the V_{DDQ} voltage half, providing the reference (V_{REF}) voltage. The MIC5164 controls two external N-Channel MOSFETs to form two separate regulators. It operates by switching between either the high-side MOSFET or the low-side MOSFET, depending on whether the current is being sourced to the load or being sunk by the regulator.

**VDDQ**
The VDDQ pin on the MIC5164 provides the source current through the high side N-Channel and the reference voltage to the device. The MIC5164 can operate at V_{DDQ} input voltages as low as 1.35V. A bypass capacitance will increase performance by improving the source impedance at higher frequencies.

**VREF**
Two resistors divide down the V_{DDQ} voltage to provide V_{REF}. The resistors are valued at around 21kΩ. A minimum capacitor value of 120pF from V_{REF} to ground is mandatory.

**VCC**
VCC supplies the internal circuitry of the MIC5164 and provides the voltage to drive the external N-Channel MOSFETs. A small 1µF ceramic capacitor is recommended for bypassing the VCC pin.

**FB and COMP**
The feedback (FB) pin provides the path for the error amplifier to regulate V_T. A feedback resistor is recommended and resistor values should not exceed 10kΩ. The compensation capacitors should not be less than 40pF.

**EN**
The MIC5164 features an active-high enable (EN) input. In the off-mode state, leakage currents are reduced to microamperes. EN has thresholds compatible with TTL/CMOS for simple logic interfacing.

**PG**
The MIC5164 features a Power Good (PG) output. PG is an open-drain output with an active-high signal. PG requires a pull-up resistor to VCC.
Application Information

High-performance memory requires high-speed signaling. This requires special attention to maintain signal integrity. Bus termination provides a means to increase signaling speed while maintaining good signal integrity. An example of bus termination is the Series Stub Termination Logic or SSTL. Figure 2 is an example of an SSTL 2 single-ended series parallel terminated output. SSTL 2 is a JEDEC signaling standard operating off a 2.5V supply. It consists of a series resistor (R_s) and a terminating resistor (R_T). Values of R_s range between 10Ω to 30Ω with a typical of 22Ω, while R_T ranges from 22Ω to 28Ω with a typical value of 25Ω. V_REF must maintain 1/2 VDD with a ±1% tolerance, while V_TT will dynamically sink and source current to maintain a termination voltage of ±40mV from the VREF line under all conditions. This method of bus termination reduces common mode noise, settling time, voltage swings, EMI/RFI and improves slew rates.

The MIC5165 provides two drive signals, the high-side MOSFET acts as a pass element to provide output voltage and low side MOSFET acts as pull-down to regulate the output termination voltage (V_TT). An internal error amplifier compares the termination voltage (V_TT) and V_REF, controlling two external N-Channel MOSFETs to sink and source current to maintain a termination voltage (V_TT) equal to V_REF. The N-Channels receive their enhancement voltage from a separate VCC pin on the device.

Although the general discussion is focused on SSTL, the MIC5164 is also capable of providing bus terminations for SCSI, GTL, HSTL, LV-TTL, Rambus, LV-PECL, DDR, DDR2, DDR3 memory termination and other systems.

VDDQ

The VDDQ pin on the MIC5164 provides the source current through the high-side N-Channel and the reference voltage to the device. The MIC5164 can operate at V_DDO voltages as low as 1.35V. Due to the possibility of large transient currents being sourced from this line, significant bypass capacitance will aid in performance by improving the source impedance at higher frequencies. Since the reference is simply V_DDO/2, perturbations on V_DDO will also appear at half the amplitude on the reference. For this reason, low-ESR capacitors such as ceramics or OS-CON are recommended on V_DDO.

V_TT

V_TT is the actual termination point. V_TT is regulated to V_REF. Due to high speed signaling, the load current seen by V_TT is constantly changing. To maintain adequate large signal transient response, large OS-CON and ceramics are recommended on V_TT. The proper combination and placement of the OS-CON and ceramic capacitors is important to reduce both ESR and ESL such that high-current and high-speed transients do not exceed the dynamic voltage tolerance requirement of V_TT. The larger OS-CON capacitors provide bulk charge storage while the smaller ceramic capacitors provide current during the fast edges of the bus transition. Using several smaller ceramic capacitors distributed near the termination resistors is typically important to reduce the effects of PCB trace inductance.

VREF

A minimum capacitor value of 120pF from VREF to ground is required to remove high-frequency signals reflected from the source (Refer to Figure 4). Large capacitance values (>1500pF) should be avoided. Values greater than 1500pF slow down V_REF and detract from the reference voltage’s ability to track V_DDO during high-speed load transients.
VREF can also be manipulated for different applications. A separate voltage source can be used to externally set the reference point, bypassing the divider network. Also, external resistors can be added from VREF-to-VDDQ or VREF-to-ground to shift the reference point up or down.

**VCC**

The VCC voltage range is from 3V to 6V, but the minimum voltage on the VCC pin should consider the Gate-to-Source voltage of the MOSFET and VTT voltage. For example, on an SSTL compliant terminator, VDDQ equals 2.5V and VTT equals 1.25V. If the N-Channel MOSFET selected requires a gate source voltage of 2.5V, VCC should be a minimum of 3.75V.

\[ V_{CC_{min}} = V_{TT} + V_{GS} \]

**Feedback and Compensation**

The feedback (FB) pin is connected to VTT for regulation. An external resistor must be placed between FB and VTT. This allows the error amplifier to be correctly externally compensated. For most applications, a 510Ω resistor is recommended.

The COMP pin on the MIC5164 is the output of the internal error amplifier. By placing a capacitor and resistor between the COMP pin and the FB pin, this coupled with the feedback resistor, places an external pole and zero on the error amplifier. With a 510Ω FB resistor, a minimum 220pF capacitor is recommended for a 3A peak termination circuit. An increase in the load will require additional N-Channel MOSFETs and/or increase in output capacitance may require feedback and/or compensation capacitor values to be changed to maintain stability.

**Enable**

EN can be tied directly to VDDQ or VCC for functionality. Do not float the EN pin. Floating this pin causes the enable circuitry to be in an undetermined state.

**Power Good**

PG signal output remains high as long as output is within ±10% range of regulated VTT and goes low if output moves beyond this range.

**Input Capacitance**

The MIC5164 application operates in the linear region during the steady state condition, so there are no switching current pulses from the input capacitor. The application does not require a bulk input capacitor, but using one greatly improves device performance during fast load transients. Since output voltage VTT follows the input voltage VDDQ, attention should be given to possible voltage dips on VDDQ pin. Capacitors with low ESR such as OS-CON and ceramics are recommended for bypassing the input. Although a 100μF ceramic capacitor will suffice for most applications, input capacitance may need to be increased in cases where the termination circuit is greater than 1-inch away from the bulk capacitance.

**Output Capacitance**

Large, low-ESR capacitors are recommended for the output (VTT) of the MIC5164. Although low-ESR capacitors are not required for stability, they are recommended to reduce the effects of high-speed current transients on VTT. The change in voltage during the transient condition will be the effect of the peak current multiplied by the output capacitor’s ESR. For that reason, OS-CON type capacitors are excellent for this application. They have extremely low ESR and large capacitance-to-size ratio. Ceramic capacitors are also well suited to termination due to their low ESR. These capacitors should have a dielectric rating of X5R or X7R. Y5V and Z5U type capacitors are not recommended, due to their poor performance at high frequencies and over temperature. The minimum recommended capacitance for a 3A peak circuit is 100μF. Output capacitance can be increased to achieve greater transient performance.

**MOSFET Selection**

The MIC5164 utilizes external N-Channel MOSFETs to sink and source current. MOSFET selection will be determined by two main characteristics: size and gate threshold (Vgs).

**MOSFET Power Requirements**

One of the most important factors to determine is the amount of power the MOSFET required to dissipate.
Power dissipation in an SSTL circuit will be identical for both the high-side and low-side MOSFETs. Since the supply voltage is divided by half to supply $V_{TT}$, both MOSFETs have the same voltage dropped across them. They are also required to be able to sink and source the same amount of current (for either all 0's or all 1's). This equates to each side being able to dissipate the same amount of power. Power dissipation calculation for the high-side driver is as follows:

$$P_D = (V_{DDQ} - V_{TT}) \times I_{\text{SOURCE}}$$

where $I_{\text{SOURCE}}$ is the average source current. Power dissipation for the low-side MOSFET is as follows:

$$P_D = V_{TT} \times I_{\text{SINK}}$$

where $I_{\text{SINK}}$ is the average sink current.

In a typical 3A peak SSTL_2 circuit, power considerations for MOSFET selection would occur as follows:

$$P_D = (V_{DDQ} - V_{TT}) \times I_{\text{SOURCE}}$$
$$P_D = (2.5V - 1.25V) \times 1.6A$$
$$P_D = 2W$$

This typical SSTL_2 application would require the high-side and low-side N-Channel MOSFETs to be able to handle 2 Watts each. In higher current applications, multiple N-Channel MOSFETs may be placed in parallel to spread the power dissipation. These MOSFETs will share current, distributing power dissipation across each device.

The maximum MOSFET die (junction) temperature limits maximum power dissipation. The ability of the device to dissipate heat away from the junction is specified by the junction-to-ambient ($\theta_{JA}$) thermal resistance.

This is the sum of junction-to-case ($\theta_{JC}$) thermal resistance, case-to-sink ($\theta_{CS}$) thermal resistance and sink-to-ambient ($\theta_{SA}$) thermal resistance:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

In our example of a 3A peak SSTL_2 termination circuit, we have selected a D-pack N-Channel MOSFET that has a maximum junction temperature of 125°C. The device has a junction-to-case thermal resistance of 1.5°C/Watt. Our application has a maximum ambient temperature of 60°C. The required junction-to-ambient thermal resistance can be calculated as follows:

$$\theta_{JA} = \frac{T_J - T_A}{P_D}$$

Where $T_J$ is the maximum junction temperature, $T_A$ is the maximum ambient temperature and $P_D$ is the power dissipation.

In our example:

$$\theta_{JA} = \frac{125°C - 60°C}{2W}$$
$$\theta_{JA} = 32.5°C/W$$

This shows that our total thermal resistance must be better than 32.5°C/W. Since the total thermal resistance is a combination of all the individual thermal resistances, the amount of heat sink required can be calculated as follows:

$$\theta_{SA} = \theta_{JA} - (\theta_{JC} + \theta_{CS})$$

In our example:

$$\theta_{SA} = 32.5°C/W - (1.5°C/W + 0.5°C/W)$$
$$\theta_{SA} = 30.5°C/W$$

In most cases, case-to-sink thermal resistance can be assumed to be about 0.5°C/W.

The SSTL termination circuit for our example, using two D-pack N-Channel MOSFETs (one high-side and one low-side) will require enough copper area to spread the heat from the MOSFET. In this example to dissipate 2W from TO-252 package a 2 oz copper of 1.0 in² on component side is required. In some cases, airflow may also help to reduce thermal resistance. For different MOSFET package refer to manufacturer Data Sheet for copper area requirements.
**MOSFET Gate Threshold**

N-Channel MOSFETs require an enhancement voltage greater than its source voltage. Typical N-Channel MOSFETs have a gate-source threshold ($V_{GS}$) of 1.8V or higher. Since the source of the high side N-Channel MOSFET is connected to $V_{TT}$, the MIC5164 VCC pin requires a voltage greater than the $V_{GS}$ voltage. For example, our SSTL_2 termination circuit has a $V_{TT}$ voltage of 1.25V. For N-Channel MOSFET that has a $V_{GS}$ rating of 2.5V, the VCC voltage can be as min as 3.75V. For N-Channel MOSFET that has a 4.5V $V_{GS}$, the minimum VCC required is 5.75V. It is recommended that the VCC voltage has enough margin to be able to fully enhance the MOSFETs for large signal transient response. In addition, low gate thresholds MOSFETs are recommended to reduce the VCC requirements.

![Figure 5. DDR2 Termination (Four MOSFETs Support Up To 7A)](image5)

![Figure 6. SSTL-2 Application (Two MOSFETs Support Up To 3.5A)](image6)
Functional Characteristics
Ripple Measurements

To properly measure ripple on either input or output of a switching regulator, a proper ring in tip measurement is required. Standard oscilloscope probes come with a grounding clip, or a long wire with an alligator clip. Unfortunately, for high-frequency measurements, this ground clip can pick up high-frequency noise and erroneously inject it into the measured output ripple.

By maintaining the shortest possible ground lengths on the oscilloscope probe, true ripple measurements can be obtained. This requires the removing of the oscilloscope probe sheath and ground clip from a standard oscilloscope probe and wrapping a non-shielded bus wire around the oscilloscope probe. If there does not happen to be any non-shielded bus wire immediately available, the leads from axial resistors will work.

Figure 7. Low-Noise Measurement
PCB Layout Guideline

Warning!!! To minimize EMI and output noise, follow these layout recommendations.

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC5164 controller application:

IC and MOSFET
- Place the IC close to the point of load (POL).
- The trace connecting controller drive pins to MOSFETs gates should be short and wide to avoid oscillations. These oscillations are the result of tank circuit formed by trace inductance and gate capacitance.
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

Input Capacitor
- Place the input capacitor next.
- Place the input capacitors on the same side of the board and as close to the MOSFET and IC as possible.
- Place a ceramic bypass capacitor next to MOSFET.
- Keep both the VDDQ and GND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal, but not between the input capacitors and MOSFET.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

Output Capacitor
- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high-current load trace can degrade the DC load regulation.
Design Example

MIC5164 as a DDR3 Memory Termination Device for 3.5A Application (VDDQ and MOSFET Input Separated)
## Bill of Materials

<table>
<thead>
<tr>
<th>Item</th>
<th>Part Number</th>
<th>Manufacturer</th>
<th>Description</th>
<th>Qty.</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C2, C3, C4</td>
<td>GRM21BR60J226ME39L</td>
<td>Murata</td>
<td>22µF, 6.3V, Ceramic capacitor, X5R, 0805</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>C2012X5R0J226M</td>
<td>TDK</td>
<td>22µF, 6.3V, Ceramic capacitor, X5R, 0805</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>08056D226MAT2A</td>
<td>AVX</td>
<td>22µF, 6.3V, Ceramic capacitor, X5R, 0805</td>
<td>1</td>
</tr>
<tr>
<td>C5</td>
<td>GRM188R60J106ME47D</td>
<td>Murata</td>
<td>10µF, 6.3V, Ceramic capacitor, X5R, 0603</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>C1608X5R0J106M</td>
<td>TDK</td>
<td>10µF, 6.3V, Ceramic capacitor, X5R, 0603</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>06036D106MAT2A</td>
<td>AVX</td>
<td>10µF, 6.3V, Ceramic capacitor, X5R, 0603</td>
<td>1</td>
</tr>
<tr>
<td>C6</td>
<td>GRM1885CJH390JA01D</td>
<td>Murata</td>
<td>39pF, 50V, Ceramic capacitor, NPO, 0603</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>C1608C0G1H390J</td>
<td>TDK</td>
<td>39pF, 50V, Ceramic capacitor, NPO, 0603</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>1206D476MAT2A</td>
<td>AVX</td>
<td>47µF, 6.3V, Ceramic capacitor, X5R, 1206</td>
<td>1</td>
</tr>
<tr>
<td>C7</td>
<td>06035C101MAT2A</td>
<td>AVX</td>
<td>100pF, 50V, Ceramic capacitor, X7R, 0603</td>
<td>1</td>
</tr>
<tr>
<td>C8</td>
<td>GRM188R71H391KA01D</td>
<td>Murata</td>
<td>390pF, 50V, Ceramic capacitor, X7R, 0603</td>
<td>1</td>
</tr>
<tr>
<td>C9, C10</td>
<td>GRM31CR60J476ME19L</td>
<td>Murata</td>
<td>47µF, 6.3V, Ceramic capacitor, X5R, 0603</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>C3216X5R0J476M</td>
<td>TDK</td>
<td>47µF, 6.3V, Ceramic capacitor, X5R, 0603</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1206D476MAT2A</td>
<td>AVX</td>
<td>47µF, 6.3V, Ceramic capacitor, X5R, 0603</td>
<td>1</td>
</tr>
<tr>
<td>C13</td>
<td>GRM188R71I102KA01D</td>
<td>Murata</td>
<td>1nF, 50V, Ceramic capacitor, X7R, 0603</td>
<td>1</td>
</tr>
<tr>
<td>C14</td>
<td>GRM188R71I103KA01D</td>
<td>Murata</td>
<td>10nF, 50V, Ceramic capacitor, X7R, 0603</td>
<td>1</td>
</tr>
<tr>
<td>C15, C26</td>
<td>0603ZD105KAT2A</td>
<td>AVX</td>
<td>1µF, 10V, Ceramic capacitor, X5R, 0603</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>GRM188R61A105K</td>
<td>Murata</td>
<td>1µF, 10V, Ceramic capacitor, X5R, 0603</td>
<td>1</td>
</tr>
<tr>
<td>C22, C28</td>
<td>VJ0603A121JXACW1BC</td>
<td>Vishay</td>
<td>120pF, 25V, Ceramic capacitor, NPO, 0603</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>06033A121JAT2A</td>
<td>AVX</td>
<td>120pF, 25V, Ceramic capacitor, NPO, 0603</td>
<td>1</td>
</tr>
<tr>
<td>C23, C12</td>
<td>VJ0603Y221KXACW1BC</td>
<td>Vishay</td>
<td>220pF, 50V, Ceramic capacitor, X7R, 0603</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>06033C221JAT2A</td>
<td>AVX</td>
<td>220pF, 50V, Ceramic capacitor, X7R, 0603</td>
<td>1</td>
</tr>
<tr>
<td>C24, C11</td>
<td>TCJB107M006R0070</td>
<td>AVX</td>
<td>100µF, 6.3V, Tantalum capacitor, 1210</td>
<td>2</td>
</tr>
<tr>
<td>C25, C31</td>
<td>C4532X5R0J107M</td>
<td>TDK</td>
<td>100µF, 6.3V, Ceramic capacitor, X5R, 1812</td>
<td>3</td>
</tr>
<tr>
<td>C31</td>
<td>Open (2SEPC2700M)</td>
<td>Sanyo</td>
<td>2700µF, 2.5V OS-CON Cap</td>
<td>1</td>
</tr>
<tr>
<td>C32, C21</td>
<td>EEE-FPA122UAP</td>
<td>Panasonic</td>
<td>1200µF, 10V, Electrolytic capacitor, SMD, 10x10.2-case</td>
<td>1</td>
</tr>
<tr>
<td>L1</td>
<td>CDEP105ME-1R2MC</td>
<td>Sumida</td>
<td>1.2µH, 21A, Inductor, 10.4mmX10.4mm</td>
<td>1</td>
</tr>
<tr>
<td>Q1</td>
<td>2N7002E(SOT-23)</td>
<td>Vishay</td>
<td>Signal MOSFET, SOT-23-6</td>
<td>1</td>
</tr>
<tr>
<td>Q21, Q22</td>
<td>SUD50N02-06P</td>
<td>Vishay</td>
<td>Low VGS(th) N-Channel 20-V (D-S)</td>
<td>2</td>
</tr>
<tr>
<td>R1</td>
<td>CRCW0603820RFT1</td>
<td>Vishay Dale</td>
<td>820Ω, Resistor, 1%, 0603</td>
<td>1</td>
</tr>
<tr>
<td>R2</td>
<td>CRCW0603698RFT1</td>
<td>Vishay Dale</td>
<td>698Ω, Resistor, 1%, 0603</td>
<td>1</td>
</tr>
<tr>
<td>R3</td>
<td>CRCW0603202RFT1</td>
<td>Vishay Dale</td>
<td>20K, Resistor, 1%, 0603</td>
<td>1</td>
</tr>
<tr>
<td>R4</td>
<td>CRCW0603475RFT1</td>
<td>Vishay Dale</td>
<td>47.5K, Resistor, 1%, 0603</td>
<td>1</td>
</tr>
<tr>
<td>R5</td>
<td>CRCW06031003FRT1</td>
<td>Vishay Dale</td>
<td>100K, Resistor, 1%, 0603</td>
<td>1</td>
</tr>
</tbody>
</table>
## Bill of Materials (Continued)

<table>
<thead>
<tr>
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<th>Description</th>
<th>Qty.</th>
</tr>
</thead>
<tbody>
<tr>
<td>R21</td>
<td>CRCW0805510RFKTA</td>
<td>Vishay Dale</td>
<td>510Ω, Resistor, 1%, 0805</td>
<td>1</td>
</tr>
<tr>
<td>R23, R24</td>
<td>CRCW06031K00FKTA</td>
<td>Vishay Dale</td>
<td>1K, Resistor, 1%, 0603</td>
<td>2</td>
</tr>
<tr>
<td>R22</td>
<td>CRCW06030000FKTA</td>
<td>Vishay Dale</td>
<td>0Ω, Resistor, 1%, 0603</td>
<td>1</td>
</tr>
<tr>
<td>R25</td>
<td>CRCW06031002FRT1</td>
<td>Vishay Dale</td>
<td>10K, Resistor, 1%, 0603</td>
<td>1</td>
</tr>
<tr>
<td>U1</td>
<td>MIC22950YML</td>
<td>Micrel</td>
<td>10A, 0.4MHz-2MHz Synchronous Buck Regulator</td>
<td>1</td>
</tr>
<tr>
<td>U21</td>
<td>MIC5164YMM</td>
<td>Micrel</td>
<td>Dual Regulator Controller for DDR, DDR2, DDR3</td>
<td>1</td>
</tr>
</tbody>
</table>

Notes:
2. TDK:  [www.tdk.com](http://www.tdk.com).
3. AVX:  [www.avx.com](http://www.avx.com).
4. Vishay:  [www.vishay.com](http://www.vishay.com).
7. Sumida:  [www.sumida.com](http://www.sumida.com).
PCB Layout Recommendations – $V_{DDQ}$ and MOSFET Input Tied Together
PCB Layout Recommendations – $V_{DDQ}$ and MOSFET Input Tied Together (Continued)
PCB Layout Recommendations – $V_{DDQ}$ and MOSFET Input Tied Together (Continued)
Package Information

10-Pin MSOP (MM)

NOTES:
1. DIMENSIONS ARE IN MM (INCHES).
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   EITHER OF WHICH SHALL NOT EXCEED 0.20 (0.008)
   PER SIDE.
Recommended Landing Pattern

Recommended Land Pattern for MSOP 10 Lead

LP # MSOP-18LD LP-1
All units are in mm
Tolerance ± 0.05 if not noted

10-Pin MSOP (MM)

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