The PIC16F84 (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS30430C), except for the anomalies described below.

All the problems listed here will be addressed in future revisions of the PIC16F84 silicon.

1. **Module: CPU (STATUS bit)**
   
The operation of the power-down (PD) bit in the STATUS register may not function correctly for temperatures below -20 °C.
   
   **Work Around**
   
   None

2. **Module: Data EEPROM**
   
   Do not perform a modify (set or clear a bit) of the EECON1 register one instruction cycle after an EEPROM read. This will corrupt the EEDATA register.
   
   **Example:**
   
   ```
   BSF EECON1, RD
   BCF EECON1, WREN
   ```
   
   **Work Around**
   
   Use either of the following two code segment in place of the above example.
   
   ```
   BSF EECON1, RD
   NOP
   BCF EECON1, WREN
   ```
   
   or
   
   ```
   BCF EECON1, WREN
   BSF EECON1, RD
   ```

3. **Module: Timer0**
   
The TMR0 register may increment when the WDT postscaler is switched to the Timer0 prescaler. If TMR0 = FFh, this will cause TMR0 to overflow (setting T0IF).
   
   **Work Around**
   
   Follow the following sequence:
   
   a) Read the 8-bit TMR0 register into the W register
   b) Clear the TMR0 register
   c) Assign WDT postscaler to Timer0
   d) Write W register to TMR0

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**Note:** As with any windowed EPROM device, please cover the window at all times, except when erasing.
Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30430C), the following clarifications and corrections should be noted.

1. **Module: Data EEPROM**

   In the PIC16F8X Data Sheet (DS30430B), the following clarifications and corrections should be noted.

   a) Erase/Write Cycle Time for Data EEPROM should be changed from 10 ms maximum to 20 ms maximum, as shown in Table 1.

<table>
<thead>
<tr>
<th>Parameter No.</th>
<th>Sym.</th>
<th>Characteristic</th>
<th>Actual Data</th>
<th>Data Sheet</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>D122</td>
<td>TDEW</td>
<td>Erase Write Cycle Time</td>
<td>10</td>
<td>20</td>
</tr>
</tbody>
</table>

   * This parameter is characterized but not tested

2. **Module: Device Idp**

   a) The maximum device Idp in the LP oscillator mode (at 32KHz, 2.0 V, and WDT disabled) should be changed from 32 μA maximum to 45 μA maximum, as shown in Table 1.

<table>
<thead>
<tr>
<th>Parameter No.</th>
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</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td>D014</td>
<td>IDD</td>
<td>Supply Current</td>
<td>15</td>
<td>45</td>
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