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Table of Contents

Preface ....................................................................................................................... 5

Chapter 1. Overview
   1.1 Introduction ..................................................................................................... 9
   1.2 Features ......................................................................................................... 9
      1.2.1 Test Points .......................................................................................... 10
      1.2.2 Electrical Characteristics ..................................................................... 10
      1.2.3 Analog and Digital Signals ................................................................. 11
      1.2.4 dsPIC33CH512MP506 DP PIM – PCB Edge Connector ...................... 11
   1.3 UART Communication .................................................................................. 12
   1.4 Low-Frequency Bode Plot Measurements .................................................. 12

Appendix A. Board Layout and Schematics
   A.1 Pinout ........................................................................................................... 15
   A.2 Board Schematics ........................................................................................ 17
   A.3 PCB Layout .................................................................................................. 19

Appendix B. Bill of Materials (BOM)
   B.1 Bill of Materials .......................................................................................... 23

Appendix C. Characterization Data
   C.1 Measurement Accuracy Impacts ................................................................. 27
      C.1.1 High-Speed Analog Signal Tracking Considerations ......................... 27
      C.1.2 Example .............................................................................................. 29

Worldwide Sales and Service .................................................................................... 34
Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and
documentation are constantly evolving to meet customer needs, so some actual dialogs
and/or tool descriptions may differ from those in this document. Please refer to our website
(www.microchip.com) to obtain the latest documentation available.

Documents are identified with a “DS” number. This number is located on the bottom of each
page, in front of the page number. The numbering convention for the DS number is
“DSXXXXXXXXA”, where “XXXXXXXX” is the document number and “A” is the revision level
of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help.
Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the
dsPIC33CH512MP506 Digital Power Plug-In Module (PIM). Items discussed in this
chapter include:

• Document Layout
• Conventions Used in this Guide
• Recommended Reading
• The Microchip Website
• Product Change Notification Service
• Customer Support
• Document Revision History

DOCUMENT LAYOUT

This document provides an overview of the dsPIC33CH512MP506 Digital Power PIM.
The document is organized as follows:

• Chapter 1. “Overview” — This chapter introduces the dsPIC33CH512MP506
  Digital Power PIM and provides a brief overview of its various features.
• Appendix A. “Board Layout and Schematics” — This appendix presents the
  schematics and the board layouts for the dsPIC33CH512MP506 Digital Power PIM.
• Appendix B. “Bill of Materials (BOM)” — This appendix presents the Bill of
  Materials for the dsPIC33CH512MP506 Digital Power PIM.
• Appendix C. “Characterization Data” — This appendix provides
  characterization data and guidance on sub-circuits of the dsPIC33CH512MP506
  Digital Power PIM.
CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

## DOCUMENTATION CONVENTIONS

<table>
<thead>
<tr>
<th>Description</th>
<th>Represents</th>
<th>Examples</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Arial font:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Italic characters</td>
<td>Referenced books</td>
<td><em>MPLAB® IDE User’s Guide</em></td>
</tr>
<tr>
<td>Emphasized text</td>
<td></td>
<td><em>...is the only compiler...</em></td>
</tr>
<tr>
<td>Initial caps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A window</td>
<td>the Output window</td>
<td></td>
</tr>
<tr>
<td>A dialog</td>
<td>the Settings dialog</td>
<td></td>
</tr>
<tr>
<td>A menu selection</td>
<td>select Enable Programmer</td>
<td></td>
</tr>
<tr>
<td>Quotes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A field name in a window or</td>
<td>&quot;Save project before build&quot;</td>
<td></td>
</tr>
<tr>
<td>dialog</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Underlined, italic text with</td>
<td></td>
<td></td>
</tr>
<tr>
<td>right angle bracket</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A menu path</td>
<td></td>
<td><em>File&gt;Save</em></td>
</tr>
<tr>
<td>Bold characters</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A dialog button</td>
<td>Click OK</td>
<td></td>
</tr>
<tr>
<td>A tab</td>
<td>Click the <strong>Power</strong> tab</td>
<td></td>
</tr>
<tr>
<td>N'Rnnnn</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A number in verilog format,</td>
<td></td>
<td></td>
</tr>
<tr>
<td>where N is the total number</td>
<td></td>
<td></td>
</tr>
<tr>
<td>of digits, R is the radix and</td>
<td></td>
<td></td>
</tr>
<tr>
<td>n is a digit.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Text in angle brackets &lt; &gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A key on the keyboard</td>
<td></td>
<td><em>Press &lt;Enter&gt;, &lt;F1&gt;</em></td>
</tr>
<tr>
<td><strong>Courier New font:</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Plain Courier New</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sample source code</td>
<td></td>
<td><em>#define START</em></td>
</tr>
<tr>
<td>Filenames</td>
<td></td>
<td><em>autoexec.bat</em></td>
</tr>
<tr>
<td>File paths</td>
<td></td>
<td><em>c:\mcc18\h</em></td>
</tr>
<tr>
<td>Keywords</td>
<td></td>
<td><em>_asm, _endasm, static</em></td>
</tr>
<tr>
<td>Command-line options</td>
<td></td>
<td><em>-Opa+, -Opa-</em></td>
</tr>
<tr>
<td>Bit values</td>
<td></td>
<td><em>0, 1</em></td>
</tr>
<tr>
<td>Constants</td>
<td></td>
<td><em>0xFF, ‘A’</em></td>
</tr>
<tr>
<td>Italic Courier New</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A variable argument</td>
<td></td>
<td><em>file.o, where file can be any valid</em></td>
</tr>
<tr>
<td>Square brackets [ ]</td>
<td>Optional arguments</td>
<td><em>mcc18 [options] file [options]</em></td>
</tr>
<tr>
<td>Curly brackets and pipe</td>
<td>Choice of mutually exclusive arguments; an OR selection</td>
<td>*errorlevel {0</td>
</tr>
<tr>
<td>character: { }</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ellipses...</td>
<td>Replaces repeated text</td>
<td><em>var_name [, var_name...]</em></td>
</tr>
<tr>
<td>Represents code supplied by</td>
<td></td>
<td><em>void main (void)</em></td>
</tr>
<tr>
<td>user</td>
<td></td>
<td><em>{ ... }</em></td>
</tr>
</tbody>
</table>
RECOMMENDED READING

This user’s guide describes how to use the dsPIC33CH512MP506 Digital Power PIM. Other useful document(s) are listed below. The following Microchip document is available and recommended as a supplemental reference resource:

• “dsPIC33CH128MP508 Family Data Sheet” (DS70005319)
  Refer to this document for detailed information on the dsPIC33CH Dual Core Digital Signal Controllers (DSCs). Reference information found in this data sheet includes:
  - Device memory maps
  - Device pinout and packaging details
  - Device electrical specifications
  - List of peripherals included on the devices

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• Corporate Application Engineer (CAE)
• Embedded Solutions Engineer (ESE)

Customers should contact their distributor, representative or Embedded Solutions Engineer (ESE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the website at:
http://www.microchip.com/support.

DOCUMENT REVISION HISTORY

Revision A (April 2019)

This is the initial version of this document.
1.1 INTRODUCTION

The dsPIC33CH512MP506 Digital Power Plug-In Module (DP PIM) is a demonstration board that, in conjunction with different power boards, showcases the Microchip dsPIC33CH512MP506 16-Bit Digital Signal Controller (DSC) features. The DP PIM provides access to the dsPIC33CH512MP506 analog inputs, the Digital-to-Analog Converter (DAC) output, the Pulse-Width Modulation (PWM) outputs and the General Purpose Input and Output (GPIO) ports.

The series of Microchip DP PIMs feature different device families, from dsPIC33E to dsPIC33CK and dsPIC33CH. These devices have different CPU performance levels as well as peripheral features and functions. However, even if the features and performance levels are different, all DP PIMs have the same functional card edge connector pinout to support seamless migration between device families.

1.2 FEATURES

The dsPIC33CH512MP506 DP PIM has the following features, as shown in Figure 1-1.

1. Microchip dsPIC33CH512MP506 16-Bit DSC (64-pin TQFP package).
2. ICSP™ programming header for the Master core (6-pin, 2.54 mm header).
3. ICSP programming header for the Slave core (6-pin, 1.27 mm header – not populated).
4. On-board LDO with Power Good (PG) function.
5. Solder pad for ground connection.
7. MCP2221A USB to UART/i^2^C serial converter.
8. Power indicator LED (Green).
10. Board edge connection interface for analog inputs/outputs.
11. Board edge connection interface for PWM outputs, digital peripherals and GPIO ports.

Note: Both cores can be programmed and debugged through one ICSP interface.
12. Analog input with op amp buffer via test point loop connector; can be used for Bode plot measurements.
14. Test point loop for DAC output.
15. Test point to access RD13 (also available on card edge connector pin 12).
16. Test point to access RD15 (also available on card edge connector pin 8).
17. Op amp buffers for medium speed ADC inputs.
18. MEMS oscillator.

Board dimensions are: 51 mm (length) x 38.5 mm (width).

1.2.1 Test Points

Table 1-1 lists the test points available on the dsPIC33CH512MP506 DP PIM.

<table>
<thead>
<tr>
<th>Test Point Name</th>
<th>Function/Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TP1, TP2</td>
<td>Bode Measurement Signal Injection Point</td>
</tr>
<tr>
<td>TP3</td>
<td>RB2_DAC1_OUT: Digital-to-Analog Converter Output</td>
</tr>
<tr>
<td>TP4</td>
<td>Test Point for Debugging: Access to RD13 through 270Ω Resistor</td>
</tr>
<tr>
<td>TP5</td>
<td>General Purpose Test Point Connected to RD15 along with LD2 (Red LED)</td>
</tr>
</tbody>
</table>

1.2.2 Electrical Characteristics

Table 1-2 shows the electrical characteristics of the dsPIC33CH512MP506 DP PIM.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>3.6 VDC to 10 VDC, Absolute Maximum 16 VDC</td>
</tr>
<tr>
<td>Current Consumption</td>
<td>Minimum 82 mA, Typical 108 mA, Absolute Maximum 200 mA</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>Minimum 295 mW, Typical 414 mW, Maximum 1100 mW</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

Note: Typical Test Conditions: Ambient Temperature +25°C, Master core running at 90 MIPS, Slave core running at 100 MIPS, all peripherals powered but not enabled, power-on LED, LD1, active, no USB device or debugger connected.
1.2.3 Analog and Digital Signals

The dsPIC33CH512MP506 DP PIM ensures good signal integrity and provides all signals needed to control a power train. These signals are divided into two main sections: Analog and Digital.

1. Analog Section

The analog section is located at the short segment of the edge connector. It consists of 17 signals, all referenced to the analog ground. These lines are split into the following subsections:

• High-Speed Comparator Inputs: RC filtered with corner frequency of 10 MHz and maximum signal rise/fall time of 33 ns. These lines are designed to be used with on-chip comparators for signal tracking tasks, such as peak, valley or zero-cross detections.

• High-Speed ADC Inputs: RC filtered with corner frequency of 2 MHz and maximum signal rise/fall time of 180 ns. These lines are connected to the Track-and-Hold (T&H) circuitry of the dedicated ADC inputs and to the Sample-and-Hold (S&H) circuitry of the shared ADC inputs.

• Medium Speed ADC Inputs: Buffered input lines, RC filtered with corner frequency of 1 MHz and maximum signal rise/fall time of 360 ns.

• Low-Speed ADC Inputs: RC filtered with corner frequency of 190 kHz and maximum signal rise/fall time of 1.8 µs.

• 12-Bit DAC Output with Optional On-Board RC Filtering.

2. Digital Section

The digital section is located at the long segment of the edge connector. It consists of 31 signals, all referenced to digital ground. These lines are split into four subsections:

• High-Speed PWM Outputs: Each line has a 75Ω series resistance.

• Medium Speed GPIO: Each line has a 270Ω series resistance.

• Programing/Debugging Lines: Each line has a 100Ω series resistance.

• Communication Lines (SPI): Each line has a 75Ω series resistance.

2. Note: The range of the digital I/Os allows access to other peripheral functions of the populated DSC, such as communication interfaces like I²C, SPI, UART, Single-Edge Nibble Transmission (SENT), Controller Area Network (CAN), input capture, output compare, Combinatorial Logic Cells (CLC) and more. Please refer to the device data sheet for further information on available functions.

1.2.4 dsPIC33CH512MP506 DP PIM – PCB Edge Connector

The dsPIC33CH512MP506 DP PIM has an edge connector compatible with any application board that provides a mating socket.

The mating socket type is Samtec, Inc.: MECF-30-01-L-DV-WT.
1.3 UART COMMUNICATION
The on-board USB to UART serial bridge enables easy serial connection to PCs. The USB port can provide power to the Digital Power PIM and allows the user to communicate with the dsPIC® Digital Signal Controller (DSC).

The USB driver package and software tool support of the MCP2221A serial converter also offers free terminal software for I2C Master and Slave emulation, as well as generic API drivers for custom software development. Please visit the MCP2221A product web page for more details (www.microchip.com).

1.4 LOW-FREQUENCY BODE PLOT MEASUREMENTS
The dsPIC33CH512MP506 device, along with an additional on-board circuitry, allows Bode plot measurements to be performed without the need for an isolation transformer. The transformer might still be required if the injected signal tends to be at a very low frequency (for instance, in case of Power Factor Correction (PFC) applications).

Perform the following steps:
1. Solder the 150Ω resistor from position R74 to R94. Make sure that the RD10_S1AN13_IN line is not driven by any other low-impedance source.
2. Run the power stage in Open-Loop mode with a fixed duty cycle.
3. Connect the Bode 100 AC output to TP1 and TP2. The on-board operational amplifier will add a VDD/2 (1.65V) offset. In this case, no injection transformer is needed.
4. Connect RB2_DAC1_OUT to CH2 of the Bode 100.
5. Use the S1AN13 input to sample the signal from Bode 100 in every PWM cycle at Frequency Switching (fsw) (action in firmware is needed).
6. Remove the Vdd/2 offset to regain a signal with no DC value (action in firmware is needed).
7. Add sampled AC signal to the nominal duty cycle (PDCx) (action in firmware is needed).
8. Use a second dedicated ADC core input (ANx) to sample the output of the plant at FSW. The output can be:
   • Output Voltage.
   • Average coil current sampled at TON/2, where TON is the switch-on time.
9. Duty cycle input and plant output are converted into an analog signal using RB2_DAC1_OUT.

The measured transfer function is the plant (power stage and digital modulator), after scaling and ADC sampling, versus digital duty cycle input (PDCx).

Note: Due to run-time delays of Sample-and-Hold circuits and conversion time of ADC and DAC, this measurement is only recommended for low-frequency measurements: a maximum two decades below sampling frequency.
Figure 1-2 and Figure 1-3 show examples of schemes of plant and closed-loop measurements, respectively.

**FIGURE 1-2: SCHEME OF PLANT MEASUREMENT**

[Diagram of plant measurement scheme with labels and connections]

**FIGURE 1-3: SCHEME OF CLOSED-LOOP MEASUREMENT**

[Diagram of closed-loop measurement scheme with labels and connections]
Appendix A. Board Layout and Schematics

This appendix contains the pinout, the schematics and the board layouts for the dsPIC33CH512MP506 DP PIM.

• Pinout
• Board Schematics
• PCB Layout

A.1 PINOUT

Pinout and electrical parameters are shown in Table A-1.

<table>
<thead>
<tr>
<th>Name</th>
<th>Edge Connector Pin</th>
<th>Device Pin</th>
<th>Function/Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND_A</td>
<td>1</td>
<td>20</td>
<td>Analog Ground</td>
<td></td>
</tr>
<tr>
<td>GND_A</td>
<td>2</td>
<td>20</td>
<td>Analog Ground</td>
<td></td>
</tr>
<tr>
<td>RB2_DAC1_OUT</td>
<td>3</td>
<td>33</td>
<td>DAC Output, Optional RC Filter</td>
<td>560R Series Resistance</td>
</tr>
<tr>
<td>RC7_AN15_IN</td>
<td>4</td>
<td>32</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 190 kHz, tr = 1.8 µs</td>
</tr>
<tr>
<td>RC0_S1AN10_IN</td>
<td>5</td>
<td>13</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 1 MHz, tr = 360 ns – Buffered</td>
</tr>
<tr>
<td>RC2_S1ANA0_IN</td>
<td>6</td>
<td>23</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 1 MHz, tr = 360 ns – Buffered</td>
</tr>
<tr>
<td>—</td>
<td>7</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>RC3_S1CMP3B_IN</td>
<td>8</td>
<td>27</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 10 MHz, tr = 33 ns</td>
</tr>
<tr>
<td>RD11_S1AN17_IN</td>
<td>9</td>
<td>30</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 1 MHz, tr = 360 ns – Buffered</td>
</tr>
<tr>
<td>RC1_S1ANA1_IN</td>
<td>10</td>
<td>22</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 1 MHz, tr = 360 ns – Buffered</td>
</tr>
<tr>
<td>RA2_S1AN16_IN</td>
<td>11</td>
<td>16</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 190 kHz, tr = 1.8 µs</td>
</tr>
<tr>
<td>RA3_S1ANO_IN</td>
<td>12</td>
<td>17</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 1.9 MHz, tr = 180 ns</td>
</tr>
<tr>
<td>RA1_AN1_IN</td>
<td>13</td>
<td>15</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 1.9 MHz, tr = 180 ns</td>
</tr>
<tr>
<td>RA4_S1AN1_IN</td>
<td>14</td>
<td>18</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 1.9 MHz, tr = 180 ns</td>
</tr>
<tr>
<td>RA0_AN0_IN</td>
<td>15</td>
<td>14</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 1.9 MHz, tr = 180 ns</td>
</tr>
<tr>
<td>RD10_S1AN13_IN</td>
<td>16</td>
<td>31</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 190 kHz, tr = 1.8 µs</td>
</tr>
<tr>
<td>RD12_S1AN14_IN</td>
<td>17</td>
<td>21</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 190 kHz, tr = 1.8 µs</td>
</tr>
<tr>
<td>RC6_S1CMP1B_IN</td>
<td>18</td>
<td>24</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 10 MHz, tr = 33 ns</td>
</tr>
<tr>
<td>—</td>
<td>19</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>RB1_S1AN4_IN</td>
<td>20</td>
<td>29</td>
<td>Analog Input, RC Filtered</td>
<td>F_c = 190 kHz, tr = 1.8 µs</td>
</tr>
<tr>
<td>Slot</td>
<td>21</td>
<td>Slot</td>
<td>Slot</td>
<td></td>
</tr>
<tr>
<td>Slot</td>
<td>22</td>
<td>Slot</td>
<td>Slot</td>
<td></td>
</tr>
<tr>
<td>—</td>
<td>23</td>
<td>—</td>
<td>—</td>
<td></td>
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<tr>
<td>RC8_RP56_ASDA1</td>
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<td>75R Series Resistance</td>
</tr>
<tr>
<td>RB12_RP44</td>
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<td>Digital General Purpose</td>
<td>270R Series Resistance</td>
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<td>RD14</td>
<td>26</td>
<td>11</td>
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<td>270R Series Resistance</td>
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<td>RB13_RP45</td>
<td>27</td>
<td>64</td>
<td>Digital General Purpose</td>
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### Table A-1: Pinout and Electrical Parameters (continued)

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<thead>
<tr>
<th>Name</th>
<th>Edge Connector Pin</th>
<th>Device Pin</th>
<th>Function/Description</th>
<th>Remarks</th>
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<td>RD9</td>
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<td>RD6_S1PWM6H</td>
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<td>PWM Output</td>
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<tr>
<td>RC9_ASCL1</td>
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<td>32 37</td>
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<tr>
<td>RD5_S1PWM6L</td>
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<td>33 44</td>
<td>PWM Output</td>
<td>75R Series Resistance</td>
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<td>RB11</td>
<td>_</td>
<td>34 62</td>
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<td>270R Series Resistance</td>
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<td>RB14_S1RP46</td>
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<td>RB10</td>
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<tr>
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<td>PWM Output</td>
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<td>PWM Output</td>
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<td>Digital General Purpose</td>
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<td>PWM Output</td>
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<td>48 4</td>
<td>Digital General Purpose</td>
<td>270R Series Resistance</td>
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<td>MCLR_IN</td>
<td>_</td>
<td>49 7</td>
<td>Device Reset</td>
<td>100R Series Resistance</td>
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<tr>
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<td>270R Series Resistance</td>
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<tr>
<td>RB4_PGC2</td>
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<td>51 35</td>
<td>Programing/Debugging</td>
<td>100R Series Resistance</td>
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<td>Digital General Purpose</td>
<td>270R Series Resistance</td>
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<tr>
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<td>53 46</td>
<td>Digital General Purpose</td>
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<tr>
<td>RD13</td>
<td>_</td>
<td>54 12</td>
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<tr>
<td>RB5_SDA2</td>
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<td>55 45</td>
<td>Digital General Purpose</td>
<td>75R Series Resistance</td>
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<tr>
<td>RB3_PGD2</td>
<td>_</td>
<td>56 34</td>
<td>Programing/Debugging</td>
<td>100R Series Resistance</td>
</tr>
<tr>
<td>VDD</td>
<td>_</td>
<td>57</td>
<td>LDO VDD Rail</td>
<td>6.3V max, 70 mA max</td>
</tr>
<tr>
<td>GND_D</td>
<td>_</td>
<td>58 9,26,40,56</td>
<td>Digital Ground</td>
<td>—</td>
</tr>
<tr>
<td>VDD</td>
<td>_</td>
<td>59</td>
<td>LDO VDD Rail</td>
<td>6.3V max, 70 mA max</td>
</tr>
<tr>
<td>GND_D</td>
<td>_</td>
<td>60 9,26,40,56</td>
<td>Digital Ground</td>
<td>—</td>
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</table>
Figure A-1 and Figure A-2 show the board schematics.

FIGURE A-1:  dsPIC33CH512MP506 DIGITAL POWER PIM SCHEMATIC REV. 1.0 (PAGE 1 OF 2)

Board Layout and Schematics
A.3 PCB LAYOUT

The dsPIC33CH512MP506 DP PIM is a four-layer FR4, 1.55 mm, Plated-Through-Hole (PTH) PCB construction. Figure A-3 through Figure A-5 illustrate the PCB layers and Figure A-6 shows the assembly drawings of the dsPIC33CH512MP506 DP PIM.

FIGURE A-3: dsPIC33CH512MP506 DIGITAL POWER PIM TOP SILKSCREEN AND TOP COPPER
FIGURE A-4: dsPIC33CH512MP506 DIGITAL POWER PIM MID1 AND MID2 INNER COPPER (BOTTOM VIEW)
FIGURE A-5: dsPIC33CH512MP506 DIGITAL POWER PIM BOTTOM COPPER AND BOTTOM SILKSCREEN (BOTTOM VIEW)

Bottom Copper

Bottom Silkscreen
FIGURE A-6: dsPIC33CH512MP506 DIGITAL POWER PIM TOP AND BOTTOM ASSEMBLY
Appendix B. Bill of Materials (BOM)

This appendix contains the Bill of Materials (BOM) for the dsPIC33CH512MP506 Digital Power PIM.

- Bill of Materials

B.1 BILL OF MATERIALS

Table B-1 shows the Bill of Materials for the dsPIC33CH512MP506.

<table>
<thead>
<tr>
<th>Qty</th>
<th>Designator</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>C0, C3, C8, C17, C18, C20, C21, C22, C23, C24, C51</td>
<td>Capacitor, Ceramic, 0.1 µF, 50V, 10%, X7R, SMD, 0402</td>
<td>TDK Corporation</td>
<td>C1005X7R1H104K050BB</td>
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<tr>
<td>2</td>
<td>C1, C2</td>
<td>Capacitor, Ceramic, 47 pF, 50V, 5%, NP0, SMD, 0402</td>
<td>Murata Electronics©</td>
<td>GRM1555C1H470JA01D</td>
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<tr>
<td>5</td>
<td>C6, C13, C14, C15, C16</td>
<td>Capacitor, Ceramic, 1 µF, 10V, 10%, X7S, SMD, 0402</td>
<td>TDK Corporation</td>
<td>C1005X7S1A105K050BC</td>
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<tr>
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<td>Murata Electronics</td>
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<tr>
<td>4</td>
<td>C9, C10, C11, C12</td>
<td>Capacitor, Ceramic, 10 µF, 10V, 20%, X5R, SMD, 0603</td>
<td>Samsung Group</td>
<td>CL10A106MP8NNNC</td>
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<td>TDK Corporation</td>
<td>C1005C0G1H560J050BA</td>
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<tr>
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<td>Capacitor, Ceramic, 560 pF, 50V, 5%, C0G, NP0, SMD, 0603</td>
<td>KEMET</td>
<td>C0603C561J5GACTU</td>
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<tr>
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<td>C32, C35, C36, C37, C38, C41, C42, C43, C44</td>
<td>Capacitor, Ceramic, 5600 pF, 25V, 5%, C0G, SMD, 0603</td>
<td>TDK Corporation</td>
<td>C1608C0G1E562J080AA</td>
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<td>Capacitor, Ceramic, 100 pF, 50V, 5%, NP0, SMD, 0603</td>
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<td>Johanson Technology Inc.</td>
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<td>Wurth Elektronik</td>
<td>82400152</td>
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<td>D2</td>
<td>Diode, Schottky, SBR1A20T5-7, 520 mV, 1A, 20V, SOD-523</td>
<td>Diodes Incorporated©</td>
<td>SBR1A20T5-7</td>
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<tr>
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<td>D3, D4, D5, D6</td>
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<td>Panasonic© - ECG</td>
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<td>FB1, FB2, FB3, FB4, FB5, FB6, FB7</td>
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<td>Murata Electronics</td>
<td>BLM15PX601SN1D</td>
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<td>J1</td>
<td>Connector Header-2.54, Male, 1x6 Gold, 5.84 MH TH, Vertical</td>
<td>FCI</td>
<td>68000-106HLF</td>
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<td>1</td>
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<td>Connector, USB 2.0, Micro-B, Female, TH/SMD, R/A</td>
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## TABLE B-1: dsPIC33CH512MP506 DIGITAL POWER PIM BILL OF MATERIALS (BOM) (CONTINUED)

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<th>Qty</th>
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<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
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<td>L1</td>
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<td>LTST-C190KGKT</td>
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<td>Keystone Electronics Corp.</td>
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<td>------------</td>
<td>-------------</td>
<td>--------------</td>
<td>-------------------------</td>
</tr>
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<td>Keystone Electronics Corp.</td>
<td>5004</td>
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<td>Microchip Technology Inc.</td>
<td>MCP1755T-3302E/OT</td>
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<td>U3</td>
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<td>Microchip Technology Inc.</td>
<td>dsPIC33CH512MP506-I/PT</td>
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<td>Microchip Technology Inc.</td>
<td>MCP6V91UT-E/LTY</td>
</tr>
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<td>Microchip Technology Inc.</td>
<td>DSC6011JI2A-008.0000</td>
</tr>
</tbody>
</table>
Appendix C. Characterization Data

This chapter provides some characterization data and further guidance on sub-circuits of this Digital Power PIM to allow engineers to gain a better understanding of technical limitations, as well as enable users to solve design trade-offs in additional circuits on custom boards, such as signal conditioning or auxiliary power supplies.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range), and therefore, outside the warranted range.

C.1 MEASUREMENT ACCURACY IMPACTS

C.1.1 High-Speed Analog Signal Tracking Considerations

Each of the four groups of the analog inputs, high-speed ADC, mid-speed ADC, low-speed ADC and high-speed comparator inputs have been equipped with RC low-pass filters to prevent corruption of sampling results, such as alias-frequencies being injected into a series of ADC sampling results, and to ensure proper operation of the high-speed comparators in noisy environments. These deliberate bandwidth limitations, however, may affect the accuracy of the ADC results when tracking high-speed signals.

C.1.1.1 FILTER BANDWIDTH IMPACTS

This section discusses the influence of the RC low-pass filter bandwidth limits versus the expected sampling error to allow designers to identify the maximum signal slew rate, which can be tracked with a certain known accuracy.

The cutoff frequency, \( f_c \), of an RC low-pass filter defines the frequency at which its output signal magnitude is reduced by -3dB.

The first-order RC filter cutoff frequency is defined by Equation C-1.

**EQUATION C-1:**

\[
    f_c = \frac{1}{2\pi(R_{Filt}C_{Filt})}
\]

When using high-speed ADCs with sampling times of 10 ns to 50 ns or less, tracking signal transients at this frequency will also show a 3 dB offset in ADC results in accordance to the damped signal gain. To allow a more accurate analysis of the tracking error, with regards to the transient frequency, we need to look at the total gain characteristic over frequency.
The transfer function of a first-order RC low-pass filter is defined by Equation C-2 through Equation C-4.

\[
\text{EQUATION C-2:} \quad H(s) = \frac{1}{1 + \frac{s}{\omega_c}}
\]

\[
\text{EQUATION C-3:} \quad \omega_c = 2\pi f_c = \frac{1}{R_{\text{Filt}} C_{\text{Filt}}}
\]

\[
\text{EQUATION C-4:} \quad H(s) = \frac{1}{1 + sR_{\text{Filt}} C_{\text{Filt}}}
\]

\[
\text{FIGURE C-1: FIRST-ORDER RC LOW-PASS FILTER TRANSFER FUNCTION}
\]

First-Order RC Filter Transfer Function

\[ R = 270\Omega, \ C = 560 \ \text{pF} \]

By plotting the frequency domain transfer function of the RC filter, it is shown that the output voltage of the RC filter network at the cutoff frequency, \( f_c \), is not only damped in amplitude, but also shifted in time. While the amplitude reduction is absolute, the phase delay may require a relocation of the ADC sample trigger to achieve accurate results.

As both magnitude and phase of the RC filter output signal do not change instantly, but over frequency with varying degree, the deviation from the unfiltered feedback signal, and thus, the related ADC result deviation, may have to be considered.
C.1.2 Example

In order to demonstrate the impact of the on-board RC filtering, the following example shows the impact when tracking the average value of a 500 kHz at 50% duty cycle current feedback signal with minimum sampling error.

Let the average value be 500 mV and the peak-to-peak voltage 200 mV, following ideal current-to-voltage conversion. Figure C-2 shows the unfiltered ideal signal along with the waveforms obtained after this signal is passed through any of the on-board RC filters. Note that the filtering does not alter the average value along (ADC Input Voltage = 0.5) any of the filtered signals. The mid-points of each filtered AC signals, however, have been shifted in time with respect to the phase delay of the RC filter. When this phase delay is not properly considered, the ADC trigger may be displaced from the desired average point of the oversampled signal, resulting in a significant measurement error.

FIGURE C-2: UNFILTERED AND FILTERED TRIANGULAR WAVEFORMS
Depending on the application, in order to obtain the average value with the required accuracy, a time delay in the sampling trigger of the ADC might need to be introduced. In our specific case, in order to take the sample with the best accuracy, the trigger should be offset by approximately 60, 135 and 390 ns, as shown in Figure C-3.

**FIGURE C-3: SAMPLING TRIGGER PLACEMENT FOR BEST ACCURACY**

C.1.2.1 STEP RESPONSE DELAY ESTIMATION

Deriving from Equation C-1, the time constant of the first-order RC filter is defined by Equation C-5, which is generally used to characterize the response of a first-order RC filter to a step input, as shown in Equation C-6.

**EQUATION C-5:**

\[ \tau = R_{\text{Filt}} \cdot C_{\text{Filt}} \]

**EQUATION C-6:**

\[ V_{\text{OUT}}(t) = V_{\text{IN}}(t) \cdot (1 - e^{-t/\tau}) \]
Figure C-4 shows the calculated step responses of the on-board filters normalized to the input voltage.

**FIGURE C-4: NORMALIZED STEP RESPONSE**

In case a sample is taken at the filter output time, $t$, after the step input was applied, the percentage error with respect to the settled value can be calculated by using Equation C-7 and Equation C-8 (substituting Equation C-6).

**EQUATION C-7:**

$$
\varepsilon(t) = 100 \cdot \frac{V_{OUT}(t) - V_{IN}(t)}{V_{IN}(t)}
$$

**EQUATION C-8:**

$$
\varepsilon(t) = 100 \cdot e^{-t/\tau}
$$
Figure C-5 depicts the remaining percentage error with respect to the sampling time.

**FIGURE C-5: NORMALIZED OUTPUT ERROR**

On the other hand, if a maximum tolerable percentage error, $\varepsilon_{\text{max}}$, is defined in advance, the earliest time the sample should be taken can be calculated by using Equation C-9, which is obtained from Equation C-8 by expressing $t$.

**EQUATION C-9:**

$$t_s = -\tau \cdot \ln\left(\frac{\varepsilon_{\text{max}}}{100}\right)$$

Filter capacitors on the board are either 560 pF or 5600 pF, whereas the on-chip hold capacitance is around 5 pF. Due to the large ratio of the on-board versus on-chip capacities, and for the sake of simplicity, the loading effect of the Sample-and-Hold (S&H) circuitry has been neglected here.
Demanding applications, however, might need to consider the loading effect of the S&H capacitance as well. The electrical model shown in Figure C-6 can be used to make more elaborate calculations.

**FIGURE C-6:**

Legend:

- **CPIN** = Input Capacitance
- **VT** = Threshold Voltage
- **RSS** = Sampling Switch Resistance
- **RIC** = Interconnect Resistance
- **RS** = Source Resistance
- **CHOLD** = Sample-and-Hold Capacitance
- **ILEAKAGE** = Leakage Current at the Pin due to Various Junctions

**Note 1:** The CPIN value depends on the device package and is not tested. The effect of the CPIN is negligible if RS ≤ 5 kΩ.
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