Current Bias Generator (CBG)

HIGHLIGHTS

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1.0 INTRODUCTION

The Current Bias Generator (CBG) consists of two classes of current sources: 10 µA and 50 µA sources. The major features of each current source are:

- **10 µA Current Sources:**
  - Current sourcing only
  - Up to four independent sources
- **50 µA Current Sources:**
  - Selectable current sourcing or sinking
  - Selectable current mirroring for sourcing and sinking

A simplified block diagram of the CBG module is shown in Figure 1-1.

---

**Figure 1-1: Current Bias Generator Sources**

10 µA Source

```
ON
I10ENx
AVDD

ADC(R)
```

```
SRCENx
ON
AVDD

ADC(R)
```

50 µA Source

```
ON
I/O Pin

RESD(f)
```

```
ON
I/O Pin

RESD(f)
```

---

**Note 1:** RESD is typically 300 Ohms; for more information, refer to the device data sheet.

**Note 2:** Refer to the device data sheet for information on the ADC internal resistance.
2.0 CBG CONTROL REGISTERS

This section outlines the specific functions of each register that controls the operation of the CBG module. The registers are as follows:

- **BIASCON: Current Bias Generator Control Register**
  - The enables for the CBG module
  - The Individual enables for each 10 µA current source

- **IBIASCONH: Current Bias Generator 50 µA Current Source Control High**
  - The individual source enables for each source
  - The individual sink enables for each source
  - The Current Mirror mode reference enable for each source
  - The Current Mirror mode enabled for each source

- **IBIASCONL: Current Bias Generator 50 µA Current Source Control Low**
  - The individual source enables for each source
  - The individual sink enables for each source
  - The Current Mirror mode reference enable for each source
  - The Current Mirror mode enabled for each source
2.1 Register Map

Table 2-1 provides a brief summary of the related Current Bias Generator (CBG) module registers. The corresponding registers appear after the summary, followed by a detailed description of each register.

Table 2-1: Current Bias Generator (CBG) Register Map

<table>
<thead>
<tr>
<th>Name</th>
<th>Bit Range</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIASCON</td>
<td>15:0</td>
<td>ON</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>10EN3 10EN2 10EN1 10EN0</td>
</tr>
<tr>
<td>IBIASCONH</td>
<td>15:0</td>
<td>—</td>
<td>—</td>
<td>SHRSRCEN3</td>
<td>SHRSNKEN3</td>
<td>GENSRCEN3</td>
<td>GENRSNKEN3</td>
<td>SRCEN3</td>
<td>SNKEN3</td>
<td>—</td>
<td>—</td>
<td>SHRSRCEN2</td>
<td>SHRSNKEN2</td>
<td>GENSRCEN2</td>
<td>GENRSNKEN2</td>
<td>SRCEN2</td>
<td>SNKEN2</td>
</tr>
<tr>
<td>IBIASCONL</td>
<td>15:0</td>
<td>—</td>
<td>—</td>
<td>SHRSRCEN1</td>
<td>SHRSNKEN1</td>
<td>GENSRCEN1</td>
<td>GENRSNKEN1</td>
<td>SRCEN1</td>
<td>SNKEN1</td>
<td>—</td>
<td>—</td>
<td>SHRSRCEN0</td>
<td>SHRSNKEN0</td>
<td>GENSRCEN0</td>
<td>GENRSNKEN0</td>
<td>SRCEN0</td>
<td>SNKEN0</td>
</tr>
</tbody>
</table>

Legend: — = unimplemented, read as ‘0’.
Current Bias Generator (CBG)

Register 2-1: BIASCON: Current Bias Generator Control Register

<table>
<thead>
<tr>
<th>bit 15</th>
<th>bit 14-4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ON</strong>: Current Bias Module Enable bit</td>
<td><strong>Unimplemented</strong>: Read as ‘0’</td>
<td><strong>I10EN3</strong>: 10 µA Enable for Output #3 bit</td>
<td><strong>I10EN2</strong>: 10 µA Enable for Output #2 bit</td>
<td><strong>I10EN</strong>: 10 µA Enable for Output #1 bit</td>
<td><strong>I10EN0</strong>: 10 µA Enable for Output #0 bit</td>
</tr>
<tr>
<td>1 = Module is enabled (10 µA and 50 µA sources)</td>
<td></td>
<td>1 = 10 µA output is enabled</td>
<td>1 = 10 µA output is enabled</td>
<td>1 = 10 µA output is enabled</td>
<td>1 = 10 µA output is enabled</td>
</tr>
<tr>
<td>0 = Module is disabled and powered down</td>
<td></td>
<td>0 = 10 µA output is disabled</td>
<td>0 = 10 µA output is disabled</td>
<td>0 = 10 µA output is disabled</td>
<td>0 = 10 µA output is disabled</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown
Register 2-2:  IBIASCONH: Current Bias Generator 50 µA Current Source Control High

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>---</td>
<td>---</td>
<td>SHRSRCEN3</td>
<td>SHRSNKEN3</td>
<td>GENSRCEN3(1)</td>
<td>GENSNKEN3(1)</td>
<td>SRCEN3</td>
<td>SNKEN3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>---</td>
<td>---</td>
<td>SHRSRCEN2</td>
<td>SHRSNKEN2</td>
<td>GENSRCEN2(1)</td>
<td>GENSNKEN2(1)</td>
<td>SRCEN2</td>
<td>SNKEN2</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 15-14   Unimplemented: Read as ‘0’
bit 13  SHRSRCEN3: Share Source Enable for Output #3 bit
       1 = Sourcing Current Mirror mode is enabled (enables reference sharing)
       0 = Sourcing Current Mirror mode is disabled
bit 12  SHRSNKEN3: Share Sink Enable for Output #3 bit
       1 = Sinking Current Mirror mode is enabled (enables reference sharing)
       0 = Sinking Current Mirror mode is disabled
bit 11  GENSRCEN3: Generated Source Enable for Output #3 bit(1)
       1 = Source generates the current source mirror reference
       0 = Source does not generate the current source mirror reference
bit 10  GENSNKEN3: Generated Sink Enable for Output #3 bit(1)
       1 = Source generates the current sink mirror reference
       0 = Source does not generate the current sink mirror reference
bit 9   SRCEN3: Source Enable for Output #3 bit
        1 = Current source is enabled
        0 = Current source is disabled
bit 8   SNKEN3: Sink Enable for Output #3 bit
        1 = Current sink is enabled
        0 = Current sink is disabled
bit 7-6   Unimplemented: Read as ‘0’
bit 5   SHRSRCEN2: Share Source Enable for Output #2
        1 = Sourcing Current Mirror mode is enabled (enables reference sharing)
        0 = Sourcing Current Mirror mode is disabled
bit 4   SHRSNKEN2: Share Sink Enable for Output #2 bit
        1 = Sinking Current Mirror mode is enabled (enables reference sharing)
        0 = Sinking Current Mirror mode is disabled
bit 3   GENSRCEN2: Generated Source Enable for Output #2 bit(1)
        1 = Source generates the current source mirror reference
        0 = Source does not generate the current source mirror reference
bit 2   GENSNKEN2: Generated Sink Enable for Output #2 bit(1)
        1 = Source generates the current sink mirror reference
        0 = Source does not generate the current sink mirror reference
bit 1   SRCEN2: Source Enable for Output #2 bit
        1 = Current source is enabled
        0 = Current source is disabled
bit 0   SNKEN2: Sink Enable for Output #2 bit
        1 = Current sink is enabled
        0 = Current sink is disabled

Note 1:  When using Current Mirror mode, the corresponding SHRSRCENx or SHRSNKENx bit must be enabled on the master channel as well as all channels sharing the reference.
Current Bias Generator (CBG)

Register 2-3:  IBIASCONL: Current Bias Generator 50 µA Current Source Control Low

| Bit 15-14 | Unimplemented: Read as ‘0’ |
| Bit 13    | SHRSRCEN1: Share Source Enable for Output #1 bit |
|          | 1 = Sourcing Current Mirror mode is enabled (enables reference sharing) |
|          | 0 = Sourcing Current Mirror mode is disabled |
| Bit 12    | SHRSNKEN1: Share Sink Enable for Output #1 bit |
|          | 1 = Sinking Current Mirror mode is enabled (enables reference sharing) |
|          | 0 = Sinking Current Mirror mode is disabled |
| Bit 11    | GENSRCEN1: Generated Source Enable for Output #1 bit(1) |
|          | 1 = Source generates the current source mirror reference |
|          | 0 = Source does not generate the current source mirror reference |
| Bit 10    | GENSNKEN1: Generated Sink Enable for Output #1 bit(1) |
|          | 1 = Source generates the current sink mirror reference |
|          | 0 = Source does not generate the current sink mirror reference |
| Bit 9     | SRCEN1: Source Enable for Output #1 bit |
|          | 1 = Current source is enabled |
|          | 0 = Current source is disabled |
| Bit 8     | SNKEN1: Sink Enable for Output #1 bit |
|          | 1 = Current sink is enabled |
|          | 0 = Current sink is disabled |
| Bit 7-6   | Unimplemented: Read as ‘0’ |
| Bit 5     | SHRSRCEN0: Share Source Enable for Output #0 bit |
|          | 1 = Sourcing Current Mirror mode is enabled (enables reference sharing) |
|          | 0 = Sourcing Current Mirror mode is disabled |
| Bit 4     | SHRSNKEN0: Share Sink Enable for Output #0 bit |
|          | 1 = Sinking Current Mirror mode is enabled (enables reference sharing) |
|          | 0 = Sinking Current Mirror mode is disabled |
| Bit 3     | GENSRCEN0: Generated Source Enable for Output #0 bit(1) |
|          | 1 = Source generates the current source mirror reference |
|          | 0 = Source does not generate the current source mirror reference |
| Bit 2     | GENSNKEN0: Generated Sink Enable for Output #0 bit(1) |
|          | 1 = Source generates the current sink mirror reference |
|          | 0 = Source does not generate the current sink mirror reference |
| Bit 1     | SRCEN0: Source Enable for Output #0 bit |
|          | 1 = Current source is enabled |
|          | 0 = Current source is disabled |
| Bit 0     | SNKEN0: Sink Enable for Output #0 bit |
|          | 1 = Current sink is enabled |
|          | 0 = Current sink is disabled |

**Note 1:** When using Current Mirror mode, the corresponding SHRSRCENx or SHRSNKENx bit must be enabled on the master channel as well as all channels sharing the reference.
3.0 MODULE APPLICATION

3.1 Module Description

The CBG module consists of two classes of current sources: the 10 µA current source and the 50 µA current source.

The 10 µA current source is a general purpose, sourcing only current. This current source can be used to generate voltages with an external resistor (refer to Figure 3-1), or to provide biasing to external circuitry or sensors.

The 50 µA current source's intended use is to generate an offset voltage to shift an external signal to be within the input range of the internal analog peripherals, such as the ADC. Shifting the input voltage maintains the dynamic range of the AC component of the input signal, but removes the offset voltage. An external resistor (refer to Figure 3-3 and Figure 3-4) is used in conjunction with the current source to develop the offset voltage. The offset can be either positive or negative, as needed by the application, to shift the input voltage into the usable range.

The 50 µA source is capable of operating in a Current Mirror mode with two or more sources. This mode can be used to generate offset voltages for differential signals (refer to Figure 3-5).

<table>
<thead>
<tr>
<th>Note 1:</th>
<th>Due to the small generated currents, the external resistors are large. This large resistor value protects the device input circuitry by limiting the current injected into the device when the current source is not enabled.</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:</td>
<td>Both classes of current sources can be externally paralleled by connecting the output pins together to increase current.</td>
</tr>
<tr>
<td>3:</td>
<td>It is possible to enable the 50 µA Current Source Sinking and Sourcing modes at the same time. This will not damage the device, but does increase current consumption. In this configuration, only a negligible current will be sourced or sunk by the pin associated with the current source.</td>
</tr>
<tr>
<td>4:</td>
<td>The large resistors used to create the voltage offset may exceed the ADC input impedance specification. To meet the ADC input requirements, one or more of the following may be required:</td>
</tr>
<tr>
<td></td>
<td>• Increase in sampling time.</td>
</tr>
<tr>
<td></td>
<td>• Use of an internal amplifier, such as an op amp or PGA.</td>
</tr>
<tr>
<td></td>
<td>• Use of a small capacitor on the input pin if the input signal does not change quickly.</td>
</tr>
<tr>
<td></td>
<td>• Use of an AC bypass capacitor.</td>
</tr>
</tbody>
</table>
3.2 Basic Operation of the 10 µA Source

The primary application of this source is to generate current to create an external voltage. This voltage can then be measured with the internal ADC or used to bias external circuitry. This class of source can only supply (source) current. To generate an external voltage, an external resistor is connected between the current source pin and AVss (refer to Figure 3-1). The current flow generates a voltage across the RSHIFT resistor (refer to Equation 3-1 and Example 3-1). Multiple sources can be paralleled, as needed, to increase current. This voltage can then be measured by the internal ADC or external circuitry.

**Figure 3-1: 10 µA Current Source**

![10 µA Current Source Diagram](image)

**Equation 3-1: Equation for Determining the Value of RSHIFT**

\[ V(REXT) = 10 \mu A \times REXT \]

**Note:** \( V(REXT) \) should not exceed \( AVDD - 0.5V \) typical (see Section 3.3.6 “Operating Range”).

**Example 3-1: Enabling a 10 µA Source**

\( REXT = 10 \text{ kOhms, } AVDD = 3.3V \)
\( VPIN = 10k \times 10 \mu A = 100 \text{ mV} \)
\( VREXT << 3.3V - .5V, \text{ and therefore, meets the } V(REXT) \text{ requirement} \)

```c
// User code to enable a 10ua source
BIASCONbits.ON = 1; // enable the module
BIASCONbits.I10EN0 = 1; // enable 10ua source channel 0
```
3.3 Basic Operation of the 50 µA Source

The primary application of the 50 µA current source is to remove the DC offset so that the signal to be measured is within the ADC module’s input range. Figure 3-2 shows a typical signal to be measured: an AC signal with a DC offset. This class of current source can be used to create a positive or negative shift with an external resistor. The following examples show the basic configurations for shifting the input voltage and the required calculations. The equations in Equation 3-2 are used for positive and negative voltage shift calculations.

Equation 3-2: Equation for Determining the Value of RSHIFT

\[
R_{SHIFT} = \frac{V_{SHIFT}}{50 \, \mu A}
\]

\[
V_{SHIFT} = V_{IN}^{DC} - \left(\frac{V_{IN}^{AC}}{2}\right)
\]

Note: \(V(R_{SHIFT})\) should not exceed \(AVDD - 0.7\)V typical (see Section 3.3.6 “Operating Range”).

Figure 3-2: AC Signal Component with a DC Offset
3.3.1 VOLTAGE SHIFTING FOR A POSITIVE INPUT VOLTAGE

To shift a positive input voltage, a single CBG source is used. The source is used to generate a negative voltage to offset the input signal. Refer to Figure 3-3. Equation 3-1 shows the calculations and configuration for this application.

**Figure 3-3: Single-Ended Positive Voltage Shift**

**Example 3-2: Single-Ended Positive Voltage Shift**

3V p-p Signal with a -24V Offset:

- $V_{min} = -24V - (3V / 2) = -25.5V$
- $V_{max} = -24V + (3V / 2) = -22.5V$
- $V_{shift} = |V_{min}|$
- $R_{shift} = 25.5V / 50\mu A = 510k Ohm$

standard 5% value is 510k Ohm  
standard 1% value is 511k Ohm  
Shift with standard value resistor is 511k * 50\mu A = 25.55V$

- $V_{input range} = (V_{max} - V_{shift}) - (V_{min} - V_{shift})$
- $V_{input range} = (49.5V - 46.5V) - (46.5V - 46.5V) = 3V$

// sample code to enable 50\mu A current sink.  
BIASCONbits.ON = 1; // enable the module  
IBIASCONLbits.SNKEN1 = 1; // enable 50ua sink channel 1
3.3.2 VOLTAGE SHIFTING FOR A NEGATIVE INPUT VOLTAGE

To shift a negative input voltage, a single CBG source is used. The source is used to generate a positive voltage to offset the input signal (refer to Figure 3-4). Example 3-3 shows the calculations for this configuration.

**Figure 3-4: Single-Ended Negative Voltage Shift**

![Figure 3-4: Single-Ended Negative Voltage Shift](image)

**Example 3-3: Single Ended Negative Voltage Shift**

Input Device Operating at 3.3V, Signal is 3V p-p with a 48V DC Offset, Desired Input to ADC: 0V to 3V

**Note:** Offset will be negative so the current source must sink current to remove the offset.

3V p-p signal with a 48V offset

\[
\begin{align*}
V_{\text{Vin min}} &= 48V - (3V / 2) = 46.5V \\
V_{\text{Vin max}} &= 48V + (3V / 2) = 49.5V \\
V_{\text{Shift}} &= |V_{\text{Vin min}}| \\
R_{\text{Shift}} &= 46.5V / 50\mu A = 930k \text{ Ohm} \\
\text{standard 1% value is 931k Ohm} \\
\text{Shift with standard value resistor is 931k} \times 50\mu A = 46.55V \\
\text{input range} &= (V_{\text{Vin max}} - V_{\text{Shift}}) - (V_{\text{Vin min}} - V_{\text{Shift}}) \\
&= (49.5V - 46.5V) - (46.5V - 46.5V) = 3V
\end{align*}
\]

// sample code to enable 50uA current sink.
BIASCOMbits.ON = 1;        // enable the module
IBIASCONLbits.SNKEN1 = 1;  // enable 50ua sink channel 1
3.3.3 CURRENT MIRRORING AND DIFFERENTIAL INPUTS

The 50 µA source is capable of operating in a Current Mirror mode. Current Mirroring mode connects two or more sources together and uses the current through the reference source to set the current through other sources. This mode is used when the current matching between the sources is important, for example, when shifting differential voltages.

Current Mirroring mode requires one source to be configured as the reference source by setting its GENSRCENx bit for sourcing or setting the GENSNKENx bit for sinking current. Enabling the SHRSRCENx bit for sourcing or the SHRSNKENx bit for sinking configures a source to use the reference source to set its current. Multiple sources can share a reference. The current mirror source and sink each have a single interconnect, therefore it is not possible to have multiple independent sets of mirrored sources for sinking or sourcing.

The current for the reference source is set by its RSHIFT resistor value (refer to Equation 3-3). The value of the RSHIFT resistors should be closely matched to reduce an unintended voltage offset.

To shift a differential input, two CBG sources are configured as a current mirror. The two sources are then used to generate negative offsets to remove the DC offset from the input signal. Refer to Figure 3-5 and Example 3-4.

Equation 3-3: Equation for Determining the Value of RSHIFT

\[ R_{SHIFT} = \frac{V_{SHIFT}}{50 \mu A} \]

Figure 3-5: Differential Voltage Shift

Note 1: Internal op amp or Programmable Gain Amplifier (PGA).
Example 3-4: Differential Voltage Shift

Shifting a Differential Voltage

Given:
Device Operating at 3.3V,
Input Signal: 0.5V Pk-Pk with a 12V DC Offset,
Desired Input to Amplifier: 0V to 0.5V

Note: Offset will be negative so the current source must sink current to remove the offset.

\[ V_{\text{IN(DC)}} = 12V - \left( \frac{0.5V}{2} \right) = 11.5V \]
\[ R_{\text{SET}} = \frac{(11.5V - 0.7V)}{50\mu A} = 216k \text{ Ohms} \]
Standard 1% value is 215k Ohm
Shift with standard value resistor is 215k * 50\mu A = 10.75V

\[ R_{\text{SHIFT}} = R_{\text{SET}} \]

// configure current sinks
IBIASCONHbits.GENSNKEN3 = 1; // configure as current mirror reference
IBIASCONHbits.SHRSNKEN3 = 1; // output reference current
IBIASCONHbits.SHRSNKEN2 = 1; // configure to use current mirror reference
BIASCONbits.ON = 1; // enable module
3.3.4 SHIFTING INPUT VOLTAGES AND ATTENUATING THE INPUT SIGNAL

For signals with an amplitude greater than the ADC input range, and also containing a DC offset, a voltage shift and a voltage divider are needed (refer to Figure 3-6). This combination allows the input signal to be scaled for the ADC input and removes the DC offset (refer to Equation 3-4).

**Equation 3-4: Determining Resistor Values for Input Scaling and Voltage Shifting**

\[
R_{SHIFT} = \frac{V_{SHIFT} - (R_{SHIFT} \times 50 \ \mu A) \times R_{ATTEN}}{R_{ATTEN} \times R_{SHIFT}}
\]

**Figure 3-6: 80V with 6V Pk-Pk Signal**

**Note 1:** Internal op amp or Programmable Gain Amplifier (PGA).
3.3.5 SETTING THE OUTPUT CURRENT

In Current Mirror mode, the mirror current is set by the RSHIFT resistor connected to the reference source. The value of this resistor is calculated with the formula in Equation 3-5 and Example 3-5. If a different current is desired, the 50 µA current value in the equation can be replaced by the desired current and the resulting resistor value calculated. The typical range of operation is 5 µA to 50 µA. The mirrored channels should use the same resistor value as was calculated for the reference source.

Equation 3-5: Setting the Output Current

\[
R_{\text{EXT}} = \frac{(AVDD - V_{\text{TH (typ)}})}{I}
\]

The resulting generated voltage should be less than:

\[V_{DD} - 0.7V\]

(refer to Section 3.3.6 “Operating Range”)

Example 3-5: Setting the Output Current

Desired Current: 25 µA

\[
R_{\text{EXT}} = \frac{(3.3V - 0.7V)}{25\mu A} = 104 \text{ kOhms}
\]

Closest standard value is 105 kOhms.

3.3.6 OPERATING RANGE

The maximum voltage that can be developed across a resistor driven by a current source depends on AVDD and the other voltage sources in the circuit.

When the resistor is connected to AVSS, such as seen in Figure 3-1, the maximum voltage that can be developed is approximately AVDD. However, when the developed voltage is greater than the current source’s internal threshold, the output current is reduced. To prevent this, the maximum developed voltage across REST + REXT should be limited to AVDD – 0.5V (typical) for the 10 µA source and AVDD – 0.7V (typical) for the 50 µA source.

3.3.7 ADC INPUT CONSIDERATIONS

The input impedance for the ADC determines the required change time, specified in ADC clocks or TAD. The impedance consists of the following internal resistances, the ADC channel select switch and RESD, as well as any external resistance. The large external resistor values required to generate offsets may violate the device’s ADC input specifications. This may require the use of an internal amplifier op amp or PGA to isolate the ADC from the large resistance.
3.4 Device Pin ESD Configuration

Devices have multiple ESD resistors on each pin (refer to Figure 3-1 and Figure 3-3). The ADC and other analog peripherals (not shown), each have separate ESD resistors. With this configuration, the voltage measured by the ADC does not include the voltage across the current source’s ESD resistor.

3.5 Interrupts

The current source modules do not generate interrupts.

3.6 Operating in Power-Saving Modes

Both classes of current sources continue to operate in power save modes.

3.7 Effects of a Reset

A Reset forces module registers to their initial Reset values, disabling the current sources.
4.0 RELATED APPLICATION NOTES

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the dsPIC33/PIC24 device families, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to the Current Bias Generator (CBG) module are:

<table>
<thead>
<tr>
<th>Title</th>
<th>Application Note #</th>
</tr>
</thead>
<tbody>
<tr>
<td>No related application notes at this time.</td>
<td>N/A</td>
</tr>
</tbody>
</table>

**Note:** Visit the Microchip web site ([www.microchip.com](http://www.microchip.com)) for additional application notes and code examples for the dsPIC33/PIC24 device families.
5.0 REVISION HISTORY

Revision A (March 2016)
This is the initial version of this document.
Note the following details of the code protection feature on Microchip devices:

• Microchip products meet the specification contained in their particular Microchip Data Sheet.

• Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

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