Errata Description

The following is a known problem in revision R and prior of the AT89S8253 in SPI communication:

During a master-slave SPI communication, whenever the SS input pin of the AT89S8253 acting as the slave device is pulled high during a transmission cycle, the internal SPI bit counter of the (slave) AT89S8253 does not get reset. If SS goes high during a data transfer, all subsequent data will be corrupted in the slave. If SS goes high in between transfers, the data remains unaffected.

Workarounds:

1. Perform a hardware reset.

or

2. Clear and then set the SPE bit in the SPCR register of the (slave) AT89S8253.