Next-generation LIN System Basis Chip with HV Switch Interface

Daniel Yordanov, Berthold Gruber

The LIN (Local Interconnect Network) bus is a vehicle bus standard used within the latest automotive network architectures and extends the portfolio of automotive electrical networks now available. The low-cost, single-wire serial communication system for distributed electronics in vehicles is highly suited to body control applications, including power windows, mirrors, smart wipers, door locks, seat/roof/lighting control, lamps and indicators, dashboard instruments, steering wheels, climate and air-conditioning (HVAC) systems, motors, switch panels and sensors.

It is mainly used as a cost-effective sub-network of a CAN bus to integrate intelligent sensor devices or actuators where the LIN master node also acts as a gateway to connect the LIN bus with the corresponding CAN bus.

Going hand in hand with rapid LIN market growth, the requirements for greater system efficiency and lower costs exerted on LIN products have continued to increase as well.
As a result of the ever growing number of in-vehicle electronic systems, the number of switches for controlling various applications is also increasing. Applications with switches located far away from the control electronics and wires integrated within the wiring harness need to have high-voltage switches.

The next-generation Atmel® ATA6641/42 System Basis Chip (SBC) with an eight-channel high-voltage switch interface, a LIN2.1 and SAEJ2602-2-compliant LIN transceiver, low-drop voltage regulator and an adjustable window watchdog enables the development of inexpensive, low-end, but also powerful slave and master nodes for LIN bus systems meeting the latest OEM requirements.

Due to its optimized architecture, the ATA6641/42 offers a high degree of flexibility for deployment in various applications such as switch connection through the wiring harness, port/contact monitoring, contact cleaning, switches (towards GND or VBAT) and LED/relay/power transistor control.

The block diagram (see figure 2) depicts the basic structure of the ATA6641/42.

Two versions are available: the ATA6641 with a 3.3V voltage regulator and the ATA6642 with a 5V voltage regulator. The voltage regulator delivers up to 80mA load current. Sleep mode and active low-power mode guarantee very low current consumption even in the case of a floating bus line or a short circuit on the LIN bus to GND. To maintain very low current consumption in sleep mode, a special technique ensures that the circuit switches back to sleep mode after approximately 10ms if the bus line is floating or in case of a short circuit.

Improved slope control at the LIN driver ensures secure data communication of up to 20kBaud. Data rates of up to 250kBaud also enable high-speed data communication.

Most features can be configured via the SPI. This 16-bit SPI interface simplifies and speeds up configuration of the slave/master LIN node for any given application.

Figure 3 shows a typical application using the ATA6641/42.

The ATA6641/4/1’s switch interface unit consists of eight high-side current sources. They deliver a constant current level derived from a reference value measured at the IREF pin. This pin is voltage stabilized (V_{REF} = 1.23V typ.) so that the reference current is directly dependent on the externally applied resistor connected between IREF pin and ground. The resulting current at the CSx pins is \( (V_{\text{REF}} = 1.23V) \times r_{\text{CS}} \). For example, with a 12K resistor between IREF and GND the value of the current at the CSx pins is 10mA (assumed IMUL = 0 => r_{CS,H} = 100). Failsafe measures are able to detect both a missing as well as a short-circuited resistor. If a resistor
is short-circuited, an internally generated reference current $I_{\text{REFS}}$ is used to maintain a basic level of functionality.

Each switch input has a high-voltage comparator, a state-change-detection register for wake-up, interrupt request generation and a voltage divider with a low-voltage output that can be fed through to the measurement pin VDIV.

**Switch Control**

Eight high-voltage I/O ports form the heart of the ATA6641/42 and make it exceptionally well suited for switch control applications with higher ESD requirements. These I/O ports allow highly flexible control of up to eight single switches or a switch matrix or any combinations of both, as shown in figure 5, supplied by an internal current source of from 5mA to 25mA. Three I/O ports can be configured either as current sources (e.g., for switches toward ground) or as current sinks (e.g., for switches toward battery); the other five pins have current sourcing capability only. The I/O interface is shown in figure 4.

The device’s flexible switch monitoring is controlled by the application’s microcontroller. The implemented state-change-detection circuitry allows configuration of each input so that it triggers an interrupt upon state change even during low-power mode. Therefore the respective current source needs to be configured so that it is controlled via the CSPWM pin. A rising edge on this pin enables the current source and delivers a stable switch read-back signal at the CS pin; a falling edge updates the switch state. A change of state generates an interrupt request. If no wake-up should occur on a given switch—either because there is no application demand for this, or due to a failure, e.g., a hanging switch or a shorted connection line—wake-up can be prevented by disabling the current source in the SPI configuration register.

If switches are placed outside and connected via a wiring harness to the ECU, complete diagnosis of short-circuits or cable breaks can be performed. Ports that are not used for switch detection can be switched off.

The device also features a high-precision current source for multi-resistor coding. The scan current through the switches can be chosen to be sufficiently high so that the current will clean the switches.

**Voltage Measurement**

The I/O ports not only contain a high-voltage (HV) comparator for simple switches but also a voltage divider. The low-voltage signal—which is linearly dependent on the input voltage—is provided at the VDIV pin to enable analog voltage measurements on the high-voltage pins by using the ADC of the application’s microcontroller.

The VDIV pin—which can be sourced either by the VBATT pin or one of the switch input pins CS1 to CS8—guarantees a voltage and temperature-stable output ratio of the selected input.
PWM Control

The ATA6641/42’s switch interface current sources can be used to directly control pulse-width-modulated loads (such as LEDs). The PWM signal applied to the CSPWM input pin is used as control signal for the chosen current sources at the corresponding I/O ports. This PWM signal can be applied to each I/O pin.

The CSPWM input pin accepts logic-level signals (such as those from the microcontroller) and is equipped with a pull-down structure so that, in case of an open connection, this input is well defined.

H-bridge Relay Control

The ATA6641/42 can be used as a relay driver. If the 20mA output current of each I/O-port is not sufficient to drive the load, it is possible to connect the output pins together to achieve a higher load current. In the example shown in figure 8 three outputs are tied together. This results in a minimum output current of 3 x 20mA = 60mA.

As an additional safety feature, the CS1 and CS2 high-voltage interface pins are used as sensor inputs for checking proper relay operation. The relays are configured as H-bridges, allowing a motor to be driven in both directions. A typical application for this configuration is a window lifter.

LIN Auto-addressing

After switching on the network, and before the communication begins, each LIN slave node will be assigned a unique address. Typically this address is implemented by hardwiring, programming (OTP or bitwise), special connectors, or DIP switches. Common to all the methods mentioned is the configuration of the system or the replacement of a faulty slave node requires manual action. The only way to avoid the latter is to store the slave nodes using different addresses.

In contrast to these methods, auto-addressing means that completely identical slave nodes can be connected to the LIN network without having to distinguish their addresses. The addresses of the individual nodes are assigned according to their position on the bus.

Another solution is an automatic addressing process called slave node position detection. In this case, the master assigns
the node addresses of the slaves during initialization. As all LIN nodes are in a wired AND connection, all bus connections are equal and thus not able to detect their position on the bus on their own. Additional measures are required to detect the relative position of every slave on the bus.

The list below describes various methods for achieving this solution:

1. Addressing with an additional current source and a resistor inside the plug: with different resistors required at every slave node, they are therefore not identical
2. Bus shunt method: a shunt resistor is inserted into the bus line at each slave
3. A switch is implemented at every slave node between two LIN transceivers
4. Addressing by DIP switches: this requires manual setting of the switches
5. Plug method: this involves an additional connector in the plug and at the slaves; coded connections are done by the plug
6. Extra wire daisy chain method

The ATA6641/42 is perfectly suited for the extra wire daisy chain method because the two high-voltage I/O ports can be used as a high-side and low-side switch. Figure 9 shows the basic functionality of this method using the ATA6641/42.

This method allows absolutely identical LIN slaves to be connected to the LIN bus without end-of-line or connector-pin programming. All LIN slaves need to provide two extra pins; in the case of the ATA6641/42 these are the high-voltage I/O CS1 and CS2 ports. Both are able to switch to VS or to GND. The CS1 pin is the data input, and the CS2 pin is the data output. The CS1 data input of the first slave node is connected to the data output of the master. The output of the first node CS2 is connected to the input CS1 of the second node and so on, resulting in a daisy chain. The addressing procedure starts with all outputs (CS2) set to high level with the exception of the master. This means that the first slave node following the master node is detected by a low level at its data input. The first node selected in this way takes the address from the LIN configuration message from the master. This first slave node switches its data output CS2 to GND and the second slave node thus has a low level at its CS1 data input. The second slave node then takes the address from the LIN configuration message and switches its output CS2 to GND. These steps are repeated until all slave nodes have an address.

Figure 10 demonstrates this method with an ambient light control application using the ATA6641/42.