Features

- Low Threshold
- High Input Impedance
- 110 pF Maximum Low-Input Capacitance
- Fast Switching Speeds
- Low On-Resistance
- Free from Secondary Breakdown
- Low Input and Output Leakage

Applications

- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Battery-Operated Systems
- Photovoltaic Drives
- Analog Switches
- General Purpose Line Drivers
- Telecommunication Switches

General Description

The TN2501 low-threshold Enhancement-mode (normally-off) transistor uses a vertical Diffusion Metal Oxide Semiconductor (DMOS) structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in Metal-Oxide Semiconductor (MOS) devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

Microchip’s vertical DMOS Field-Effect Transistors (FETs) are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance and fast switching speeds are desired.

Package Type

See Table 3-1 for pin information.
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage .................................................................................................................. BV_DSS
Drain-to-Gate Voltage ..................................................................................................................... BV_DGS
Gate-to-Source Voltage .................................................................................................................... ±20V
Operating Ambient Temperature, T_A .............................................................................................. –55°C to +150°C
Storage Temperature, T_S ................................................................................................................ –55°C to +150°C

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-to-Source Breakdown Voltage</td>
<td>BV_DSS</td>
<td>18</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>VGS = 0V, ID = 1 mA</td>
</tr>
<tr>
<td>Gate Threshold Voltage</td>
<td>VGS(th)</td>
<td>0.3</td>
<td>—</td>
<td>1</td>
<td>V</td>
<td>VGS = VDS, ID = 1 mA</td>
</tr>
<tr>
<td>Change in VGS(th) with Temperature</td>
<td>∆VGS(th)</td>
<td>—</td>
<td>—</td>
<td>–4</td>
<td>mV/°C</td>
<td>VGS = VDS, ID = 1 mA (Note 1)</td>
</tr>
<tr>
<td>Gate Body Leakage Current</td>
<td>IGSS</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>nA</td>
<td>VGS = ±15V, VDS = 0V</td>
</tr>
<tr>
<td>Zero-Gate Voltage Drain Current</td>
<td>IDSS</td>
<td>—</td>
<td>—</td>
<td>10</td>
<td>μA</td>
<td>VGS = 0V, VDS = Maximum rating</td>
</tr>
<tr>
<td>On-State Drain Current</td>
<td>ID(ON)</td>
<td>250</td>
<td>600</td>
<td>—</td>
<td>mA</td>
<td>VGS = VDS = 3V</td>
</tr>
<tr>
<td>Static Drain-to-Source On-State Resistance</td>
<td>RDS(ON)</td>
<td>—</td>
<td>25</td>
<td>3.5</td>
<td>Ω</td>
<td>VGS = 1.2V, ID = 3 mA</td>
</tr>
<tr>
<td>Change in RDS(ON) with Temperature</td>
<td>∆RDS(ON)</td>
<td>—</td>
<td>0.75</td>
<td>%/°C</td>
<td>VGS = 3V, ID = 200 mA (Note 1)</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Specification is obtained by characterization and is not 100% tested.
### AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications:** \( T_A = 25^\circ \text{C} \) unless otherwise specified. All AC parameters are sample tested.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Forward Transconductance</td>
<td>( G_{FS} )</td>
<td>150</td>
<td>300</td>
<td>—</td>
<td>mmho</td>
<td>( V_{DS} = 3 \text{V}, , I_D = 200 \text{mA} )</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>( C_{ISS} )</td>
<td>—</td>
<td>—</td>
<td>110</td>
<td>pF</td>
<td>( V_{DS} = 0 \text{V}, , V_{GS} = 15 \text{V}, , f = 1 \text{MHz} )</td>
</tr>
<tr>
<td>Common Source Output Capacitance</td>
<td>( C_{DSS} )</td>
<td>—</td>
<td>—</td>
<td>60</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Reverse Transfer Capacitance</td>
<td>( C_{RSS} )</td>
<td>—</td>
<td>—</td>
<td>35</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Turn-On Delay Time</td>
<td>( t_{d(ON)} )</td>
<td>—</td>
<td>—</td>
<td>5</td>
<td>ns</td>
<td>( V_{DD} = 15 \text{V}, , I_D = 250 \text{mA}, , R_{GEN} = 25 \Omega )</td>
</tr>
<tr>
<td>Rise Time</td>
<td>( t_r )</td>
<td>—</td>
<td>—</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-Off Delay Time</td>
<td>( t_{d(OFF)} )</td>
<td>—</td>
<td>—</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Fall Time</td>
<td>( t_f )</td>
<td>—</td>
<td>—</td>
<td>8</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

### DIODE PARAMETER

- **Diode Forward Voltage Drop**
  \( V_{SD} \): 1.1 V to 1.8 V, \( V_{GS} = 0 \text{V}, I_{SD} = 200 \text{mA} \)  
  (Note 1)

- **Reverse Recovery Time**
  \( t_{rr} \): 100 ns, \( V_{GS} = 0 \text{V}, I_{SD} = 200 \text{mA} \)

**Note 1:** All DC parameters are 100% tested at 25°C unless otherwise stated.  
(Pulse test: 300 µs pulse, 2% duty cycle)

### TEMPERATURE SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEMPERATURE RANGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Ambient Temperature</td>
<td>( T_A )</td>
<td>—55</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>( T_S )</td>
<td>—55</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>PACKAGE THERMAL RESISTANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3-lead SOT-89</td>
<td>( \theta_{JA} )</td>
<td>—</td>
<td>133</td>
<td>—</td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

### THERMAL CHARACTERISTICS

- **Package**
  - 3-lead SOT-89

<table>
<thead>
<tr>
<th>Package</th>
<th>( I_D ) (Note 1) (Continuous) (mA)</th>
<th>( I_D ) (Pulsed) (mA)</th>
<th>Power Dissipation at ( T_A = 25^\circ \text{C} ) (Note 2) (W)</th>
<th>( I_{DR} ) (Note 1) (mA)</th>
<th>( I_{DRM} ) (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3-lead SOT-89</td>
<td>400</td>
<td>560</td>
<td>1.6</td>
<td>400</td>
<td>560</td>
</tr>
</tbody>
</table>

**Note 1:** \( I_D \) (continuous) is limited by maximum rated \( T_J \).  
**Note 2:** \( T_A = 25^\circ \text{C} \). Mounted on an FR4 Board, 25 mm x 25 mm x 1.57 mm.
2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

**FIGURE 2-1:** Output Characteristics.

**FIGURE 2-2:** Transconductance vs. Drain Current.

**FIGURE 2-3:** Maximum Rated Safe Operating Area.

**FIGURE 2-4:** Saturation Characteristics.

**FIGURE 2-5:** Power Dissipation vs. Ambient Temperature.

**FIGURE 2-6:** Thermal Response Characteristics.
FIGURE 2-7: $B_{V_{DSS}}$ Variation with Temperature.

FIGURE 2-8: Transfer Characteristics.

FIGURE 2-9: Capacitance vs. Drain-to-Source Voltage.

FIGURE 2-10: On-Resistance vs. Drain Current.

FIGURE 2-11: $V_{(th)}$ and $R_{DS}$ Variation with Temperature.

FIGURE 2-12: Gate Drive Dynamic Characteristics.
3.0 PIN DESCRIPTION

The details on the pins of TN2501 are listed on Table 3-1. Refer to Package Type for the location of pins.

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Gate</td>
<td>Gate</td>
</tr>
<tr>
<td>2</td>
<td>Drain</td>
<td>Drain</td>
</tr>
<tr>
<td>3</td>
<td>Source</td>
<td>Source</td>
</tr>
</tbody>
</table>
4.0  FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TN2501.

![Switching Waveforms and Test Circuit](image)

**FIGURE 4-1:**  Switching Waveforms and Test Circuit.

**TABLE 4-1:**  PRODUCT SUMMARY

<table>
<thead>
<tr>
<th>$BV_{DSS}/BV_{DGS}$ (V)</th>
<th>$R_{DS(ON)}$ (Maximum) (Ω)</th>
<th>$I_{D(ON)}$ (Minimum) (mA)</th>
<th>$V_{GS(TH)}$ (Maximum) (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>18</td>
<td>2.5</td>
<td>250</td>
<td>1</td>
</tr>
</tbody>
</table>
## 5.0 PACKAGING INFORMATION

### 5.1 Package Marking Information

**Legend:**

- **XX...X**  
  Product Code or Customer-specific information
- **Y**  
  Year code (last digit of calendar year)
- **YY**  
  Year code (last 2 digits of calendar year)
- **WW**  
  Week code (week of January 1 is week ‘01’)
- **NNN**  
  Alphanumeric traceability code
- **Pb-free JEDEC® designator for Matte Tin (Sn)**

- **edis**
  This package is Pb-free. The Pb-free JEDEC designator (edis)
  can be found on the outer packaging for this package.

**Example:**

- 3-lead SOT-89
  - XXXYYWW
  - NNN
  - TN5U855
  - 398

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.
3-Lead TO-243AA (SOT-89) Package Outline (N8)

![Diagrams of Top View and Side View of the package outline.

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>A</th>
<th>b</th>
<th>b1</th>
<th>C</th>
<th>D</th>
<th>D1</th>
<th>E</th>
<th>E1</th>
<th>e</th>
<th>e1</th>
<th>H</th>
<th>L</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIN</td>
<td>1.40</td>
<td>0.44</td>
<td>0.36</td>
<td>0.35</td>
<td>4.40</td>
<td>-</td>
<td>2.90</td>
<td>-</td>
<td>2.00</td>
<td>-</td>
<td>1.50</td>
<td>BSC</td>
</tr>
<tr>
<td>NOM</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1.50</td>
<td>BSC</td>
</tr>
<tr>
<td>MAX</td>
<td>1.60</td>
<td>0.56</td>
<td>0.48</td>
<td>0.44</td>
<td>4.60</td>
<td>1.83</td>
<td>2.60</td>
<td>2.29</td>
<td>1.05</td>
<td>0.73</td>
<td>3.94</td>
<td>0.73</td>
</tr>
</tbody>
</table>

† This dimension differs from the JEDEC drawing.

Drawings not to scale.
APPENDIX A: REVISION HISTORY

Revision A (May 2018)

• Converted Supertex Doc# DSFP-TN2501 to Microchip DS20005948A
• Changed the package marking format
• Added some sections to comply with Microchip formatting standards
• Made minor text changes throughout the document
**PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>XX</th>
<th>Package Options</th>
<th>Environmental</th>
<th>Media Type</th>
<th>Example:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device:</td>
<td>TN2501 = N-Channel Enhancement-Mode Vertical DMOS FET</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package:</td>
<td>N8 = 3-lead SOT-89</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Environmental:</td>
<td>G = Lead (Pb)-free/RoHS-compliant Package</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Media Type:</td>
<td>(blank) = 2000/Reel for an N8 Package</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

a) TN2501N8-G: N-Channel Enhancement-Mode, Vertical DMOS FET, 3-lead SOT-89, 2000/Reel
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Fax: 44-118-921-5820  

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