General Description

The SY88149NDL/349NDL evaluation board enables fast and thorough evaluation of the SY88149NDL/349NDL burst mode limiting post amplifiers.

The board is an easy-to-use, single-supply design, engineered to be driven by a high-speed pattern generator and intended to terminate to a 50Ω scope.

The board features simple user adjustability of the LOS threshold through the adjustment of an on-board potentiometer and different setting option selections using jumpers.

The SY88149NDL and SY88349NDL are part of Micrel’s industry leading burst mode family of ultra-small high speed fiber optic ICs for GEPON/GPON applications.

Datasheets and support documentation are available on Micrel’s web site at: www.micrel.com or by contacting Micrel sales and field applications support team.

Features

- <5ns SD_Assert (LOS_De-assert) time
- AUTO RESET or manual RESET LOS/SD output
- Selectable LOS/SD output option
- High-sensitivity LOS/SD signal detect
- Low-noise LVPECL (149) and CML (349) data outputs
- Squelching function to maintain output stability
- Programmable LOS/SD level set (LOS/SD_LVL)
- Selectable noise discriminator to filter input signal and reduce LOS/SD false triggering
- 5mVpp input sensitivity
- 1.25Gbps (149) and 2.5Gbps (349) operation
- Single 3.3V power supply
- Available in a 3mm x 3mm 16-pin QFN package

Applications

- GEPON/GPON OLT
- Gigabit Ethernet
- Fibre Channel
- OC-3/12/24 SONET/SDH
- High-gain line driver and line receiver
- Low-gain TIA interface

Markets

- FTTx PON
- Datacom
- Telecom
- Optical transceivers
Evaluation Board

Install jumper to Enable ND if SD selected
Install jumper to Enable ND if LOS selected

LOS/SD_SEL:
Jumper between pins to the left or leave J8 open to select SD
Jumper between pins to the right to select LOS

/AUTORESET:
Connect to L to Enable
Connect to H or leave open to Disable

Ordering Information

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<tr>
<th>Part Number</th>
<th>PCB Revision</th>
<th>Description</th>
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<tr>
<td>SY88149ND-EVAL</td>
<td>SY88149/349HAL_Rev C</td>
<td>Evaluation board for 1Gbps burst mode limiting post amplifiers with ultra-fast signal assert timing.</td>
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<tr>
<td>SY88349ND-EVAL</td>
<td>SY88149/349HAL_Rev C</td>
<td>Evaluation board for 2.5Gbps burst mode limiting post amplifiers with ultra-fast signal assert timing.</td>
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Evaluation Board Description

The SY88149NDL/349NDL evaluation board is designed to operate with a single 3.3V ±10% power supply and is configured with AC-coupled inputs and outputs. The high-speed input and output signals are brought out to SMA connectors through matched-length AC-coupled differential traces.

AC-Coupled Input

The AC-coupled inputs are biased with the external 50Ω termination resistors to VREF pin.

AC-Coupled Output

The board is configured with AC-coupled outputs to interface directly with 50Ω load equipment inputs. If only one output is being used, the unused complimentary output must be terminated with 50Ω to ground.

Coupling Caps Selection

The RC time constant created by the coupling cap and the input termination resistor can cause a baseline DC droop if it's chosen too small for the data rate and if the data pattern contain long strings of consecutive identical digits (CID) or it can cause pattern-dependent jitter if the selected value is too large for the data rate. The coupling cap value should be chosen to get an optimized low frequency cutoff that minimizes the two problems together.

For burst mode applications, the low frequency cutoff should be high enough to support long strings of CID and low enough to assure a fast receiver settlement time to avoid errors during transitions between bursts of different power levels. As detailed in the application note, the solution consists of using two low-frequency cutoff frequencies and a RESET pulse to switch between them. The latter option is not implemented in this evaluation board.

Measurements

Evaluating RXOUT+ and RXOUT-

1. Set a DC power supply to +3.3V and turn it off. Connect the positive lead to VCC post and the negative lead to GND post.
2. Connect the JAM input to the GND (without jumper on J12, connect the left pin to GND using a wire) to enable DOUT and /DOUT output buffers.
3. Set the desired frequency on a pattern generator with amplitude between 5mVpp and 1800mVpp. Typical data patterns are 2\(^{1-1}\) or 2\(^{23-1}\) PRBS patterns depending on the application. Because the inputs to the board are AC-coupled, the voltage offset of the pattern generator is not significant, so it can be set between GND and VCC.
4. Connect the pattern generator with differential outputs as a data source to the DIN and /DIN inputs on the SY88149NDL/349NDL evaluation board. Use matched length differential cables.
5. Turn the power supply on.
6. Observe DOUT and /DOUT outputs on a 50Ω input scope.

LOS/SD Timing Measurements

The board comes with 100nF coupling caps at the inputs and outputs. To minimize the effect of the input RC time, constant-on the signal delay from the SMA connectors to the input of the device, which may increase the measured LOS/SD assert/de-assert time, the caps must be replaced with lower value caps (100pF or lower).

LOS Hysteresis Measurements

The SY88149NDL/349NDL evaluation board provides a potentiometer (R9) to allow for convenient adjustment of LOS/SDLVL without the need for an extra power supply. LOS/SDLVL taps off a potentiometer connected between VCC and an internal reference voltage of approximately VCC-1.3V. Hence, LOS/SDLVL can be set to any voltage between VCC and VCC-1.3V, as specified in the SY88149NDL and SY88349NDL datasheets. The potentiometer creates a voltage divider. Thus, the LOS/SDLVL can be calculated by the following equation

\[
\text{LOS/SDLVL} = V_{\text{CC}} - \left(\frac{1.3 \times R}{R + 1.5}\right)
\]

where the value for R is kΩ.

R is the resistance of the potentiometer from VCC to the tap at LOS/SDLVL. The steps below show how to measure to LOS/SD hysteresis as a function of the input voltage swing at the DIN and /DIN inputs.

Minimum Input Swing Hysteresis Measurement

The minimum BER acceptable input swing for the SY88149NDL and SY88349NDL is 5mVpp.

1. Set a DC power supply to +3.3V and turn it off. Connect the positive lead to VCC post and the negative lead to GND post.
2. Connect the JAM input to the GND (without jumper on J12, connect the left pin to GND using a wire) to enable DOUT and /DOUT output buffers.
3. Connect a DMM or similar voltage measurement device between the LOS/SDLVL pin and VCC.
4. Connect a second DMM or similar voltage measurement device between the LOS output and GND. For the remainder of this document, this DMM will be referred to as the LOS DMM. To use a scope instead of the LOS DMM, disconnect JAM from GND and install jumper to set the squelch function and...
observe the output waveform (DOUT and/or /DOUT) on the scope instead of measuring LOS with DMM.

5. Connect the pattern generator with differential outputs as a data source to DIN and /DIN inputs on the evaluation board. Use matched length differential cables.

6. Turn the power supply on.

7. Adjust the trim pot R2 so the voltage at the LOS/SDLVL pin is around 1.3V below VCC. This sets the LOS/SDL for maximum sensitivity. At this level, the LOS/SDL output should go HIGH or LOW (as measured with the LOS DMM) as the input voltage swing at DIN and /DIN is adjusted up and down around 5mVpp.

8. Now adjust the trim pot to set the sensitivity to a desired level and lower the amplitude of the input signal until LOS is asserted HIGH, then increase the input signal until the LOS de-asserts LOW.

9. The hysteresis between the assert and de-assert levels can be calculated with the following equation where LOS-D is the LOS de-assert input level and LOS-A is the LOS assert input level. This hysteresis should be >3dB.

\[
\text{Hysteresis (dB)} = 20 \log_{10} \frac{\text{LOS} - D}{\text{LOS} - A}
\]

Eq. 2

/AUTORESET and Manual RESET Selection
To enable /AUTORESET, install a jumper between the central pin and pin “L” of J13. To disable /AUTORESET and use manual RESET instead, install jumper between the central pin and pin “H” or remove the jumper.

LOS or SD Selection
To select SD function on LOS/SD pin, install a jumper on J8 between the central pin and the pin to the left or leave J8 open. To select LOS function, install jumper on J8 between the central pin and the pin to the right.

Noise Discriminator (ND)
To enable the noise discriminator, install jumper on J15 when LOS is selected or install jumper on J14 if SD is selected.

LOS/SDLVL Adjust
To adjust LOS/SDLVL, install jumper on J9 and trim potentiometer R9.

Squelch Function
To enable the squelch function, connect LOS/SD output to JAM input by installing jumper on J12.
**Bill of Materials**

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<th>Item</th>
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<th>Manufacturer</th>
<th>Description</th>
<th>Qty.</th>
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<td>C5-16</td>
<td>C1005X7R1C104K050BC</td>
<td>TDK(1)</td>
<td>CAP CER 0.1µF 16V 10% X7R 0402</td>
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<tr>
<td>C3-4</td>
<td>C2012X8R1H104K125AA</td>
<td>TDK</td>
<td>CAP CER 0.1µF 50V 10% X8R 0805</td>
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<td>C1</td>
<td>C1005X5R0J106M050B</td>
<td>TDK</td>
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<td>J8-9, J12-15</td>
<td>TSW-103-07-S-S</td>
<td>Samtec(2)</td>
<td>0.1mil Center through hole terminal strip</td>
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<td>ERJ-2GE0R00X</td>
<td>Panasonic(3)</td>
<td>RES 0.0 OHM 1/10W JUMP 0402 SMD</td>
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<td>Johnson Components(6)</td>
<td>SMA End Launch Receptacle Connector</td>
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<td>U1</td>
<td>SY88149NDL/349NDL</td>
<td>Micrel, Inc.(7)</td>
<td>Burst mode limiting post amplifier</td>
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For SY88149NDL, add:

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<th>Description</th>
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<tr>
<td>C17-18</td>
<td>C1005X7R1C104K050BC</td>
<td>TDK</td>
<td>CAP CER 0.1µF 16V 10% X7R 0402</td>
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<td>R5-6, R11</td>
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<td>Panasonic</td>
<td>RES 49.9 OHM 1/10W 1% 0402 SMD</td>
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**Notes:**
1. TDK: [www.tdk.com](http://www.tdk.com).
TCG Support
Hotline: 1-408-955-1690
Email support: HBWHelp@micrel.com

Application Hints and Notes
For application notes on high-speed termination on high bandwidth FOM and clock synthesizer products, SONET jitter measurement, and other TCG products, visit Micrel's web site at www.micrel.com.