Features

- Precision 1:2, 800 mV LVPECL Fanout Buffer
- Guaranteed AC Performance over Temperature and Voltage:
  - \( >5 \text{ GHz } f_{\text{MAX}} \) (Clock)
  - \(<110 \text{ ps Rise/Fall Times}\)
  - \(<260 \text{ ps Propagation Delay}\)
  - \(<15 \text{ ps Max Skew}\)
- Low Jitter Design
  - 60 fs RMS Phase Jitter
- Accepts an Input Signal as Low as 100 mV
- Unique Input Termination and VT Pin Accepts DC- and AC-Coupled Differential Inputs (LVPECL, LVDS and CML)
- 800 mV (100k) LVPECL Output Swing
- 2.5V ±5% or 3.3V ±10% Power Supply Operation
- Industrial Temperature Range: \(-40^\circ \text{C} \text{ to } +85^\circ \text{C}\)
- Available in 16-Pin (3 mm x 3 mm) QFN Package

Applications

- All SONET and GigE Clock Distribution
- Fibre Channel Clock and Data Distribution
- Backplane Distribution
- High-End, Low Skew, Multiprocessor Synchronous Clock Distribution

General Description

The SY58012U is a 2.5V/3.3V precision, high-speed, fully differential 1:2 LVPECL fanout buffer. Optimized to provide two identical output copies with less than 15 ps of skew, the SY58012U can process clock signals as fast as 5 GHz or 5 Gbps data.

The differential input includes Microchip's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, (AC-coupled or DC-coupled) as small as 100 mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage (\(V_{\text{REF-AC}}\)) is provided to bias the VT pin. The outputs are 100k LVPECL compatible, with extremely fast rise/fall times guaranteed to be less than 110 ps.

The SY58012U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (\(-40^\circ \text{C} \text{ to } +85^\circ \text{C}\)). For applications that require faster rise/fall times, or greater bandwidth, consider the SY58013U 1:2 fanout buffer with 400 mV output swing, or the SY58011U 1:2 CML (400 mV) fanout buffer. The SY58012U is part of Microchip’s high-speed, Precision Edge® product line.

Package Type

SY58012U
3 mm x 3 mm QFN-16 (M)
(Top View)
Functional Block Diagram

```
IN  500Ω
VT  500Ω
/IN

VREF-AC

Q0  /Q0
Q1  /Q1
```
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Power Supply Voltage (V\textsubscript{CC}) ..................................................................................................................... –0.5V to +4.0V
Input Voltage (V\textsubscript{IN}) ....................................................................................................................................... –0.5V to V\textsubscript{CC}
LVPECL Output Current (I\textsubscript{OUT})
   Continuous ...................................................................................................................................................50 mA
   Surge ..........................................................................................................................................................100 mA
Termination Current (I\textsubscript{VT})
   Source or Sink on VT Pin.........................................................................................................................±100 mA
Input Current
   Source or Sink Current on IN, /IN ...............................................................................................................±50 mA
Reference Current (V\textsubscript{REF-AC})
   V\textsubscript{REF-AC} Current ........................................................................................................................................±1.5 mA
Storage Temperature Range (T\textsubscript{S}) ......................................................................................................–65°C to +150°C

Operating Ratings ††

Supply Voltage (V\textsubscript{CC}) .......................................................................................................................... +2.375V to +3.63V
Operating Temperature Range (T\textsubscript{A}) .....................................................................................................–40°C to +85°C

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
†† Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
## DC ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:** $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated. **Note 1**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Voltage Range</td>
<td>$V_{CC}$</td>
<td>2.375</td>
<td>—</td>
<td>3.63</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>Power Supply Current</td>
<td>$I_{CC}$</td>
<td>—</td>
<td>55</td>
<td>80</td>
<td>mA</td>
<td>No load, max. $V_{CC}$</td>
</tr>
<tr>
<td>Input HIGH Voltage $IN, /IN$</td>
<td>$V_{IH}$</td>
<td>$V_{CC} - 1.6$</td>
<td>—</td>
<td>$V_{CC}$</td>
<td>V</td>
<td><strong>Note 2</strong></td>
</tr>
<tr>
<td>Input LOW Voltage $IN, /IN$</td>
<td>$V_{IL}$</td>
<td>0</td>
<td>—</td>
<td>$V_{IH} - 0.1$</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>Input Voltage Swing $IN, /IN$</td>
<td>$V_{IN}$</td>
<td>0.1</td>
<td>—</td>
<td>1.7</td>
<td>V</td>
<td>See Figure 4-1</td>
</tr>
<tr>
<td>Differential Input Voltage Swing</td>
<td>$V_{DIFF_IN}$</td>
<td>0.2</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>See Figure 4-2</td>
</tr>
<tr>
<td>IN to VT Resistance</td>
<td>$R_{IN}$</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>Ω</td>
<td>—</td>
</tr>
<tr>
<td>Voltage from Input to VT</td>
<td>$V_{T_IN}$</td>
<td>—</td>
<td>—</td>
<td>1.28</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>Output Reference Voltage</td>
<td>$V_{REF_-AC}$</td>
<td>$V_{CC} - 1.3$</td>
<td>$V_{CC} - 1.2$</td>
<td>$V_{CC} - 1.1$</td>
<td>V</td>
<td>—</td>
</tr>
</tbody>
</table>

**Note 1:** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

**Note 2:** $V_{IH\_MIN}$ not lower than 1.2V.

## LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:** $V_{CC} = +2.5V \pm 5\%$ or $+3.3V \pm 10\%$, $R_L = 50\Omega$ to $V_{CC} - 2V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated. **Note 1**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output High Voltage $Q_0, /Q_01, Q_1, /Q_1$</td>
<td>$V_{OH}$</td>
<td>$V_{CC} - 1.145$</td>
<td>—</td>
<td>$V_{CC} - 0.895$</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>Output Low Voltage $Q_0, /Q_01, Q_1, /Q_1$</td>
<td>$V_{OL}$</td>
<td>$V_{CC} - 1.945$</td>
<td>—</td>
<td>$V_{CC} - 1.695$</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>Output Differential Swing $Q_0, /Q_01, Q_1, /Q_1$</td>
<td>$V_{OUT}$</td>
<td>550</td>
<td>800</td>
<td>—</td>
<td>mV</td>
<td>See Figure 4-1</td>
</tr>
<tr>
<td>Differential Output Voltage Swing $Q_0, /Q_01, Q_1, /Q_1$</td>
<td>$V_{DIFF_OUT}$</td>
<td>1100</td>
<td>1600</td>
<td>—</td>
<td>mV</td>
<td>See Figure 4-2</td>
</tr>
</tbody>
</table>

**Note 1:** The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
## AC ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:** $V_{CC} = +2.5\,\text{V} \pm 5\%$ or $+3.3\,\text{V} \pm 10\%$, $R_L = 50\,\Omega$ to $V_{CC} - 2\,\text{V}$; $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise stated. **Note 1**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Frequency</td>
<td>$f_{MAX}$</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>Gbps</td>
<td>NRZ (Data)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>GHz</td>
<td>$V_{OUT} \geq 400,\text{mV}$ (Clock)</td>
</tr>
<tr>
<td>Propagation Delay</td>
<td>$t_{PD}$</td>
<td>110</td>
<td>170</td>
<td>260</td>
<td>ps</td>
<td>$V_{IN} \geq 100,\text{mV}$</td>
</tr>
<tr>
<td>Channel-to-Channel Skew</td>
<td>$t_{CHAN}$</td>
<td>—</td>
<td>75</td>
<td>—</td>
<td>ps</td>
<td><strong>Note 3</strong></td>
</tr>
<tr>
<td>Part-to-Part Skew</td>
<td>$t_{SKEW}$</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>ps</td>
<td><strong>Note 3</strong></td>
</tr>
<tr>
<td>Additive Phase Jitter</td>
<td>$t_{JITTER}$</td>
<td>—</td>
<td>37</td>
<td>—</td>
<td>fs</td>
<td>622 MHz Integration Range: 12 kHz to 20 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>97</td>
<td>—</td>
<td></td>
<td>156.25 MHz Integration Range: 12 kHz to 20 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>167</td>
<td>—</td>
<td></td>
<td>100 MHz Integration Range: 12 kHz to 20 MHz</td>
</tr>
<tr>
<td>Output Rise/Fall Time</td>
<td>$t_r/t_f$</td>
<td>35</td>
<td>80</td>
<td>110</td>
<td>ps</td>
<td>20% to 80% at full swing</td>
</tr>
</tbody>
</table>

**Note 1:** High frequency AC parameters are guaranteed by design and characterization.

**Note 2:** Input-to-input skew is the difference in time from and input-to-output in comparison to any other input-to-output.

**Note 3:** Part-to-Part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.
### TEMPERATURE SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>$T_A$</td>
<td>–40</td>
<td>—</td>
<td>+85</td>
<td>°C</td>
<td>—</td>
</tr>
<tr>
<td>Lead Temperature</td>
<td></td>
<td>—</td>
<td>—</td>
<td>+260</td>
<td>°C</td>
<td>Soldering, 20 sec.</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_S$</td>
<td>–65</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td>—</td>
</tr>
</tbody>
</table>

**Package Thermal Resistances (Note 1)**

| Thermal Resistance, 3x3 QFN-16Lead      | θ_JA  | 60   | —    | —    | °C/W  | Still-air 500 lpfm       |
|                                         |       | 54   | —0   |      |       |                          |
|                                         | ψ_JB  | 33   | —    | —    | °C/W  | Junction-to-board        |

**Note 1:** Package thermal resistance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. $\psi_{JB}$ and $\theta_{JA}$ values are determined for a 4-layer board in still-air number, unless otherwise stated.
2.0  TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

\( V_{CC} = 3.3V \), \( GND = 0V \), \( V_{IN} = 400 \text{ mV} \), \( T_A = +25^\circ \text{C} \), unless otherwise stated.

**FIGURE 2-1:**  Frequency vs. Amplitude.

**FIGURE 2-2:**  Channel-To-Channel Skew vs. Temperature.

**FIGURE 2-3:**  Propagation Delay vs Input Voltage Swing.

**FIGURE 2-4:**  Propagation Delay vs Temperature.

**FIGURE 2-5:**  200 MHz Output.

**FIGURE 2-6:**  2.5 GHz Output.
FIGURE 2-7: 5 GHz Output.

FIGURE 2-8: 5 Gbps Output.
3.0 PHASE NOISE PLOTS

$V_{CC} = +3.3\, V$, $T_A = +25^\circ C$.

**FIGURE 3-1:** 100 MHz Phase Jitter, Device.

**FIGURE 3-2:** 100 MHz Phase Jitter, Source.
FIGURE 3-3: 156.25 MHz Phase Jitter, Device.

FIGURE 3-4: 156.25 MHz Phase Jitter, Source.
FIGURE 3-5: 622 MHz Phase Jitter, Device.

FIGURE 3-6: 622 MHz Phase Jitter, Source.
4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 4</td>
<td>IN, /IN</td>
<td>Differential Input: This input pair is the signal to be buffered. Each pin of this pair internally terminates with 50Ω to the VT pin. Note that this input will default to an indeterminate state if left open. See Section 5.0 “Input Interface Applications”.</td>
</tr>
<tr>
<td>2</td>
<td>VT</td>
<td>Input Termination Center-Tap: Each input terminates to this pin. The VT pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See Section 5.0 “Input Interface Applications”.</td>
</tr>
<tr>
<td>3</td>
<td>VREF_AC</td>
<td>Reference Output Voltage: This output biases to VCC – 1.2V. It is used when AC-coupling the inputs (IN, /IN). Connect VREF_AC directly to the VT pin. Bypass with 0.01 μF low ESR capacitor to VCC. Maximum current source or sink is 0.5 mA. See Section 5.0 “Input Interface Applications”.</td>
</tr>
<tr>
<td>5, 8, 13, 16</td>
<td>VCC</td>
<td>Positive Power Supply: Bypass with 0.1 μF//0.01 μF low ESR capacitors. 0.01 μF capacitor should be as close to VCC pin as possible.</td>
</tr>
<tr>
<td>12, 11, 9, 10</td>
<td>Q0, /Q0 Q1, /Q1</td>
<td>LVPECL Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 800 mV. Unused output pairs may be left floating with no impact on jitter. See Section 6.0 “LVPECL Output Applications”.</td>
</tr>
<tr>
<td>6, 7, 14, 15</td>
<td>GND, Exposed Pad</td>
<td>Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.</td>
</tr>
</tbody>
</table>
Single-Ended and Differential Swings

![Single-Ended Voltage Swing](image1)

**FIGURE 4-1:** Single-Ended Voltage Swing.

![Differential Voltage Swing](image2)

**FIGURE 4-2:** Differential Voltage Swing.

Timing Diagram

![Timing Diagram](image3)

**FIGURE 4-3:** Simplified Differential Input Stage.
5.0  INPUT INTERFACE APPLICATIONS

**FIGURE 5-1:** LVPECL Input Interface.

Note:
For $V_{CC} = 2.5V$ system, $R_{pd} = 19 \Omega$
For $V_{CC} = 3.3V$ system, $R_{pd} = 50 \Omega$

**FIGURE 5-2:** AC-Coupled LVPECL Interface.

Note:
For $V_{CC} = 3.3V$ system, $R_{pd} = 100 \Omega$
For $V_{CC} = 2.5V$ system, $R_{pd} = 50 \Omega$

**FIGURE 5-3:** LVDS Input Interface.

**FIGURE 5-4:** DC-Coupled CML Input Interface.

**FIGURE 5-5:** DC-Coupled CML Input Interface.
6.0 LVPECL OUTPUT APPLICATIONS

LVPECL output have very low output impedance (open emitter), and small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. There are several techniques in terminating the LVPECL output, as shown in Figure 6-1 through Figure 6-3.

**FIGURE 6-1:** Parallel Termination: Thevenin Equivalent.

**Note 1:** For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω
**Note 2:** For +3.3V systems: R1 = 130Ω, R2 = 82Ω

**FIGURE 6-2:** Three-Resistor “Y-Termination”.

**Note 1:** Power-saving alternative to Thevenin termination.
**Note 2:** Place termination resistors as close to destination inputs as possible.
**Note 3:** Rb resistor sets the DC bias voltage, equal to VT.
   - For +2.5V systems Rb = 19Ω.
   - For +3.3V systems Rb = 46Ω to 50Ω.
**Note 4:** C1 is an optional bypass capacitor intended to compensate for any tᵢ/ᵣ mismatches.
FIGURE 6-3: Terminating Unused I/O.

Note 1: Unused output (/Q) must be terminated to balance the output.

2: For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25 kΩ, R4 = 1.2 kΩ.
   For +3.3V systems: R1 = 130Ω, R2 = 82Ω, R3 = 1 kΩ, R4 = 1.6 kΩ.

3: C1 is an optional bypass capacitor intended to compensate for any t_{t_{f}} mismatches.

4: Unused output pairs (Q and /Q) may be left floating.
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

Example 16-Lead QFN*

Legend:

- Product code or customer-specific information
- Year code (last digit of calendar year)
- Year code (last 2 digits of calendar year)
- Week code (week of January 1 is week '01')
- Alphanumeric traceability code
- Pb-free JEDEC® designator for Matte Tin (Sn)
- This package is Pb-free. The Pb-free JEDEC designator (e3)
  can be found on the outer packaging for this package.
- Pin one index is identified by a dot, delta up, or delta down (triangle
  mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will
be carried over to the next line, thus limiting the number of available
characters for customer-specific information. Package may or may not include
the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.
16-Lead QFN 3 mm x 3 mm Package Outline and Recommended Land Pattern

**Title:**
16 Lead QFN 3x3mm Package Outline & Recommended Land Pattern

<table>
<thead>
<tr>
<th>Drawing #</th>
<th>QFN33-16LD-PL-1</th>
<th>Unit</th>
<th>MM</th>
</tr>
</thead>
</table>

**Notes:**
1. Max package warpage is 0.05 MM
2. Max allowable burr is 0.076 MM in all directions
3. Pin #1 is on top will be laser marked
4. Red circle in land pattern indicate thermal via. Size should be 0.30-0.35 MM in diameter and should be connected to GND for max thermal performance.
5. Green rectangles (shaded area) indicate solder stencil opening on exposed pad area. Size should be 0.60x0.60 MM in size, 0.20 MM spacing.

For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.
POD-Land Pattern drawing # QFN33-16LD-PL-1

RECOMMENDED LAND PATTERN

EXPOSED METAL TRACE

SOLDER STENCIL OPENING

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.
APPENDIX A: REVISION HISTORY

Revision A (March 2020)

• Converted Micrel document SY58012U to Microchip data sheet template DS20006319A.
• Minor text changes throughout.
**PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>X</th>
<th>X</th>
<th>X</th>
<th>XX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tape and Reel</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Examples:**

a) SY58012UMG: SY58012, 2.5V/3.3V Supply Voltage, 3 mm x 3 mm 16-Lead QFN, –40°C to +85°C Temperature Range, 100/Tube

b) SY58012UMG-TR: SY58012, 2.5V/3.3V Supply Voltage, 3 mm x 3 mm 16-Lead QFN, –40°C to +85°C Temperature Range, 1,000/Reel

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

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