SAM R34/R35 Errata

The SAM R34/ R35 family of devices conform functionally to the current device data sheet, except for the anomalies described in this document.

The SAM R34/R35 contains a SAML21 ARM® Cortex®-M0+ processor and UHF Transceiver (SX1276)

For Errata information on UHF Transceiver – refer to SX1276 Errata Note.

Note: This document summarizes all silicon errata issues seen on SAM R34/R35 devices, revision C.

Table 1. SAM R34/35 Silicon Device Identification

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device Identification (DID[31:0])</th>
<th>Revision ID (DID.REVISION[3:0])</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATSAMR34J18B</td>
<td>0x10810x28</td>
<td>C</td>
</tr>
<tr>
<td>ATSAMR34J17B</td>
<td>0x10810x29</td>
<td></td>
</tr>
<tr>
<td>ATSAMR34J16B</td>
<td>0x10810x2A</td>
<td></td>
</tr>
<tr>
<td>ATSAMR35J18B</td>
<td>0x10810x2B</td>
<td></td>
</tr>
<tr>
<td>ATSAMR35J17B</td>
<td>0x10810x2C</td>
<td></td>
</tr>
<tr>
<td>ATSAMR35J16B</td>
<td>0x10810x2D</td>
<td></td>
</tr>
</tbody>
</table>
# Table of Contents

SAM R34/R35 Error.................................................................1
1. Silicon Error Summary........................................................4
2. Silicon Error Issues............................................................8
   2.1. Device Service Unit (DSU).................................................8
       2.1.1. Wake-up From Standby Retention Mode Reference:16144 8
   2.2. 48 MHz Digital Frequency-Locked Loop (DFLL48M)..............8
       2.2.1. Write Access to DFLL Register Reference:9905 8
       2.2.2. Out of Bounds Interrupt Reference:16192 8
   2.3. Device Service Unit (DSU)..................................................8
   2.3.1. Linked Descriptor Reference:15670 8
       2.3.2. Linked Descriptors Reference:15683 9
   2.4. 96 MHz Fractional Digital Phase Locked Loop (FDPLL96M)......9
       2.4.1. DPLL Ratio Register Reference:15753 9
   2.5. PORT - I/O Pin Controller................................................9
       2.5.1. PORT Read/Write on Non-Implemented Register Reference:15611 9
       2.5.2. Pull-up and Pull-down Configurations on PA24 and PA25 Pins Reference:15581 9
   2.6. Supply Controller (SUPC).................................................10
       2.6.1. Buck Converter Mode Reference: CHIP003-311 & CHIP003-314 10
       2.6.2. Buck Converter as a Main Voltage Regulator Reference:15264 10
   2.7. Analog-to-Digital Controller (ADC)....................................10
       2.7.1. ADC Result in Unipolar Mode Reference:14431 10
       2.7.2. Free-Running Mode Reference:15463 10
       2.7.3. SYNCH BUSY.SWTRIG Bit Reference:16027 10
   2.8. Timer/Counter (TC).........................................................11
       2.8.1. SYNCH BUSY Flag Reference:15056 11
   2.9. Timer/Counter for Control Applications (TCC)......................11
       2.9.1. Advance Capture Mode Reference:14817 11
       2.9.2. SYNCH BUSY Flag Reference:15057 11
       2.9.3. MAX Capture Mode Reference:15059 11
       2.9.4. Dithering Mode Reference:15625 11
   2.10. Serial Communication Interface (SERCOM).........................12
       2.10.1. USART in Auto-Baud Mode Reference:13852 12
       2.10.2. SDA and SCL Fall Time Reference:16225 12
   2.11. External Interrupt Controller (EIC).................................12
       2.11.1. EIC ASYNCH Register Reference:14417 12
       2.11.2. Low Level or Rising Edge or Both Edges Reference:15278 12
       2.11.3. NMI Configuration Reference:15279 12
       2.11.4. Asynchronous Edge Detection Reference:16103 12
   2.12. True Random Number Generator (TRNG)............................13
   2.13. Event System (EVSYS)..................................................13
2.13.1. Synchronous Path Reference: 14532 ................................................................. 13
2.13.2. Overrun Flag Reference: 14835 ................................................................. 13

3. Revision History .................................................................................................... 14

The Microchip Web Site ......................................................................................... 15
Customer Change Notification Service .............................................................. 15
Customer Support ................................................................................................. 15
Microchip Devices Code Protection Feature ..................................................... 15
Legal Notice .............................................................................................................. 16
Trademarks ................................................................................................................ 16
Quality Management System Certified by DNV ................................................... 17
Worldwide Sales and Service ................................................................................. 18
Table 1-1. Silicon Errata Summary

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Issue Summary</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>2.1 Device Service Unit (DSU)</strong></td>
<td>Wake up From Standby Retention Mode</td>
<td>When device is waking from Standby Retention mode, selected alternate function on PA30 (for example, SERCOM) will be lost and it functions as the SWCLK pin and can switch device to Debug mode. See 2.1.1 Wake-up From Standby Retention Mode Reference:16144.</td>
<td>X</td>
</tr>
<tr>
<td><strong>2.2 48 MHz Digital Frequency-Locked Loop (DFLL48M)</strong></td>
<td>Write Access to DFLL Register</td>
<td>The DFLL clock must be requested before being configured, otherwise a write access to a DFLL register can freeze the device. See 2.2.1 Write Access to DFLL Register Reference:9905.</td>
<td>X</td>
</tr>
<tr>
<td><strong>2.2 48 MHz Digital Frequency-Locked Loop (DFLL48M)</strong></td>
<td>Out of Bounds Interrupt</td>
<td>If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. See 2.2.2 Out of Bounds Interrupt Reference:16192.</td>
<td>X</td>
</tr>
<tr>
<td><strong>2.2 48 MHz Digital Frequency-Locked Loop (DFLL48M)</strong></td>
<td>DFLL Status Bit in USB Clock Recovery Mode</td>
<td>The DFLL status bits in the STATUS register, during the USB clock recovery mode, can be wrong after a USB suspend state. (Only Applicable to SAM R34 device variants). See 2.2.3 DFLL Status Bit in USB Clock Recovery Mode (Only Applicable to SAM R34 Device Variants) Reference:16193.</td>
<td>X</td>
</tr>
<tr>
<td><strong>2.3 Direct Memory Access Controller (DMAC)</strong></td>
<td>Linked Descriptor</td>
<td>When using many DMA channel, if one of these DMA channels has a linked descriptor, a fetch error can appear on this channel. See 2.3.1 Linked Descriptor Reference:15670.</td>
<td>X</td>
</tr>
<tr>
<td><strong>2.3 Direct Memory Access Controller (DMAC)</strong></td>
<td>Linked Descriptors</td>
<td>When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch. See 2.3.2 Linked Descriptors Reference:15683.</td>
<td>X</td>
</tr>
<tr>
<td><strong>2.4 96 MHz Fractional Digital Phase Locked Loop (FDPLLR96M)</strong></td>
<td>DPLLRA30 Register</td>
<td>When FDPLL ratio value in the DPLLRA30 register is changed on the fly, the STATUS.DPLLRATIO register will not be set even though the ratio is updated. See 2.4.1 DPLLRA30 Register Reference:15753.</td>
<td>X</td>
</tr>
<tr>
<td>Module</td>
<td>Feature</td>
<td>Issue Summary</td>
<td>C</td>
</tr>
<tr>
<td>--------</td>
<td>---------</td>
<td>---------------</td>
<td>---</td>
</tr>
<tr>
<td>2.5 PORT - I/O Pin Controller</td>
<td>PORT Read/Write on Non-Implemented Register</td>
<td>PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB), do not generate a PAC protection error. See 2.5.1 PORT Read/Write on Non-Implemented Register Reference:15611.</td>
<td>X</td>
</tr>
<tr>
<td>2.5 PORT - I/O Pin Controller</td>
<td>Pull-up and Pull-down Configurations on PA24 and PA25 Pins</td>
<td>On PA24 and PA25 pins, the pull-up and pull-down configuration is not disabled automatically when alternative pin function is enabled. See 2.5.2 Pull-up and Pull-down Configurations on PA24 and PA25 Pins Reference:15581.</td>
<td>X</td>
</tr>
<tr>
<td>2.6 Supply Controller (SUPC)</td>
<td>Buck Converter Mode</td>
<td>Digital Phase-Locked Loop (FDPLL96M) and Digital Frequency-Locked Loop (DFLL48M) PLL's cannot be used with main voltage regulator in Buck converter mode. See 2.6.1 Buck Converter Mode Reference:CHIP003-311 &amp; CHIP003-314.</td>
<td>X</td>
</tr>
<tr>
<td>2.6 Supply Controller (SUPC)</td>
<td>Buck Converter as a Main Voltage Regulator</td>
<td>When Buck converter is set as main voltage regulator (SUPC.VREG.SEL=1), the microcontroller can freeze when leaving Standby mode. See 2.6.2 Buck Converter as a Main Voltage Regulator Reference:15264.</td>
<td>X</td>
</tr>
<tr>
<td>2.7 Analog-to-Digital Controller (ADC)</td>
<td>ADC Result in Unipolar Mode</td>
<td>The LSB of ADC result is stuck at zero in Unipolar mode for 8-bit and 10-bit resolution. See 2.7.1 ADC Result in Unipolar Mode Reference:14431.</td>
<td>X</td>
</tr>
<tr>
<td>2.7 Analog-to-Digital Controller (ADC)</td>
<td>Free-Running Mode</td>
<td>In Standby Sleep mode when the ADC is in free-running mode (CTRLC.FREERUN=1) and the RUNSTDBY bit is set to 0 (CTRLA.RUNSTDBY=0), the ADC keeps requesting its generic clock. See 2.7.2 Free-Running Mode Reference:15463.</td>
<td>X</td>
</tr>
<tr>
<td>2.7 Analog-to-Digital Controller (ADC)</td>
<td>SYNWBUSY.SWTRIG Bit</td>
<td>ADC SYNWBUSY.SWTRIG get stuck to one after wake-up from Standby Sleep mode. See 2.7.3 SYNWBUSY.SWTRIG Bit Reference:16027.</td>
<td>X</td>
</tr>
<tr>
<td>2.8 Timer/Counter (TC)</td>
<td>SYNWBUSY Flag</td>
<td>When clearing the STATUS.PERBUFV flag / STATUS.CCBUFx flag, the SYNWBUSY flag is released before the PERBUF / CCBUFx register is restored to its appropriate value. See 2.8.1 SYNWBUSY Flag Reference:15056.</td>
<td>X</td>
</tr>
<tr>
<td>Module</td>
<td>Feature</td>
<td>Issue Summary</td>
<td>C</td>
</tr>
<tr>
<td>--------------------------------------------</td>
<td>--------------------------</td>
<td>--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
<td>---</td>
</tr>
<tr>
<td>2.9 Timer/Counter for Control Applications (TCC)</td>
<td>Advance Capture Mode</td>
<td>Advance Capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) doesn’t work if an upper channel is not in one of these modes. See 2.9.1 Advance Capture Mode Reference:14817.</td>
<td>X</td>
</tr>
<tr>
<td>2.9 Timer/Counter for Control Applications (TCC)</td>
<td>SYNCBUSY Flag</td>
<td>When clearing the STATUS.xxBUFV flag, SYNCBUSY is released before the register is restored to its appropriate value. See 2.9.2 SYNCBUSY Flag Reference:15057.</td>
<td>X</td>
</tr>
<tr>
<td>2.9 Timer/Counter for Control Applications (TCC)</td>
<td>MAX Capture Mode</td>
<td>In Capture mode while using max Capture mode, with the timer set in Up-Counting mode, if an input event occurred within two cycles before TOP, the value captured is zero instead of TOP. See 2.9.3 MAX Capture Mode Reference:15059.</td>
<td>X</td>
</tr>
<tr>
<td>2.9 Timer/Counter for Control Applications (TCC)</td>
<td>Dithering Mode</td>
<td>Using TCC in Dithering mode with external retrigger events can lead to unexpected stretch of right aligned pulses or shrink of left aligned pulses. See 2.9.4 Dithering Mode Reference:15625.</td>
<td>X</td>
</tr>
<tr>
<td>2.10 Serial Communication Interface (SERCOM)</td>
<td>USART in Auto-Baud Mode</td>
<td>In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors. See 2.10.1 USART in Auto-Baud Mode Reference:13852.</td>
<td>X</td>
</tr>
<tr>
<td>2.10 Serial Communication Interface (SERCOM)</td>
<td>SDA and SCL Fall Time</td>
<td>When configured in HS or FastMode+, SDA and SCL fall times are shorter than I2C specification requirement and can lead to reflection. See 2.10.2 SDA and SCL Fall Time Reference:16225.</td>
<td>X</td>
</tr>
<tr>
<td>2.11 External Interrupt Controller (EIC)</td>
<td>EICASYNCH Register</td>
<td>Access to the EICASYNCH register in 8-bit or 16-bit mode is not functional. See 2.11.1 EICASYNCH Register Reference:14417.</td>
<td>X</td>
</tr>
<tr>
<td>2.11 External Interrupt Controller (EIC)</td>
<td>Low Level or Rising Edge or Both Edges</td>
<td>When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEEx) with the filter enabled (CONFIGn.FILTNx), a spurious flag might appear. See 2.11.2 Low Level or Rising Edge or Both Edges Reference:15278.</td>
<td>X</td>
</tr>
<tr>
<td>2.11 External Interrupt Controller (EIC)</td>
<td>NMI Configuration</td>
<td>Changing the NMI configuration (CONFIGn.SENSEEx) on the fly may lead to a false NMI interrupt. See 2.11.3 NMI Configuration Reference:15279.</td>
<td>X</td>
</tr>
<tr>
<td>Module</td>
<td>Feature</td>
<td>Issue Summary</td>
<td>C</td>
</tr>
<tr>
<td>---------------------------------------------</td>
<td>---------------------------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
<td>---</td>
</tr>
<tr>
<td>2.11 External Interrupt Controller (EIC)</td>
<td>Asynchronous Edge Detection</td>
<td>When the asynchronous edge detection is enabled, and the system is in Standby mode, only the first edge will generate an event. See 2.11.4 Asynchronous Edge Detection Reference:16103.</td>
<td>X</td>
</tr>
<tr>
<td>2.12 True Random Number Generator (TRNG)</td>
<td>Power Consumption in Standby Mode</td>
<td>When TRNG is enabled with configuration CTRL.RUNSTDBY = 0 (disabled during sleep), it could continue to operate resulting in over-consumption (~50uA) in Standby mode. See 2.12.1 Power Consumption in Standby Mode Reference: 14827.</td>
<td>X</td>
</tr>
<tr>
<td>2.13 Event System (EVSYS)</td>
<td>Synchronous Path</td>
<td>Using synchronous, spurious overrun can appear with generic clock for the channel always on. See 2.13.1 Synchronous Path Reference:14532.</td>
<td>X</td>
</tr>
<tr>
<td>2.13 Event System (EVSYS)</td>
<td>Overrun Flag</td>
<td>The acknowledge between an event user and the EVSYS clears the CHSTATUS.CHBUSYn bit before this information is fully propagated in the EVSYS one GCLK_EVSYS_CHANNEL_n clock cycle later which triggers and overrun flag. See 2.13.2 Overrun Flag Reference:14835.</td>
<td>X</td>
</tr>
</tbody>
</table>
2. **Silicon Errata Issues**
The following issues apply to the SAM R34/R35 family of devices.

2.1 **Device Service Unit (DSU)**

2.1.1 **Wake-up From Standby Retention Mode Reference:16144**
When device is waking from Standby Retention mode, selected alternate function on PA30 (for example, SERCOM) will be lost and it functions as the SWCLK pin and can switch device to Debug mode.

**Workaround**
Disable the debugger hot plug-in detection by setting the security bit. Security is set by issuing the NVMCTRL SSB command.

2.2 **48 MHz Digital Frequency-Locked Loop (DFLL48M)**

2.2.1 **Write Access to DFLL Register Reference:9905**
The DFLL clock must be requested before being configured, otherwise a write access to a DFLL register can freeze the device.

**Workaround**
Write a zero to the DFLL ONDEMAND bit in the DFLLLCTRL register before configuring the DFLL module.

2.2.2 **Out of Bounds Interrupt Reference:16192**
If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and might therefore be false out of bounds interrupts.

**Workaround**
Check the lock bits, DFLLLCKC and DFLLLCKF, in the OSCCTRL Interrupt Flag Status and Clear register (INTFLAG) are both set before enabling the DFLLOOB interrupt.

2.2.3 **DFLL Status Bit in USB Clock Recovery Mode (Only Applicable to SAM R34 Device Variants) Reference:16193**
During the USB Clock Recovery mode, the DFLL status bits in the STATUS register can be wrong after a USB suspend state.

**Workaround**
Do not monitor the DFLL status bits in the STATUS register during the USB Clock Recovery mode.

2.3 **Direct Memory Access Controller (DMAC)**

2.3.1 **Linked Descriptor Reference:15670**
When using many DMA channel, if one of these DMA channels has a linked descriptor, a fetch error can appear on this channel.
Workaround
Do not use linked descriptors, instead make a software link. Replace the channel which used the linked descriptor by a two-channel DMA (with linked descriptor disabled) handled by a two-channel event system:

- DMA channel 0 transfer completion can send a conditional event for DMA channel 1 (through event system with configuration of BTCTRL.EVOSEL=BLOCK for channel 0 and configuration CHCTRLB.EVACT=CBLOCK for channel 1)
- On the transfer complete reception of the DMA channel 0, immediately re-enable the channel 0
- Then DMA channel 1 transfer completion can send a conditional event for DMA channel 0 (through event system with configuration of BTCTRL.EVOSEL=BLOCK for channel 1 and configuration CHCTRLB.EVACT=CBLOCK for channel 0)
- On the transfer complete reception of the DMA channel 1, immediately re-enable the channel 1
- The mechanism can be launched by sending a software event on the DMA channel 0

2.3.2 Linked Descriptors Reference:15683
When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR) or an incorrect descriptor fetch. This happens if the channel number of the channel being enabled is lower than the channel already active.

Workaround
When enabling a DMA channel while other channels using linked descriptors are already active, the channel number of the new channel enabled must be greater than the other channel numbers.

2.4 96 MHz Fractional Digital Phase Locked Loop (FDPLL96M)

2.4.1 DPLLRATIO Register Reference:15753
When FDPLL ratio value in the DPLLRATIO register is changed on the fly, the STATUS.DPLLLDRTO will not be set even though the ratio is updated.

Workaround
Monitor the INTFLAG.DPLLLDRTO instead of STATUS.DPLLLDRTO to get the status for DPLLRATIO update.

2.5 PORT - I/O Pin Controller

2.5.1 PORT Read/Write on Non-Implemented Register Reference:15611
PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB), do not generate a PAC protection error.

Workaround
None.

2.5.2 Pull-up and Pull-down Configurations on PA24 and PA25 Pins Reference:15581
On PA24 and PA25 pins, the pull-up and pull-down configuration is not disabled automatically when alternative pin function is enabled.
Workaround
For PA24 and PA25 pins, the GPIO pull-up and pull-down must be disabled before enabling alternative functions on them.

2.6 Supply Controller (SUPC)

2.6.1 Buck Converter Mode Reference: CHIP003-311 & CHIP003-314
Buck Converter mode is not supported when using FDPLL96M and DFLL48M. As a result, Table 46-7 and Table 47-2 "Active Current Consumption - Active Mode" data for Buck Converter mode with DFLL48M configuration is not valid and must be disregarded.
Workaround
Use the LDO Regulator mode when using FDPLL and DFLL.

2.6.2 Buck Converter as a Main Voltage Regulator Reference: 15264
When Buck converter is set as main voltage regulator (SUPC.VREG.SEL=1), the microcontroller can freeze when leaving Standby mode.
Workaround
Enable the main voltage regulator in Standby mode (SUPC.VREG.RUNSTDBY=1) and set the standby in PL0 bit to one (SUPC.VREG.STDBYPL0=1).
Note: When SUPC.VREG.STDBYPL0=1, in Standby Sleep mode, the voltage regulator is used in PL0.

2.7 Analog-to-Digital Controller (ADC)

2.7.1 ADC Result in Unipolar Mode Reference: 14431
The LSB of ADC result is stuck at zero in Unipolar mode for 8-bit and 10-bit resolution.
Workaround
Use 12-bit resolution and take only least 8 bits or 10 bits, if necessary.

2.7.2 Free-Running Mode Reference: 15463
In Standby Sleep mode when the ADC is in free-running mode (CTRLC.FREERUN=1) and the RUNSTDBY bit is set to 0 (CTRLA.RUNSTDBY=0), the ADC keeps requesting its generic clock.
Workaround
Stop the free-running mode (CTRLC.FREERUN=0) before entering Standby Sleep mode.

2.7.3 SYNCBUSY.SWTRIG Bit Reference: 16027
ADC SYNCBUSY.SWTRIG get stuck to one after wake-up from Standby Sleep mode.
Workaround
Ignore ADC SYNCBUSY.SWTRIG status when waking up from Standby Sleep mode. ADC result can be read after INTFLAG.RESRDY is set. To start the next conversion, write a ‘1’ to SWTRIG.START.
2.8 Timer/Counter (TC)

2.8.1 SYNCBUSY Flag Reference:15056
When clearing the STATUS.PERBUF flag / STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF / CCBUFx register is restored to its appropriate value.

Workaround
Clear successively twice, the STATUS.PERBUF flag / STATUS.CCBUFx flag to ensure that, the PERBUF / CCBUFx register value is properly restored before updating it.

2.9 Timer/Counter for Control Applications (TCC)

2.9.1 Advance Capture Mode Reference:14817
Advance Capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) doesn’t work if an upper channel is not in one of these modes, for example, when CC[0]=CAPTMIN, CC[1]=CAPTMAX, CC[2]=CAPTEN, and CC[3]=CAPTEN, CAPTMIN and CAPTMAX won’t work.

Workaround
All capture will be done as expected.

2.9.2 SYNCBUSY Flag Reference:15057
When clearing the STATUS.xxBUFV flag, SYNCBUSY is released before the register is restored to its appropriate value.

Workaround
To ensure that the register value is properly restored before updating this same register through xx or xxBUF with a new value, the STATUS.xxBUFV flag must be cleared twice.

2.9.3 MAX Capture Mode Reference:15059
In Capture mode while using max Capture mode, with the timer set in Up-Counting mode, if an input event occurred within two cycles before TOP the value captured is zero instead of TOP.

Workaround
Two possible options are as follows:
1. If event is controllable, the capture event should not occur when counter is within 2 cycles before TOP value.
2. Use timer in down Counter mode and capture MIN value instead of MAX.

2.9.4 Dithering Mode Reference:15625
Using TCC in Dithering mode with external retrigger events can lead to an unexpected stretch of right-aligned pulses or shrink of left-aligned pulses.

Workaround
Do not use retrigger events or actions when TCC is configured in Dithering mode.
2.10 Serial Communication Interface (SERCOM)

2.10.1 USART in Auto-Baud Mode Reference:13852
In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

Workaround
None

2.10.2 SDA and SCL Fall Time Reference:16225
When configured in HS or FastMode+, SDA and SCL fall times are shorter than I2C specification requirement and can lead to reflection.

Workaround
When reflection is observed a 100 ohms serial resistor can be added on the impacted line.

2.11 External Interrupt Controller (EIC)

2.11.1 EICASYNCH Register Reference:14417
Access to the EIC_ASYNCH register in 8-bit or 16-bit mode is not functional.

Workaround
- Writing in 8-bit mode also writes this byte in all bytes of the 32-bit word.
- Writing higher 16-bits also writes the lower 16-bits
- Writing lower 16-bits also writes the higher 16-bits

The following two workarounds are available:
- Use 32-bit Write mode
- Write only lower 16-bits (This will write upper 16-bits also, but does not impact the application).

2.11.2 Low Level or Rising Edge or Both Edges Reference:15278
When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register immediately the EIC is enabled using the CTRLA ENABLE bit.

Workaround
Clear the INTFLAG bit once the EIC is enabled and before enabling the interrupts.

2.11.3 NMI Configuration Reference:15279
Changing the NMI configuration (CONFIGn.SENSEx) on the fly may lead to a false NMI interrupt.

Workaround
Clear the NMIFLAG bit once the NMI has been modified.

2.11.4 Asynchronous Edge Detection Reference:16103
When the asynchronous edge detection is enabled, and the system is in Standby mode, only the first edge will generate an event. The following edges will not generate events until the system wakes up.

Workaround
Asynchronous edge detection does not work; instead, use the synchronous edge detection (ASYNCH,ASYNCH[x]=0). To reduce power consumption when using synchronous edge detection, either set the GCLK_EIC frequency as low as possible or select the ULP32K clock (EIC CTRLA.CKSEL=1).

2.12 True Random Number Generator (TRNG)

2.12.1 Power Consumption in Standby Mode Reference:14827
When TRNG is enabled with configuration CTRL.RUNSTDBY = 0 (disabled during sleep), it could still continue to operate resulting in over-consumption (~50µA) in Standby mode.

Workaround
Disable the TRNG before entering Standby mode.

2.13 Event System (EVSYS)

2.13.1 Synchronous Path Reference:14532
Using synchronous, spurious overrun can appear with generic clock for the channel always on.

Workaround
- Request the generic clock on demand by setting the CHANNEL.ONDEMAND bit to one
- No penalty is introduced

2.13.2 Overrun Flag Reference:14835
The acknowledge between an event user and the EVSYS clears the CHSTATUS.CHBUSYn bit before this information is fully propagated in the EVSYS one GCLK_EVSYS_CHANNEL_n clock cycle later. As a consequence, any generator event occurring on that channel before that extra GCLK_EVSYS_CHANNEL_n clock cycle will trigger the overrun flag.

Workaround
For applications using event generators other than the software event, monitor the OVR flag.

For applications using the software event generator, wait one GCLK_EVSYS_CHANNEL_n clock cycle after the CHSTATUS.CHBUSYn bit is cleared before issuing a software event.
3. **Revision History**

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Section</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>05/2019</td>
<td>All</td>
<td>Initial Revision</td>
</tr>
</tbody>
</table>
The Microchip Web Site

Microchip provides online support via our web site at http://www.microchip.com/. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user’s guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Customer Change Notification Service

Microchip’s customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.


Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
• Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, Kleer, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTorch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntellIMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.


SQT P is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.
ISO/TS 16949
Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company’s quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001:2000 certified.
<table>
<thead>
<tr>
<th>AMERICAS</th>
<th>ASIA/PACIFIC</th>
<th>ASIA/PACIFIC</th>
<th>EUROPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Corporate Office</td>
<td>Australia - Sydney</td>
<td>India - Bangalore</td>
<td>Austria - Wels</td>
</tr>
<tr>
<td>2355 West Chandler Blvd.</td>
<td>Tel: 61-2-9868-6733</td>
<td>Tel: 91-80-3090-4444</td>
<td>Tel: 43-7242-2244-39</td>
</tr>
<tr>
<td>Chandler, AZ 85224-6199</td>
<td>China - Beijing</td>
<td>India - New Delhi</td>
<td>Fax: 43-7242-2244-393</td>
</tr>
<tr>
<td>Tel: 480-792-7200</td>
<td>Tel: 86-10-8569-7000</td>
<td>India - Pune</td>
<td>Denmark - Copenhagen</td>
</tr>
<tr>
<td>Fax: 480-792-7277</td>
<td>China - Chengdu</td>
<td>Tel: 91-11-4160-8631</td>
<td>Tel: 45-4450-2828</td>
</tr>
<tr>
<td>Technical Support:</td>
<td>Tel: 86-28-8665-5511</td>
<td>Japan - Osaka</td>
<td>Fax: 45-4485-2829</td>
</tr>
<tr>
<td><a href="http://www.microchip.com/">http://www.microchip.com/</a></td>
<td>China - Chongqing</td>
<td>Tel: 81-9-6152-7160</td>
<td>Finland - Espoo</td>
</tr>
<tr>
<td>Web Address:</td>
<td>Tel: 86-23-8980-9588</td>
<td>Japan - Tokyo</td>
<td>Tel: 358-9-4520-820</td>
</tr>
<tr>
<td><a href="http://www.microchip.com">http://www.microchip.com</a></td>
<td>China - Dongguan</td>
<td>Tel: 81-3-6880-3770</td>
<td>France - Paris</td>
</tr>
<tr>
<td>Atlanta</td>
<td>Tel: 86-769-8702-9880</td>
<td>Korea - Daegu</td>
<td>Tel: 33-1-69-53-63-20</td>
</tr>
<tr>
<td>Duluth, GA</td>
<td>China - Guangzhou</td>
<td>Korea - Seoul</td>
<td>Fax: 33-1-69-30-90-79</td>
</tr>
<tr>
<td>Tel: 678-957-9614</td>
<td>Tel: 86-20-8755-8029</td>
<td></td>
<td>Germany - Garching</td>
</tr>
<tr>
<td>Fax: 678-957-1455</td>
<td>China - Hangzhou</td>
<td></td>
<td>Tel: 49-6931-9700</td>
</tr>
<tr>
<td>Austin, TX</td>
<td>Tel: 86-87-892-8115</td>
<td></td>
<td>Germany - Haan</td>
</tr>
<tr>
<td>Tel: 512-257-3370</td>
<td>China - Hong Kong SAR</td>
<td></td>
<td>Tel: 49-2129-3766400</td>
</tr>
<tr>
<td>Boston</td>
<td>Tel: 852-2943-5100</td>
<td>Malaysia - Kuala Lumpur</td>
<td>Germany - Heilbronn</td>
</tr>
<tr>
<td>Westbrook MA</td>
<td>China - Nanjing</td>
<td>Malaysia - Penang</td>
<td>Tel: 49-7131-72400</td>
</tr>
<tr>
<td>Tel: 774-760-0087</td>
<td>Tel: 86-25-8473-2460</td>
<td>Philipsppines - Manila</td>
<td>Germany - Karlsruhe</td>
</tr>
<tr>
<td>Fax: 774-760-0088</td>
<td>China - Qingdao</td>
<td>Tel: 63-2-634-9065</td>
<td>Tel: 49-721-625370</td>
</tr>
<tr>
<td>Chicago</td>
<td>Tel: 86-532-8502-7355</td>
<td>Singapore</td>
<td>Germany - Munich</td>
</tr>
<tr>
<td>Itasca, IL</td>
<td>China - Shanghai</td>
<td>Tel: 65-6334-8870</td>
<td>Tel: 49-89-627-144-0</td>
</tr>
<tr>
<td>Tel: 630-285-0071</td>
<td>Tel: 86-21-3326-8000</td>
<td>Taiwan - Hsin Chu</td>
<td>Fax: 49-89-627-144-44</td>
</tr>
<tr>
<td>Fax: 630-285-0075</td>
<td>China - Shenzhen</td>
<td>Tel: 886-3-577-8366</td>
<td>Germany - Rosenheim</td>
</tr>
<tr>
<td>Dallas</td>
<td>Tel: 86-24-2334-2829</td>
<td>Taiwan - Kaohsiung</td>
<td>Tel: 49-8031-354-560</td>
</tr>
<tr>
<td>Addison, TX</td>
<td>China - Suzhou</td>
<td>Tel: 886-7-213-7830</td>
<td>Israel - Ra’anana</td>
</tr>
<tr>
<td>Tel: 972-818-7423</td>
<td>Tel: 86-186-6233-1526</td>
<td>Taiwan - Taipei</td>
<td>Tel: 972-9-744-7705</td>
</tr>
<tr>
<td>Fax: 972-818-2924</td>
<td>China - Wuhan</td>
<td>Tel: 886-2-2505-8600</td>
<td>Italy - Milan</td>
</tr>
<tr>
<td>Detroit</td>
<td>Tel: 86-27-5980-5300</td>
<td>Thailand - Bangkok</td>
<td>Tel: 39-0331-742611</td>
</tr>
<tr>
<td>Novi, MI</td>
<td>China - Xian</td>
<td>Tel: 66-2-694-1351</td>
<td>Fax: 39-0331-466781</td>
</tr>
<tr>
<td>Tel: 248-848-4000</td>
<td>Tel: 86-29-8833-7252</td>
<td>Vietnam - Ho Chi Minh</td>
<td>Italy - Padova</td>
</tr>
<tr>
<td>Houston, TX</td>
<td>China - Xiamen</td>
<td>Tel: 84-28-5448-2100</td>
<td>Tel: 39-049-7625286</td>
</tr>
<tr>
<td>Tel: 281-894-5983</td>
<td>Tel: 86-992-2388138</td>
<td></td>
<td>Netherlands - Drunen</td>
</tr>
<tr>
<td>Indianapolis</td>
<td>China - Zhuhai</td>
<td></td>
<td>Tel: 31-416-690399</td>
</tr>
<tr>
<td>Noblesville, IN</td>
<td>Tel: 86-756-3210040</td>
<td></td>
<td>Fax: 31-416-690340</td>
</tr>
<tr>
<td>Tel: 317-773-8323</td>
<td></td>
<td></td>
<td>Norway - Trondheim</td>
</tr>
<tr>
<td>Fax: 317-773-5453</td>
<td></td>
<td></td>
<td>Tel: 47-72864388</td>
</tr>
<tr>
<td>Tel: 317-536-2380</td>
<td></td>
<td></td>
<td>Poland - Warsaw</td>
</tr>
<tr>
<td>Los Angeles</td>
<td></td>
<td></td>
<td>Tel: 48-22-3325737</td>
</tr>
<tr>
<td>Mission Viejo, CA</td>
<td></td>
<td></td>
<td>Romania - Bucharest</td>
</tr>
<tr>
<td>Tel: 949-462-9523</td>
<td></td>
<td></td>
<td>Tel: 40-21-407-87-50</td>
</tr>
<tr>
<td>Fax: 949-462-9608</td>
<td></td>
<td></td>
<td>Spain - Madrid</td>
</tr>
<tr>
<td>Tel: 951-273-7800</td>
<td></td>
<td></td>
<td>Tel: 34-91-708-08-90</td>
</tr>
<tr>
<td>Raleigh, NC</td>
<td></td>
<td></td>
<td>Fax: 34-91-708-08-91</td>
</tr>
<tr>
<td>Tel: 919-844-7510</td>
<td></td>
<td></td>
<td>Sweden - Gothenberg</td>
</tr>
<tr>
<td>New York, NY</td>
<td></td>
<td></td>
<td>Tel: 46-31-704-60-40</td>
</tr>
<tr>
<td>Tel: 631-435-6000</td>
<td></td>
<td></td>
<td>Sweden - Stockholm</td>
</tr>
<tr>
<td>San Jose, CA</td>
<td></td>
<td></td>
<td>Tel: 46-8-5090-4654</td>
</tr>
<tr>
<td>Tel: 408-735-9110</td>
<td></td>
<td></td>
<td>UK - Wokingham</td>
</tr>
<tr>
<td>Fax: 408-436-4270</td>
<td></td>
<td></td>
<td>Tel: 44-118-921-5800</td>
</tr>
<tr>
<td>Canada - Toronto</td>
<td></td>
<td></td>
<td>Fax: 44-118-921-5820</td>
</tr>
<tr>
<td>Tel: 905-695-1980</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fax: 905-695-2078</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>