FEATURES:

- Small Package Size
- High Linear Output Power:
  - 802.11a OFDM Spectrum mask compliance up to 23 dBm
  - Added EVM~2.5% up to 18 dBm, typically, across 5.1-5.8 GHz for 54 Mbps 802.11a signal
- High Power-added Efficiency/Low Operating Current for 54 Mbps 802.11a Applications
  - ~11% @ \( P_{\text{OUT}} = 19 \text{ dBm} \) for 54 Mbps
- Gain:
  - Typically 26 dB gain across broadband 4.9-5.8 GHz
- Low Idle Current
  - ~120 mA \( I_{CQ} \)
- High Speed Power-up/-down
  - Turn on/off time (10%–90%) <100 ns
- Low Shut-down Current (<1 \( \mu \)A)
- On-chip Power Detection
- 20 dB Dynamic Range On-chip Power Detection
- \( 50\Omega \) On-chip Input Matching and Simple Output Matching
- Packages Available
  - 12-contact UQFN (2mm x 2mm x 0.6mm max thickness)

APPLICATIONS:

- WLAN (IEEE 802.11a/n)
- Japan WLAN
- HyperLAN2
- Multimedia

PRODUCT DESCRIPTION

The SST11CP15 is a high-linearity power amplifier that has low power consumption and is based on the highly-reliable InGaP/GaAs HBT technology.

The SST11CP15 can be easily configured for high-linearity, high-efficiency applications with superb power-added efficiency while operating over the entire 802.11a frequency band for U.S., European, and Japanese markets (4.9-5.8 GHz).

The SST11CP15 has excellent linearity, typically ~2.5% added EVM at 18 dBm output power which is essential for 54 Mbps 802.11a operation while meeting 802.11a spectrum mask at 23 dBm. SST11CP15 also has wide-range, single-ended power detectors which lower users’ cost on power control.

The power amplifier IC also features easy board-level usage along with high-speed power-up/down control. Low reference current (total \( I_{\text{REF}} <5 \text{ mA} \)) makes the SST11CP15 controllable by an on/off switching signal directly from the baseband chip. These features coupled with low operating current make the SST11CP15 ideal for the final stage power amplification in battery-powered 802.11a WLAN transmitter and access point applications.

The SST11CP15 is offered in 12-contact UQFN package with 0.6 mm maximum thickness. See Figure 2 for pin assignments and Table 1 for pin descriptions.
FUNCTIONAL BLOCKS

**FIGURE 1: Functional Block Diagram**
PIN ASSIGNMENTS

FIGURE 2: Pin Assignments for 12-contact UQFN

PIN DESCRIPTIONS

TABLE 1: Pin Description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Type¹</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>GND</td>
<td>0</td>
<td>Ground</td>
<td></td>
<td>The center pad should be connected to RF ground with several low inductance, low resistance vias.</td>
</tr>
<tr>
<td>RFIN</td>
<td>1</td>
<td>I</td>
<td>RF input, DC decoupled</td>
<td></td>
</tr>
<tr>
<td>VCCb</td>
<td>2</td>
<td>Power Supply</td>
<td>PWR</td>
<td>Supply voltage for bias circuit</td>
</tr>
<tr>
<td>VREF1</td>
<td>3</td>
<td>PWR</td>
<td>Current Control</td>
<td></td>
</tr>
<tr>
<td>VREF2</td>
<td>4</td>
<td>PWR</td>
<td>Current Control</td>
<td></td>
</tr>
<tr>
<td>VREF3</td>
<td>5</td>
<td>PWR</td>
<td>Current Control</td>
<td></td>
</tr>
<tr>
<td>DET</td>
<td>6</td>
<td>O</td>
<td>On-chip power detector</td>
<td></td>
</tr>
<tr>
<td>NC</td>
<td>7</td>
<td>No Connection</td>
<td></td>
<td>Unconnected pin</td>
</tr>
<tr>
<td>RFOUT</td>
<td>8</td>
<td>O</td>
<td>RF Output</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>9</td>
<td>Ground</td>
<td></td>
<td>Ground (NC is acceptable)</td>
</tr>
<tr>
<td>VCC3</td>
<td>10</td>
<td>Power Supply</td>
<td>PWR</td>
<td>Power supply, 3rd stage</td>
</tr>
<tr>
<td>VCC2</td>
<td>11</td>
<td>Power Supply</td>
<td>PWR</td>
<td>Power supply, 2nd stage</td>
</tr>
<tr>
<td>VCC1</td>
<td>12</td>
<td>Power Supply</td>
<td>PWR</td>
<td>Power supply, 1st stage</td>
</tr>
</tbody>
</table>

¹ I=Input, O=Output
Electrical Specifications

The AC and DC specifications for the power amplifier interface signals. Refer to Table 2 for the DC voltage and current specifications. Refer to Figures 3 through 8 for the RF performance.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Supply Voltage at pins 2, 10, 11, 12 (V_{CC}) .................................................. -0.3V to +5.5V
DC supply current (I_{CC}) .................................................................................. 500 mA
Operating Temperature (T_{A}) ............................................................................... -20°C to +85°C
Storage Temperature (T_{STG}) ............................................................................. -40°C to +120°C
Maximum Junction Temperature (T_{J}) ................................................................. +150°C
Maximum Output Power ......................................................................................... 27 dBm
Surface Mount Solder Reflow Temperature ......................................................... 260°C for 10 seconds

Operating Range

<table>
<thead>
<tr>
<th>Range</th>
<th>Ambient Temp</th>
<th>V_{CC}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Industrial</td>
<td>-10°C to +85°C</td>
<td>3.3V</td>
</tr>
</tbody>
</table>

Table 2: DC Electrical Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{CC}</td>
<td>Supply Voltage at pins 2, 10, 11, 12</td>
<td>2.7</td>
<td>3.3</td>
<td>4.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_{CC}</td>
<td>Supply Current @ P_{OUT} = 18 dBm at V_{CC} = 3.3V</td>
<td>210</td>
<td></td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_{CQ}</td>
<td>V_{CC} quiescent current</td>
<td>120</td>
<td></td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>I_{OFF}</td>
<td>Shut down current</td>
<td>&lt;1.0</td>
<td></td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>V_{REG}</td>
<td>Reference Voltage for recommended application</td>
<td>2.85</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Table 3: AC Electrical Characteristics for Configuration

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>F_{L-U}</td>
<td>Frequency range</td>
<td>4.9</td>
<td></td>
<td>5.8</td>
<td>GHz</td>
</tr>
<tr>
<td>Linearity</td>
<td>Output power with 2.5% EVM at 54 Mbps OFDM signal when operating at 3.3V V_{CC}</td>
<td>18</td>
<td></td>
<td>20</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>Output power level with 802.11a mask compliance across 4.9-5.8 GHz</td>
<td>23</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>G</td>
<td>Linear gain across 4.9-5.8GHz</td>
<td>26</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Det</td>
<td>Power detector output voltage range</td>
<td>0.3</td>
<td>1.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>2f, 3f, 4f, 5f</td>
<td>Harmonics at 22 dBm, without trapping capacitors</td>
<td>-40</td>
<td></td>
<td></td>
<td>dBc</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS
Test Conditions: $V_{CC} = 3.3V$, $T_A = 25^\circ C$, $V_{REG} = 2.85V$ unless otherwise noted

EVM for 54 Mbps Operation

**FIGURE 3: EVM versus Output Power**

**FIGURE 4: Power Supply Current versus Output Power**
Power Gain versus Output Power

- Freq=4.9 GHz
- Freq=5.1 GHz
- Freq=5.5 GHz
- Freq=5.825 GHz

FIGURE 5: Power Gain versus Output Power

Maximum Mask Compliance

Spectrum Mask 802.11a (5500MHz)

- Spectrum
- Relative limit

FIGURE 6: Frequency = 5.5 GHz at P_OUT = 23.3 dBm with I_CC = 390 mA
FIGURE 7: Detector Voltage vs Output Power

FIGURE 8: PAE vs Output Power
FIGURE 9: S-Parameters
**Note:** The SST11CP15 has on-chip DC-blocking caps for RF ports

**FIGURE 10:** Typical Application for High-Linearity 802.11a/n Application ($V_{CC} = 3.3V$, $V_{REG} = 2.85V$)
PRODUCT ORDERING INFORMATION

Valid combinations for SST11CP15
SST11CP15-QUBE

SST11CP15 Evaluation Kits
SST11CP15-QUBE-K

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.
PACKAGING DIAGRAMS

FIGURE 11: 12-contact Ultra-thin Quad Flat No-lead (UQFN)
SST Package Code: QUB

Note
1. Similar to JEDEC JEP95 UQFN/USON variants, though number of contacts and some dimensions are different.
2. From the bottom view, the pin 1 indicator may be either a curved indent or a 45-degree chamfer.
3. The external paddle is electrically connected to the die back-side and to VSS. This paddle must be soldered to the PC board; it is required to connect this paddle to the VSS of the unit. Connection of this paddle to any other voltage potential will result in shorts and electrical malfunction of the device.
4. Untoleranced dimensions are nominal target dimensions.
5. All linear dimensions are in millimeters (max/min).

TABLE 4: Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Description</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>• Initial Release of Data Sheet</td>
<td>Jul 2010</td>
</tr>
<tr>
<td>01</td>
<td>• Updated Features on page 1; Table 2 on page 4; and Figures 3-5, 7,8, and 10.</td>
<td>Jan 2011</td>
</tr>
</tbody>
</table>