The PIC32MZ Graphics (DA) family devices that you have received conform functionally to the current Device Data Sheet (DS60001361H), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. If applicable, any silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MZ Graphics (DA) family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table (if applicable) apply to the current silicon revision (A1).

Data Sheet clarifications and corrections (if applicable) start on page 20.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip’s programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select Window > Dashboard, and then click the Refresh Debug Tool Status icon ( ).
5. The part number and the Device and Revision ID values appear in the Output window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MZ Graphics (DA) family silicon revisions are shown in Table 1.

### TABLE 1: SILICON DEVREV VALUES

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device ID(1)</th>
<th>Revision ID for Silicon Revision(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC32MZ1025DAA169</td>
<td>0x05F0C053</td>
<td>A1 0x1</td>
</tr>
<tr>
<td>PIC32MZ1025DAB169</td>
<td>0x05F0D053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1064DAA169</td>
<td>0x05F0F053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1064DAB169</td>
<td>0x05F10053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAA169</td>
<td>0x05F15053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAB169</td>
<td>0x05F16053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAA169</td>
<td>0x05F18053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAB169</td>
<td>0x05F19053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1025DAG169</td>
<td>0x05F42053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1025DAH169</td>
<td>0x05F43053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1064DAG169</td>
<td>0x05F45053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1064DAH169</td>
<td>0x05F46053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAG169</td>
<td>0x05F4B053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAH169</td>
<td>0x05F4C053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAG169</td>
<td>0x05F4E053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAH169</td>
<td>0x05F4F053</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Refer to the “Memory Organization” and “Special Features” chapters in the current Device Data Sheet (DS60001361H) for detailed information on Device and Revision IDs for your specific device.
### TABLE 1: SILICON DEVREV VALUES (CONTINUED)

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<th>Part Number</th>
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<th>Revision ID for Silicon Revision(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC32MZ1025DAA176</td>
<td>0x05F78053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1025DAB176</td>
<td>0x05F79053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1064DAA176</td>
<td>0x05F7B053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1064DAB176</td>
<td>0x05F7C053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ2025DAA176</td>
<td>0x05F81053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ2025DAB176</td>
<td>0x05F82053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ2064DAA176</td>
<td>0x05F84053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ2064DAB176</td>
<td>0x05F85053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1025DAG176</td>
<td>0x05FAE053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1025DAH176</td>
<td>0x05FAF053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1064DAG176</td>
<td>0x05FB1053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1064DAH176</td>
<td>0x05FB2053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ2025DAG176</td>
<td>0x05FB7053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ2025DAH176</td>
<td>0x05FB8053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ2064DAG176</td>
<td>0x05FBA053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ2064DAH176</td>
<td>0x05FBB053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1025DAA288</td>
<td>0x05F5D053</td>
<td>0x1</td>
</tr>
<tr>
<td>PIC32MZ1025DAB288</td>
<td>0x05F5E053</td>
<td>0x1</td>
</tr>
<tr>
<td>PIC32MZ1064DAA288</td>
<td>0x05F60053</td>
<td>0x1</td>
</tr>
<tr>
<td>PIC32MZ1064DAB288</td>
<td>0x05F61053</td>
<td>0x1</td>
</tr>
<tr>
<td>PIC32MZ2025DAA288</td>
<td>0x05F66053</td>
<td>0x1</td>
</tr>
<tr>
<td>PIC32MZ2025DAB288</td>
<td>0x05F67053</td>
<td>0x1</td>
</tr>
<tr>
<td>PIC32MZ2064DAA288</td>
<td>0x05F69053</td>
<td>0x1</td>
</tr>
<tr>
<td>PIC32MZ2064DAB288</td>
<td>0x05F6A053</td>
<td>0x1</td>
</tr>
</tbody>
</table>

**Note 1:** Refer to the “Memory Organization” and “Special Features” chapters in the current Device Data Sheet (DS60001361H) for detailed information on Device and Revision IDs for your specific device.
## TABLE 2: SILICON ISSUE SUMMARY

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Item</th>
<th>Issue Summary</th>
<th>Affected Revisions(^{(1)})</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary Oscillator</td>
<td>Primary Oscillator Crystal</td>
<td>1.</td>
<td>The Primary Oscillator (POsc) has been tested in a normal power-up sequence and supports specific crystal operation.</td>
<td>X</td>
</tr>
<tr>
<td>Secondary Oscillator</td>
<td>Secondary Oscillator Crystal</td>
<td>2.</td>
<td>The Secondary Oscillator (SOsc) does not support crystal operation.</td>
<td>X</td>
</tr>
<tr>
<td>Reset</td>
<td>BOR</td>
<td>3.</td>
<td>A system Reset is not generated on a BOR event (VPorio &lt; Vddio &lt; VBorio). This will stop system clocks with all the I/O pin functions frozen in the present state until either Vddio falls to VPorio or Vddio &gt; VBorio.</td>
<td>X</td>
</tr>
<tr>
<td>Reset</td>
<td>HVD Reset</td>
<td>4.</td>
<td>A BOR event also sets the HVD1V8R (RCON&lt;29&gt;) bit.</td>
<td>X</td>
</tr>
<tr>
<td>Power-Saving</td>
<td>PMD Bits</td>
<td>5.</td>
<td>Turning off the REFCLK modules through the PMD (PMD6&lt;11:8&gt;) bits causes unpredictable device behavior.</td>
<td>X</td>
</tr>
<tr>
<td>DMA</td>
<td>PMD Bits</td>
<td>6.</td>
<td>Setting the PMD bit for DMA (PMD7&lt;4&gt;) does not disable clocks to the DMA peripheral.</td>
<td>X</td>
</tr>
<tr>
<td>VBAT —</td>
<td></td>
<td>7.</td>
<td>VBAT is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>Deep Sleep —</td>
<td></td>
<td>8.</td>
<td>Deep Sleep mode is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>i²C —</td>
<td></td>
<td>9.</td>
<td>The i²C module does not function reliably under certain conditions.</td>
<td>X</td>
</tr>
<tr>
<td>ADC —</td>
<td>Interrupts</td>
<td>10.</td>
<td>ADC Group Early Interrupt is not functional (IRQ205).</td>
<td>X</td>
</tr>
<tr>
<td>ADC —</td>
<td>Level Trigger</td>
<td>11.</td>
<td>ADC level trigger will not perform burst conversions in debug mode.</td>
<td>X</td>
</tr>
<tr>
<td>ADC —</td>
<td>DNL</td>
<td>12.</td>
<td>In Differential mode, code 3072 is not within the specification.</td>
<td>X</td>
</tr>
<tr>
<td>ADC —</td>
<td>Turbo Mode</td>
<td>13.</td>
<td>Turbo mode is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>SDHC —</td>
<td>Clock</td>
<td>14.</td>
<td>The SDHC module requires System PLL to be turned ON.</td>
<td>X</td>
</tr>
<tr>
<td>SDHC —</td>
<td>Clock Stability</td>
<td>15.</td>
<td>The SDHC module may not function if the SDCD pin is not used.</td>
<td>X</td>
</tr>
<tr>
<td>SDHC —</td>
<td>Card Detect Status</td>
<td>16.</td>
<td>Card detect status indication through the CDSLVL bit (SDHCSTAT1&lt;18&gt;) is inverted.</td>
<td>X</td>
</tr>
<tr>
<td>SDHC —</td>
<td>Write Protect Status</td>
<td>17.</td>
<td>Write protect status indication through the WPSLVL bit (SDHCSTAT1&lt;19&gt;) is inverted.</td>
<td>X</td>
</tr>
<tr>
<td>SDHC —</td>
<td>Stop at Block Gap</td>
<td>18.</td>
<td>The Stop at Block Gap feature of the SDHC module is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>HLVD —</td>
<td></td>
<td>19.</td>
<td>High/Low-Voltage Detect module is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>DDR2C —</td>
<td></td>
<td>20.</td>
<td>DDR2 is functional only between 0°C and 70°C.</td>
<td>X</td>
</tr>
<tr>
<td>DDR2C —</td>
<td>Internal DDRVREF Circuit</td>
<td>21.</td>
<td>Internal DDRVREF circuit is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>SQI —</td>
<td>XIP Mode</td>
<td>22.</td>
<td>SQI XIP mode is not functional in cached memory space (KSEG2).</td>
<td>X</td>
</tr>
<tr>
<td>USB —</td>
<td>Interrupt</td>
<td>23.</td>
<td>The USB General Event Interrupt (IRQ 132) is not persistent.</td>
<td>X</td>
</tr>
<tr>
<td>USB —</td>
<td>Resume</td>
<td>24.</td>
<td>The USB module does not support remote wake-up.</td>
<td>X</td>
</tr>
<tr>
<td>System Bus</td>
<td>Writes</td>
<td>25.</td>
<td>The EERP bit (SBTxECON&lt;24&gt;) is not functional.</td>
<td>X</td>
</tr>
</tbody>
</table>

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.
## TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Item</th>
<th>Issue Summary</th>
<th>Affected Revisions&lt;sup&gt;(1)&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Crypto</td>
<td>Flash Data Access</td>
<td>26.</td>
<td>The Crypto module cannot access data from Flash.</td>
<td>X</td>
</tr>
<tr>
<td>UART</td>
<td>Overflow</td>
<td>27.</td>
<td>Clearing the OERR bit (UxSTA&lt;1&gt;) clears the receiver buffer.</td>
<td>X</td>
</tr>
<tr>
<td>EBI</td>
<td>Chip Select</td>
<td>28.</td>
<td>For Asynchronous NOR Flash, EBI internal clock specification, TEBCLK (EB10), is not met.</td>
<td>X</td>
</tr>
<tr>
<td>CTMU</td>
<td>Triggers</td>
<td>29.</td>
<td>Edge Sequencing mode (EDGSEQEN(CTMUCON&lt;10&gt;)) and Edge modes are not functional.</td>
<td>X</td>
</tr>
<tr>
<td>CTMU</td>
<td>TGEN</td>
<td>30.</td>
<td>When the TGEN bit is set, manual current sourcing from CTMU is not possible.</td>
<td>X</td>
</tr>
<tr>
<td>Temperature Sensor</td>
<td>—</td>
<td>31.</td>
<td>The temperature sensor does not function.</td>
<td>X</td>
</tr>
<tr>
<td>ICSP</td>
<td>TDO</td>
<td>32.</td>
<td>While programming on any ICSP PGECx/PGEDx pair, the TDO pin will toggle.</td>
<td>X</td>
</tr>
<tr>
<td>PORTS</td>
<td>Vih Electrical Specification</td>
<td>33.</td>
<td>The VIH specification of 0.65 * VDDIO is not met.</td>
<td>X</td>
</tr>
<tr>
<td>Primary Oscillator</td>
<td>Automatic Gain</td>
<td>34.</td>
<td>The Primary Oscillator Automatic Gain Control (AGC) is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>Primary Oscillator</td>
<td>Control (AGC)</td>
<td>35.</td>
<td>The Primary Oscillator AGC Gain Search Step Settling Time Control bits are not functional.</td>
<td>X</td>
</tr>
<tr>
<td>Primary Oscillator</td>
<td>Primary Oscillator Fine</td>
<td>36.</td>
<td>The Primary Oscillator AGC Gain Control bits are not functional.</td>
<td>X</td>
</tr>
<tr>
<td>GPU</td>
<td>GPURESET bit</td>
<td>37.</td>
<td>The GPU Run-time enable/Disable feature is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>SDHC</td>
<td>SDWPPOL bit</td>
<td>38.</td>
<td>The SDHC Write-protect Polarity Inversion feature is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>PMP</td>
<td>Status Flags</td>
<td>39.</td>
<td>The PMP input buffer full flag, IB0F, and the output buffer underflow, OBUF, are getting set as soon as the PMP module is enabled in Slave mode (PMPTTL bit (PMCON&lt;10&gt;) is equal to ‘1’).</td>
<td>X</td>
</tr>
<tr>
<td>I²C</td>
<td>Start/Restart</td>
<td>40.</td>
<td>When the I²C module is in Slave mode, Start and Restart interrupts are not functional.</td>
<td>X</td>
</tr>
<tr>
<td>Crypto</td>
<td>Partial Packet</td>
<td>41.</td>
<td>The Crypto Engine does not support partial packet processing.</td>
<td>X</td>
</tr>
<tr>
<td>Crypto</td>
<td>Zero-length Packet</td>
<td>42.</td>
<td>The Crypto Engine does not support a Hash operation on an empty string.</td>
<td>X</td>
</tr>
<tr>
<td>CTMU</td>
<td>Idle</td>
<td>43.</td>
<td>CTMU current source is not enabled in Idle mode (CTMUSIDL bit in the CTMUCON register is equal to ‘1’), which prevents ADC if enabled in Idle mode from being able to measure the CTMU temperature sensor.</td>
<td>X</td>
</tr>
<tr>
<td>Timer1</td>
<td>Asynchronous Counter</td>
<td>44.</td>
<td>Timer1 in Asynchronous External Counter mode does not reflect the first count from an external T1CK input.</td>
<td>X</td>
</tr>
<tr>
<td>Timer1</td>
<td>TMR1 Register</td>
<td>45.</td>
<td>TMR1 register of Timer1 in Asynchronous mode remains at initial set value for five external clock pulses after wake-up from Sleep mode.</td>
<td>X</td>
</tr>
<tr>
<td>Timer1</td>
<td>Asynchronous Mode</td>
<td>46.</td>
<td>Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.</td>
<td>X</td>
</tr>
</tbody>
</table>

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.
### TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

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<th>Feature</th>
<th>Item</th>
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</thead>
<tbody>
<tr>
<td>Timer1</td>
<td>Gated Mode</td>
<td>47.</td>
<td>Timer1 does not work properly in Gated mode with prescaler enabled.</td>
<td>X</td>
</tr>
<tr>
<td>Timer1</td>
<td>TMR1 Register Writes</td>
<td>48.</td>
<td>Back-to-back writes to the TMR1 register are not allowed for four PBCLK cycles.</td>
<td>X</td>
</tr>
<tr>
<td>Timer1</td>
<td>Asynchronous Timer1</td>
<td>49.</td>
<td>The Asynchronous Timer Write Disable bit, TWDIS (TxCON&lt;12&gt;), and the Asynchronous Timer Write in Progress bit, TWIP (TxCON&lt;11&gt;), are non-functional.</td>
<td>X</td>
</tr>
<tr>
<td>UART</td>
<td>High-Speed Mode</td>
<td>50.</td>
<td>The UART Stop bit duration is shorter than expected in High-Speed mode (UxMODE.BRGH =1) for baud rates less than 7.5 Mbps.</td>
<td>X</td>
</tr>
<tr>
<td>Sleep</td>
<td>IPD</td>
<td>51.</td>
<td>3 mA increase in sleep current when PB5DIV is disabled.</td>
<td>X</td>
</tr>
<tr>
<td>CFG</td>
<td>Unique ID</td>
<td>52.</td>
<td>Unique ID is not programmed on devices which are released earlier than trace code dated 1821xxx.</td>
<td>X</td>
</tr>
<tr>
<td>EBI</td>
<td>EBI RDYx pin as GPIO</td>
<td>53.</td>
<td>The EBI RDYEN1 bit (CFGEBIC&lt;25&gt;), EBI RDYEN2 bit (CFGEBIC&lt;26&gt;), EBI RDYEN3 bit(CFGEBIC&lt;27&gt;) are not functional and always set to ‘1’.</td>
<td>X</td>
</tr>
<tr>
<td>I²C</td>
<td>I²C Slave</td>
<td>54.</td>
<td>The 7-bit address that matches the 10-bit upper address value (111_10xx) is not accepted regardless of the STRICT bit setting.</td>
<td>X</td>
</tr>
<tr>
<td>I²C</td>
<td>Speed</td>
<td>55.</td>
<td>I²C module does not meet low period of the SCL clock (tLOW) parameter from I²C specification for clock frequency &gt;= 400 kHz.</td>
<td>X</td>
</tr>
<tr>
<td>Input Capture</td>
<td>Debug</td>
<td>56.</td>
<td>Debug breakpoints are not supported when using Input Capture with DMA.</td>
<td>X</td>
</tr>
<tr>
<td>SDHC</td>
<td>MMC</td>
<td>57.</td>
<td>Data from the MMC card can not be read correctly when the block size is set smaller than 512 bytes.</td>
<td>X</td>
</tr>
<tr>
<td>Sleep</td>
<td>Wake-up</td>
<td>58.</td>
<td>Multiple sleep attempts which occur before the CPU has fully awakened, may stall the CPU until the next reset event.</td>
<td>X</td>
</tr>
<tr>
<td>SPI</td>
<td>Block Transmission</td>
<td>59.</td>
<td>At the end of a transmission, the SRMT bit can indicate the completion of the transmission for one PBCLK even though the transmission has one block remaining.</td>
<td>X</td>
</tr>
<tr>
<td>SQI Special Functions Registers</td>
<td></td>
<td>60.</td>
<td>The CPU stalls if the SQI Special Function Registers are read before the REFCLKO2 clock is enabled.</td>
<td>X</td>
</tr>
<tr>
<td>Timer2-9</td>
<td>Match</td>
<td>61.</td>
<td>If timer match coincides with entry into sleep mode, timer event triggers and interrupt may not occur.</td>
<td>X</td>
</tr>
<tr>
<td>Timer2-9</td>
<td>Match</td>
<td>62.</td>
<td>If timer match coincides with entry into Idle mode, timer event triggers and interrupt may not occur.</td>
<td>X</td>
</tr>
<tr>
<td>Timer2-9</td>
<td>Debug</td>
<td>63.</td>
<td>On a debug breakpoint, TMRx register, x =2-9, may not be representative of the correct value.</td>
<td>X</td>
</tr>
<tr>
<td>USB</td>
<td>LPM</td>
<td>64.</td>
<td>The USB Link Power Management (LPM) feature is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>USB</td>
<td>Host Resume</td>
<td>65.</td>
<td>The USB Host module does not send correct resume signal on the USB bus on subsequent suspend/resume sequences.</td>
<td>X</td>
</tr>
</tbody>
</table>

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.
### TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Item</th>
<th>Issue Summary</th>
<th>Affected Revisions&lt;sup&gt;(1)&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB</td>
<td>Host Disconnect Detection</td>
<td>66.</td>
<td>The USB Host module does not wake up CPU from sleep when a USB device is disconnected.</td>
<td>X</td>
</tr>
<tr>
<td>USB</td>
<td>Suspend/Resume IRQ</td>
<td>67.</td>
<td>USB Suspend/Resume Event through IRQ 103 is not functional.</td>
<td>X</td>
</tr>
</tbody>
</table>

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.
1. **Module: Primary Oscillator**

The POSC has been tested in a normal power-up sequence and supports specific crystal operation.

**Work around 1**

The Primary Oscillator (POSC) has been characterized to operate at 8 MHz and 12 MHz when the circuit shown in Figure 1 is implemented, and the operating conditions listed in Table 3 are met.

**Work around 2**

Alternatively, use an external clock or Internal FRC Oscillator. Note that communication interfaces (DDR2, USB, etc..) with tighter clock accuracy requirements will not function with the FRC as clock source.

---

**FIGURE 1: POSC CRYSTAL CIRCUIT**

---

### TABLE 3: CRYSTAL SPECIFICATION

<table>
<thead>
<tr>
<th>Crystal Frequency (See Note 1)</th>
<th>Series Resistor Rs</th>
<th>POSC Gain Setting POSCGAIN&lt;1:0&gt; (DEVCFG0&lt;20:19&gt;)</th>
<th>POSC Boost Setting POSCBOOST (DEVCFG0&lt;21&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 MHz</td>
<td>2 kΩ</td>
<td>'0b00 (GAIN_0)</td>
<td>'0b1</td>
</tr>
<tr>
<td>12 MHz</td>
<td>1 kΩ</td>
<td>'0b00 (GAIN_0)</td>
<td>'0b1</td>
</tr>
</tbody>
</table>

**Note 1:** Using any other crystal frequency will require special component selection and characterization.

**Note 2:** A parallel register (RP) should not be used to increase the gain of the POSC.

---

### Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>X</th>
</tr>
</thead>
</table>

---

2. **Module: Secondary Oscillator**

A crystal oscillator cannot be used as the input to the Secondary Oscillator (Sosc) pins: SOSCI and SOSCO.

**Work around**

Use an external clock source (32.768 Hz) applied to the SOSCO pin with the FSOSCEN bit (DEVCFG1<6>) set to '0' (i.e., the Sosc is disabled through the Configuration Word) for a real-time clock base; otherwise, use the internal LPRC for non-precision requirements.

---

### Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>X</th>
</tr>
</thead>
</table>
3. Module: Reset

A system Reset is not generated on a BOR event (VPORIO < VDDIO < VBORIO). This will stop system clocks with all the I/O pin functions frozen in the present state until either VDDIO falls to VPORIO or VDDIO > VBORIO.

Work around

Reset device using a MCLR pin through an external reset supervisor/monitor is shown in Figure 2. Set the SMCLR (DEVCFG2<15>) configuration bit to '0', which makes the MCLR to act as a POR Reset instead of a normal system reset.

Table 4 and Table 5 provide a list of external Reset supervisor and regulators with built in Reset supervisors that can be used.

When selecting an external supervisor other than the ones provided in Table 4 and Table 5, the following requirements must be taken into consideration:

- Minimum Reset trip voltage of the external supervisor should be VBORIO (Max)+0.5V.
- The external reset supervisor/LDO output going to MCLR should have an open drain output to not interfere with the MPLAB programming/debug tools.

When this work around is implemented, the minimum VDDIO operating voltage of the application needs to be above the reset supervisor maximum trip voltage + 0.2V, where 0.2V compensates for variation in the external reset supervisor voltage.

![FIGURE 2: EXTERNAL RESET CIRCUIT](image)

![TABLE 4: RESET SUPERVISOR/VOLTAGE MONITOR](table)

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Reset Trip Voltage</th>
<th>MCLR Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIC803-26D2VC3</td>
<td>2.63V</td>
<td>Reset pin (Open Drain)</td>
</tr>
</tbody>
</table>

![TABLE 5: LDOs WITH EMBEDDED RESET SUPERVISOR](table)

<table>
<thead>
<tr>
<th>Part Number</th>
<th>VIN (Max)</th>
<th>VOUT</th>
<th>IOUT</th>
<th>Reset Trip Voltage</th>
<th>MCLR Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIC5239-3.3YM</td>
<td>30V</td>
<td>3.3V</td>
<td>500 ma</td>
<td>3.3V-5%</td>
<td>FLG pin (Open Drain)</td>
</tr>
<tr>
<td>MIC5239-3.3YMM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MCP1725-3302E/MC</td>
<td>6V</td>
<td>3.3V</td>
<td>500 ma</td>
<td>3.3V-10%</td>
<td>PWRGD pin (Open Drain)</td>
</tr>
<tr>
<td>MCP1727-3302E/MF</td>
<td>6V</td>
<td>3.3V</td>
<td>1500 ma</td>
<td>3.3V-10%</td>
<td>PWRGD pin (Open Drain)</td>
</tr>
</tbody>
</table>

![Affected Silicon Revisions](table)

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
<tr>
<td>X</td>
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</tbody>
</table>
4. **Module: Reset**
   A BOR event also sets the HVD1V8R bit (RCON<29>).

   **Work around**
   True high-voltage detect will set only the HVD1V8R (RCON<29>) bit. This bit should be ignored when it is set along with the BOR (RCON<1>) bit. Also, make sure to clear the HVD1V8R bit on exit from the BOR event, if set.

   **Affected Silicon Revisions**
   | A1 | X |
   | A1 | X |

5. **Module: Power-Saving**
   Turning off the REFCLK modules through the PMD bits (PMD6<11:8>) causes unpredictable device behavior.

   **Work around**
   None. Do not disable the REFCLK modules through the PMD bits.

   **Affected Silicon Revisions**
   | A1 | X |
   | A1 | X |

6. **Module: DMA**
   Setting the PMD bit for DMA (PMD7<4>) does not disable clocks to the DMA peripheral.

   **Work around**
   Use the ON bit (DMACON<15>) to enable/disable DMA globally, or use the CHEN bit (DCHxCON<7>) to enable/disable individual channels.

   **Affected Silicon Revisions**
   | A1 | X |
   | A1 | X |

7. **Module: VBAT**
   The VBAT pin is not functional. Connect the VBAT pin to VDDIO.

   **Work around**
   None.

   **Affected Silicon Revisions**
   | A1 | X |
   | A1 | X |

8. **Module: Deep Sleep**
   Deep Sleep mode is not functional.

   **Work around**
   None.

   **Affected Silicon Revisions**
   | A1 | X |
   | A1 | X |
9. Module: I²C

Indeterminate I²C module behavior may result when data rates greater than 100 kHz and/or continuous sequential data transfers greater than 500 bytes are used.

The potential false intermittent error signals can result in one of the following error conditions, which are listed in order of decreasing frequency:

- **False Error Condition 1:** False Master Bus Collision Detect (Master-mode only) – The error is indicated through the BCL bit (I2CxSTAT<10>).
- **False Error Condition 2:** Receive Overflow (Master or Slave modes) – The error is indicated through the I2COV bit (I2CxSTAT<20>).
- **False Error Condition 3:** Suspended I²C Module Operations (Master or Slave modes) – I²C transactions in progress are inadvertently suspended without error indications.

**Note:** All three false errors are recoverable in software.

---

### Work around 1

- **False Error Condition 1:** Clear the Master Bus Collision Detect (BCL bit (I2CxSTAT<10>) after the bus returns to an Idle state. The software can monitor the S bit (I2CxSTAT<3>) and the P (I2CxSTAT<4>) bit to wait for an Idle bus. When the software services the bus collision Interrupt Service Routine and the I²C bus is free, the software can resume communication by asserting a new Start condition.

- **False Error Condition 2:** Clear the Receive Overflow Status flag I2COV bit (I2CxSTAT<20>), and then resume normal operation.

- **False Error Condition 3:** Initialize a Timer to slightly greater than the worst case I²C transaction cycle, (i.e., from Start-to-Stop, including the sum of all other application PC flow latencies, calls, interrupts, etc.). Exact timing is not required, rather just long enough so that a normal transaction is not interrupted. Prior to the beginning of each transaction, start the timer. Be sure to stop and reset the timer after completion of each successful I²C transaction. During the Timer interrupt (i.e., the I²C transaction has timed out), disable the I²C module by setting the ON bit (I2CxCON<15>) = 0. After disabling the module, wait 4 instruction cycles, after which time the I2CxSTAT register will automatically be cleared. Re-enable the I²C module by setting the ON bit = 1 and resume normal operation.

### Work around 2

Instead of using the hardware I²C module, use a software “bit-bang” implementation.

### Affected Silicon Revisions

<table>
<thead>
<tr>
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</table>

10. Module: ADC
   The ADC Group Early Interrupt (IRQ 205) feature is not functional.
   **Work around**
   Use individual ADC Early Interrupts (IRQ 119 through IRQ 203 and IRQ 206).

   **Affected Silicon Revisions**
   | A1 | X |

11. Module: ADC
   The ADC level trigger will not perform burst conversions in Debug mode.
   **Work around**
   Do not use Debug mode with the ADC level trigger.

   **Affected Silicon Revisions**
   | A1 | X |

12. Module: ADC
   In Differential mode, code 3072 has a DNL of +3.
   **Work around**
   None.

   **Affected Silicon Revisions**
   | A1 | X |

13. Module: ADC
   Turbo mode is not functional when two channels are linked for the purpose of increasing throughput.
   **Work around**
   None.

   **Affected Silicon Revisions**
   | A1 | X |

14. Module: SDHC
   The SDHC module requires the System PLL to be turned ON.
   **Work around**
   PLL should be enabled before using the SD Host Controller (SDHC) module.

   **Affected Silicon Revisions**
   | A1 | X |

15. Module: SDHC
   The SDHC module may not function if the SDCD pin is not used.
   **Work around 1**
   Set CDSSEL (SDHCCON1<7>) to ‘1’ and CDTLVL (SDHCCON1<6>) to ‘0’.

   **Work around 2**
   Ensure that the SDCD pin is used and driven to a low state externally.

   **Affected Silicon Revisions**
   | A1 | X |

16. Module: SDHC
   Card-detect status indication through the CDSLVL bit (SDHCSTAT1<18>) is inverted.
   **Work around 1**
   Use ACM42 to detect the card’s presence.

   **Work around 2**
   If SDCD is used for card detect, add a software work around to invert the CDSLVL (SDHCSTAT1<18>) state.

   **Affected Silicon Revisions**
   | A1 | X |
17. Module: SDHC
Write-protect status indication through the WPSLVL bit (SDHCSTAT1<19>) is inverted.

**Work around**
If SDWP is used for Write-protect, add a software work around to invert WPSLVL (SDHCSTAT1<19>) state.

**Affected Silicon Revisions**

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</table>

18. Module: SDHC
The Stop at Block Gap feature of the SDHC module is not functional.

**Work around**
None.

**Affected Silicon Revisions**

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</table>

19. Module: HLVD
High/Low-Voltage Detect module is not functional.

**Work around**
None.

**Affected Silicon Revisions**

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</table>

20. Module: DDR2C
DDR2 is functional only between 0°C and 70°C.

**Work around**
None.

**Affected Silicon Revisions**

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<tr>
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</table>

21. Module: DDR2C
Internal DDRVREF circuit (voltage divider) is not functional.

**Work around**
Use external voltage divider circuit on the DDRVREF pin to track VDDR1V8/2. Make sure to set INTVREFCON<1:0> (CFGMPLL<7:6>) to 0'b00 before initializing DDR2.

**Affected Silicon Revisions**

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</table>

22. Module: SQI
SQI eXecute-In-Place (XIP) mode is not functional in cached memory space (KSEG2).

**Work around**
Use KSEG3 (uncached starts at 0xF0000000) address space to access SQI Flash in XIP mode.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th></th>
<th>A1</th>
<th>X</th>
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</table>

23. Module: USB
The USB General Event Interrupt (IRQ 132) is not persistent as expected. The module is not guaranteed to generate interrupts for USB bus events when a USB interrupt is already being processed.

**Work around**
Upon entering the Interrupt Service Routine, continue to process all USB module events till the USBIF bit in the USBCRCON register (USBCRCON<26>) is cleared by the hardware.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th></th>
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<th>X</th>
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</table>

24. Module: USB
The USB module does not support remote wake-up through the USBRIE bit (USBCRCON<1>.

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th></th>
<th>A1</th>
<th>X</th>
</tr>
</thead>
</table>
25. Module: System Bus

The ERRP (SBTxECON<24>) bit is not functional and should not be used.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | X |

26. Module: Crypto

The Crypto module cannot access data from Flash due to prefetch cache corruption. Both workarounds listed below do not impact CPU performance when L1 cache is used by CPU.

**Work around 1**

Disable predictive prefetching for all addresses except CPU instructions and data. This can be achieved by NOT setting PrefEn<1:0> (PRECON<5:4>) to 0'b11.

**Work around 2**

Set Flash Wait states using the PFMWS<2:0> bits (PRECON<2:0>) to greater than four.

**Affected Silicon Revisions**

| A1 | X |

27. Module: UART

Clearing the receive buffer overrun error through the OERR bit (UxSTA<1>) clears the receive buffer. This condition occurs when the RunOVF bit (UxMODE<16>) is set, and an overflow condition occurs.

**Work around**

When a receive buffer overrun error occurs, read the entire receive FIFO through the UxRXREG register before clearing the OERR (UxSTA<1>) bit.

**Affected Silicon Revisions**

| A1 | X |

28. Module: EBI

For Asynchronous NOR Flash, EBI internal clock specification, TEbICLK (EB10) is not met.

**Work around**

When asynchronous NOR is attached to EBI, the system frequency would have to be reduced to 180 MHz for it to properly function.

**Affected Silicon Revisions**

| A1 | X |

29. Module: CTMU

Edge Sequencing mode (EdGSEQEn (CTMUON<10>)) and Edge mode are not functional.

**Work around**

Use level modes.

**Affected Silicon Revisions**

| A1 | X |

30. Module: CTMU

When the TGEN bit is set, manual current sourcing (i.e. setting the EDG1STAT bit) from CTMU is not possible.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | X |

31. Module: Temperature Sensor

The temperature sensor is not functional.

**Work around**

None.

**Affected Silicon Revisions**

| A1 | X |
32. Module: ICSP
While programming/debugging the device through any PGECx/PGEDx pair, TDO will toggle.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<td>X</td>
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</table>

33. Module: PORTS

VIH specification of 0.65 * VDDIO is not met. Use VIH specification of 0.8 * VDDIO.

Work around
None.

Affected Silicon Revisions

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<thead>
<tr>
<th>A1</th>
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<tr>
<td>X</td>
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</table>

34. Module: Primary Oscillator

The Primary Oscillator (Posc) does not support Automatic Gain Control (AGC). Therefore, the POSCACGC bit (DEVCFG0/ADEVCFG0<27>) is not functional.

Work around
None.

Affected Silicon Revisions

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<tr>
<th>A1</th>
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<tr>
<td>X</td>
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</table>

35. Module: Primary Oscillator
The Primary Oscillator (Posc) does not support Automatic Gain Control (AGC). Therefore, the Primary Oscillator AGC Gain Search Step Settling Time Control bits, POSCAGCDLY<1:0> (DEVCFG0/ADEVCFG0<25:24>), are not functional.

Work around
None.

Affected Silicon Revisions

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<tr>
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<tr>
<td>X</td>
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</tbody>
</table>

36. Module: Primary Oscillator

The Fine Gain Control bits, POSCFGAIN<1:0> (DEVCFG0/ADEVCFG0<23-22>), are not functional.

Work around
None.

Affected Silicon Revisions

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<tr>
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<tr>
<td>X</td>
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</table>

37. Module: GPU

The GPU Run-time enable/disable feature is not functional. Therefore, the GPURESET bit (CFGCON2<0>) is not functional. The GPU is always enabled regardless of the value of the GPURESET bit.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
<tr>
<td>X</td>
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</table>

38. Module: SDHC

The SDHC write-protect polarity inversion feature is not functional. Therefore, the SDWPPOL bit (CFGCON2<2>) is not functional and should not be used.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tr>
<td>X</td>
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</tbody>
</table>
39. Module: PMP
The PMP Input Buffer ‘x’ Status Full bit, IB0F (PMSTAT<8>), and the Output Buffer Underflow Status bit, OBUF (PMSTAT<6>), are set as soon as the PMP is turned ON in Slave mode (i.e., PMPTTL bit (PMCON<10>) is equal to ‘1’).

Work around
During PMP slave mode initialization, and before PMP interrupts are enabled, clear the Input Buffer Full Flag (IB0F bit (PMSTAT<8>) and the Output Buffer Underflow Flag (OBUF bit (PMSTAT<6>)) when clearing any pending IFSx interrupt flags.

40. Module: I2C
When the I2C module is in Slave mode, Start and Restart Interrupts are not occurring or properly reflected in the IFSx flag bits.

Work around
Use software polling to test the I2C Start/Restart Status bit, S (I2CxSTAT<3>).

41. Module: Crypto
The output digest of a partial message cannot be used as the initial vector for continuing the cryptographic operation on the remainder of the message. The full message must be processed in one operation.

Work around
None.

42. Module: Crypto
The Crypto Engine does not support a Hash operation on an empty string (i.e., string with zero length). The Crypto Engine times out and does not return a valid hash.

Work around
Use the fixed known hash of the empty string.

43. Module: CTMU
If the ADC module is enabled in Idle mode, it should override the setting of the CTMUSIDL bit (CTMU<CON<13>) = 1 (i.e., discontinue CTMU module operation when the device enters Idle mode), and if the ADC module attempts to make a CTMU temperature sensor measurement. However, it cannot because CTMU current sources aren’t enabled in Idle mode.

Work around
Set the CTMUSIDL bit to ‘0’ to continue module operation when the device enters Idle mode.

44. Module: Timer1
In Asynchronous external counter mode, (i.e., TCS bit (T1CON<1> = 1), TSYNC bit (T1CON<2> = 0), and TECS<1:0> (T1CON<9:8> = '0b01)), Timer1 does not reflect the first count from an external T1CLK input.

Work around
None.
45. Module: Timer1
The Timer1 register (TMR1) in Asynchronous external counter mode, (i.e., TCS bit (T1CON<1> = 1), TSYNC bit (T1CON<2> = 0), and TECS<1:0> (T1CON<9:8> = '0b01)), remains at the initial set value for five external clock pulses after wake-up from Sleep mode.

Work around
None.

Affected Silicon Revisions

| A1 | X |

46. Module: Timer1
Timer1 counts beyond the period value in Asynchronous mode when the period is 0x01.

Work around
Set the Timer1 period, PR1, to a value greater than 1.

Affected Silicon Revisions

| A1 | X |

47. Module: Timer1
Timer1 does not work properly in Gated mode (i.e., TGATE bit (T1CON<7> = 1), TCS bit (T1CON<1> = 0) with the prescaler enabled (TCKPS<1:0> bits (T1CON<5:4>) = '0b00)).

Work around
None.

Affected Silicon Revisions

| A1 | X |

48. Module: Timer1
Back-to-back CPU writes to the TMR1 register are not allowed for at least four PBCLK cycles.

Work around
None.

Affected Silicon Revisions

| A1 | X |

49. Module: Timer1
The Asynchronous Timer Write Disable bits (TWDIS (TxCON<12>)) and the Asynchronous Timer Write In Progress bits (TWIP (TxCON<11>)) are not functional.

Work around
None.

Affected Silicon Revisions

| A1 | X |

50. Module: UART
The UART TX Stop bit duration is shorter than the expected in High-Speed mode (BRGH bit (UxMODE<3> = 1) for baud rates less than 7.5 Mbps.

Work around
For baud rates less than 7.5 Mbps, operate the UART in Standard-Speed mode, that is, BRGH bit (UxMODE<3> =0). For baud rates greater than 7.5 Mbps operate the UART in High-Speed mode, that is, BRGH bit (UxMODE<3> =1).

Affected Silicon Revisions

| A1 | X |

51. Module: Sleep
If the ON bit (PB5DIV<15> = 0), and PBCLK5 is disabled, there is a 3 mA increase in Sleep IPD current.

Work around
Do not disable PBCLK5 before entering Sleep mode.

Affected Silicon Revisions

| A1 | X |
52. Module: CFG
Unique ID, DEVSNx<31:0> is not programmed in the devices released earlier than trace code dated 1821xxx.

**Work around**
None.

**Affected Silicon Revisions**

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</table>

53. Module: EBI
The EBIRDYEN1 bit (CFGEBIC<25>), EBIRDYEN2 bit (CFGEBIC<26>), and EBIRDYEN3 bit (CFGEBIC<27>) are not functional and always set to ‘1’.

**Work around**
None.

**Affected Silicon Revisions**

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<td>A1</td>
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</table>

54. Module: \(^2\text{C}\)
The 7-bit address that matches the 10-bit upper address value (111_10xx) is not accepted regardless of the STRICT bit setting.

**Work around**
None.

**Affected Silicon Revisions**

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<table>
<thead>
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<tbody>
<tr>
<td>A1</td>
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<tr>
<td>X</td>
</tr>
</tbody>
</table>

55. Module: \(^2\text{C}\)
I^2C module does not meet low period of the SCL clock (\(t_{LOW}\)) parameter from \(^2\text{C}\) specification for clock frequency >= 400 kHz.

**Work around**
None.

**Affected Silicon Revisions**

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<td>A1</td>
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<td>X</td>
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</tbody>
</table>

56. Module: Input Capture
Debug breakpoints are not supported when using Input Capture with DMA.

**Work around**
None.

**Affected Silicon Revisions**

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<tr>
<td>A1</td>
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</table>

57. Module: SDHC
Data from the MMC card can not be read correctly when the block size is set smaller than 512 bytes (i.e., the BSIZE<9:0> bits (SDHCBLKCON<9:0>) are smaller than 0x200).

**Work around**
None.

**Affected Silicon Revisions**

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<table>
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<td>A1</td>
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<td>X</td>
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</tbody>
</table>

58. Module: Sleep
Multiple sleep attempts (i.e., WAIT instruction with the SLPEN bit (OSCCON<4>) = 1) which occur within 20 μs of awake event, before the CPU has fully awakened, can cause the CPU to stall until a Power-on Reset (POR) event.

**Work around**
Ensure that at least 20 μs elapse before attempting to put the CPU to sleep (WAIT instruction with the SLPEN bit (OSCCON<4>) =1) after it awakens from a previous sleep.

**Affected Silicon Revisions**

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<td>A1</td>
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</table>
59. Module: SPI

Just before the last block of a transmission is shifted out to the SPI pins, the SRMT bit may incorrectly indicate that the transmission is done. However, this does not affect the Transmit Buffer Empty Interrupt (STXISEL<1:0> bits (SPIxCON<3:2>) = 0).

Work around
Use the interrupt notification rather than polling the SRMT bit to determine when a transmission has completed.

60. Module: SQI

The CPU stalls if the SQI Special Function Registers are read before the REFCLKO2 clock is enabled.

Work around
None.

61. Module: Timer2-9

If timer match coincides with entry into Sleep mode, timer event triggers and interrupt may not occur.

Work around
None.

62. Module: Timer2-9

When timer operation is discontinued in Idle mode (i.e., the SIDL bit (TxCON<13>) is set), and timer match coincides with entry into Idle mode, timer event triggers and interrupt may not occur.

Work around
None.

63. Module: Timer2-9

On a debug breakpoint, TMRx register, x=2-9, may not be representative of the correct value.

Work around
None.

64. Module: USB

The USB Link Power Management (LPM) feature is not functional.

Work around
None.

65. Module: USB

The USB Host module does not send the correct resume signal on the USB bus on subsequent suspend or resume sequences.

Work around
None.
66. Module: USB
The USB Host module does not wake up CPU from sleep when a USB device is disconnected.

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>X</th>
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</table>

67. Module: USB
The USB Suspend/Resume Event through IRQ 103 is not functional.

**Work around**
Handle the USB Suspend/Resume event through the IRQ132 (USB General Event) and check the SUSPIF bit (USBCSR2<16>) and the RESUMEIF bit (USBCSR2<17>) to identify the correct event.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>X</th>
</tr>
</thead>
</table>
Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest revision of the device data sheet (DS60001361H):

Note: Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: 44.1 DC Characteristics:

   Corrections were made to **TABLE 44-3** for the Package Thermal Resistance.

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Symbol</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package Thermal Resistance, 169-pin LFBGA (11x11x1.4 mm)</td>
<td>8JA</td>
<td>25</td>
<td>—</td>
<td>°C/W</td>
<td>1</td>
</tr>
<tr>
<td>Package Thermal Resistance, 169-pin LFBGA (11x11x1.56 mm)</td>
<td>8JA</td>
<td>23.5</td>
<td>—</td>
<td>°C/W</td>
<td>1,2</td>
</tr>
<tr>
<td>Package Thermal Resistance, 176-pin L0FP (20x20x1.45 mm)</td>
<td>8JA</td>
<td>20</td>
<td>—</td>
<td>°C/W</td>
<td>1</td>
</tr>
<tr>
<td>Package Thermal Resistance, 176-pin L0FP (20x20x1.45 mm)</td>
<td>8JA</td>
<td>20</td>
<td>—</td>
<td>°C/W</td>
<td>1,2</td>
</tr>
<tr>
<td>Package Thermal Resistance, 288-pin LFBGA (15x15x1.4 mm)</td>
<td>8JA</td>
<td>22</td>
<td>—</td>
<td>°C/W</td>
<td>1</td>
</tr>
</tbody>
</table>

**Note 1:** Junction to ambient thermal resistance, Theta-JA (8JA) numbers are achieved by package simulations.

**Note 2:** Devices with internal DDR2 SDRAM.
APPENDIX A: REVISION HISTORY

Rev A Document (3/2017)

Rev B Document (12/2017)
Silicon issue 25. (System Bus) was updated.
Added silicon issues 34. (Primary Oscillator), 35. (Primary Oscillator), 36. (Primary Oscillator), 37. (GPU), 38. (SDHC), 39. (PMP), 40. (I²C), 41. (Crypto), 42. (Crypto), 43. (CTMU), 44. (Timer1), 45. (Timer1), 46. (Timer1), 47. (Timer1), 48. (Timer1), and 49. (Timer1).
Added data sheet clarifications, 1. (Comparator), 3. (Device Configuration Word 0 Registers (DEVCFG0/ADEVCFG0)), and 4. (Device Configuration Word 1 Registers (DEVCFG1/ADEVCFG1)).

Rev C Document (9/2018)
Added Silicon Issues 50. (UART), 51. (Sleep), and 52. (CFG).
Removed Previous Data Sheet Clarifications 1, 2, 3, and 4.
Added Data Sheet Clarification 1. (Comparator).

Rev D Document 6/2019
Added Silicon Issues 53. (EBI), 54. (I²C), 55. (I²C), 56. (Input Capture), 57. (SDHC), 58. (Sleep), 59. (SPI), 60. (SOI), 61. (Timer2-9), 62. (Timer2-9), 63. (Timer2-9), 64. (USB), 65. (USB), and 66. (USB).
Removed previous Data Sheet Clarifications for Module 1 Comparator.

Revision E Document 09/2019
The following silicon issue was updated with new verbiage: 23. Module: "USB".
Added Silicon Issue 67. Module: "USB".
Added Data Sheet Clarification: 1. Module: "44.1 DC Characteristics:"
Note the following details of the code protection feature on Microchip devices:

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