The PIC18F26/45/46Q10 devices that you have received conform functionally to the current device data sheet (DS40001996C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F26/45/46Q10 silicon.

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

### Table 1. Silicon Device Identification

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device ID</th>
<th>Revision ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC18F26Q10</td>
<td>0x7180</td>
<td>0xA045</td>
</tr>
<tr>
<td>PIC18F45Q10</td>
<td>0x7140</td>
<td>0xA045</td>
</tr>
<tr>
<td>PIC18F46Q10</td>
<td>0x7120</td>
<td>0xA045</td>
</tr>
</tbody>
</table>

**Important:** Refer to the Device/Revision ID section in the current “PIC18F2X/4XQ10 Memory Programming Specification” (DS40001874) for more detailed information on Device Identification and Revision IDs for your specific device.
Table 2. Silicon Issue Summary

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Item No.</th>
<th>Issue Summary</th>
<th>Affected Revisions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical Specifications</td>
<td>Sleep current</td>
<td>1.1.1</td>
<td>Higher current after DFM write</td>
<td>X</td>
</tr>
<tr>
<td>Resets</td>
<td>RMCLR Flag</td>
<td>1.2.1</td>
<td>POR may clear the RMCLR bit by mistake</td>
<td>X</td>
</tr>
<tr>
<td>CWG</td>
<td>Auto shutdown sources</td>
<td>1.3.1</td>
<td>CLC2 and CLC6 not available</td>
<td>X</td>
</tr>
<tr>
<td>ADCC</td>
<td>FVR reference</td>
<td>1.4.1</td>
<td>Missing codes when FVR used as reference</td>
<td>X</td>
</tr>
<tr>
<td>ADCC</td>
<td>Burst average</td>
<td>1.4.2</td>
<td>ADCNT may not increment</td>
<td>X</td>
</tr>
<tr>
<td>ADCC</td>
<td>ADCRC (FRC) oscillator</td>
<td>1.4.3</td>
<td>Oscillator continues to run in sleep after conversion</td>
<td>X</td>
</tr>
<tr>
<td>ADCC</td>
<td>ADC Conversions</td>
<td>1.4.4</td>
<td>Unreliable conversion results with fast falling slew rate</td>
<td>X</td>
</tr>
<tr>
<td>Windowed Watchdog Timer</td>
<td>Window Operation</td>
<td>1.5.1</td>
<td>Window feature of the WWDT does not operate correctly in DOZE mode</td>
<td>X</td>
</tr>
<tr>
<td>NVM</td>
<td>NVMERR</td>
<td>1.6.1</td>
<td>NVMERR bit is set by device Reset after being cleared by software</td>
<td>X</td>
</tr>
<tr>
<td>NVM</td>
<td>Self Writes</td>
<td>1.6.2</td>
<td>Do not write above 100° C</td>
<td>X</td>
</tr>
<tr>
<td>MSSP</td>
<td>SPI</td>
<td>1.7.1</td>
<td>SSPBUF may be corrupted by writes to other GPR/SFRs</td>
<td>X</td>
</tr>
<tr>
<td>Oscillator</td>
<td>HFINTOSC</td>
<td>1.8.1</td>
<td>5% variation over temperature range</td>
<td>X</td>
</tr>
</tbody>
</table>

**Note:** Only those issues indicated in the last column apply to the current silicon revision.
# Table of Contents

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Silicon Errata Issues</td>
<td>4</td>
</tr>
<tr>
<td>1.1. Module: Electrical Specifications</td>
<td>4</td>
</tr>
<tr>
<td>1.2. Module: Resets</td>
<td>4</td>
</tr>
<tr>
<td>1.3. Module: Complementary Waveform Generator (CWG)</td>
<td>5</td>
</tr>
<tr>
<td>1.4. Module: Analog-to-Digital Converter with Computation (ADCC)</td>
<td>5</td>
</tr>
<tr>
<td>1.5. Module: Windowed Watchdog Timer (WWDT)</td>
<td>6</td>
</tr>
<tr>
<td>1.6. Module: Nonvolatile Memory (NVM)</td>
<td>7</td>
</tr>
<tr>
<td>1.7. Module: Master Synchronous Serial Port (MSSP)</td>
<td>8</td>
</tr>
<tr>
<td>1.8. Module: Oscillator</td>
<td>8</td>
</tr>
<tr>
<td>2. Data Sheet Clarifications</td>
<td>10</td>
</tr>
<tr>
<td>2.1. None</td>
<td>10</td>
</tr>
<tr>
<td>3. Revision History</td>
<td>11</td>
</tr>
<tr>
<td>Microchip Devices Code Protection Feature</td>
<td>12</td>
</tr>
<tr>
<td>The Microchip Web Site</td>
<td>12</td>
</tr>
<tr>
<td>Customer Change Notification Service</td>
<td>12</td>
</tr>
<tr>
<td>Customer Support</td>
<td>12</td>
</tr>
<tr>
<td>Microchip Devices Code Protection Feature</td>
<td>13</td>
</tr>
<tr>
<td>Legal Notice</td>
<td>13</td>
</tr>
<tr>
<td>Trademarks</td>
<td>13</td>
</tr>
<tr>
<td>Quality Management System Certified by DNV</td>
<td>14</td>
</tr>
<tr>
<td>Worldwide Sales and Service</td>
<td>15</td>
</tr>
</tbody>
</table>
1. **Silicon Errata Issues**

   **Notice:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 **Module: Electrical Specifications**

1.1.1 **Sleep Current - Higher Sleep Current after DFM Write Operation**

When performing a DFM write operation during Sleep mode, once the write operation has completed, the system clock will stay active. This means that while the device remains in this state, a higher Sleep current will be experienced.

**Work around**
Once the DFM write operation is completed, wake the device out of Sleep mode and re-execute a new Sleep command.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A5</th>
<th>X</th>
</tr>
</thead>
</table>

1.2 **Module: Resets**

1.2.1 **RMCLR Flag in PCON0 Register by Mistake**

On an initial power-up of the device, or when executing a software Reset, the PCON0 flag bit for MCLR Reset (RMCLR) may be improperly cleared by a Power-on Reset (POR) or software Reset (RT), thereby indicating a false MCLR event.

**Work around**
None.

**Affected Silicon Revisions**

| A5 | X |
1.3 Module: Complementary Waveform Generator (CWG)

1.3.1 CWG Auto-Shutdown Sources
Shutdown sources AS6E (CLC2_out) and AS7E (CLC6_out) are not available.

Work around
Route the CLC output through PPS to an output pin and use the AS0E source selection (Pin selected by CWGxPPS) and PPS controls to select the same pin as the shutdown source.

Affected Silicon Revisions

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1.4 Module: Analog-to-Digital Converter with Computation (ADCC)

1.4.1 Missing Codes with FVR Reference
Using the FVR as the positive voltage reference for the ADC can cause an increase in missing codes.

Work around
Method 1:
Increase the bit conversion time, known as TAD, to 8 μs or higher.

Method 2:
Use $V_{DD}$ as the positive voltage reference to the ADC.

Affected Silicon Revisions

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1.4.2 ADC² Burst Average Mode
When the ADC² is operated in Burst Average mode (ADMD = 0b11 in the ADCON2 register) while enabling non-continuous operation and double-sampling (ADCONT = 0 in the ADCON0 register and ADDSEN = 1 in the ADCON1 register), the value in the ADCNT register does not increment beyond ‘0b1’ toward the value in the ADRPT register.

Work around
When operating the ADC² in Burst Average mode with double-sampling, enable continuous operation of the module (ADCONT = 1 in the ADCON0 register) and set the Stop-on-Interrupt bit (ADSOI bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and re-trigger ADC² as necessary.

If the CPU is in Low-Power Sleep mode, alternatively the ADC² in non-continuous Burst Average mode can be operated with single ADC conversion (ADDSEN = 0 in the ADCON1 register) compromising noise
immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

| A5 | X |

1.4.3 ADCRC (FRC) Oscillator Operation in Sleep

If the part is in Sleep and the ADCRC (FRC) oscillator is used as clock source to the ADC, the oscillator continues to run after the conversion is complete. This will increase the current consumption in Sleep mode. The oscillator will stop after the device exits Sleep mode and resumes normal code execution.

Work around

None.

Affected Silicon Revisions

| A5 | X |

1.4.4 Unreliable Conversion Results with Fast Falling Slew Rate

When the ADC input falls by greater than 3.2V, with a slew rate faster than -11V/μs, the next ADC conversion will have the MSb improperly set. This is likely to happen when the ADC input channel is switched from one with a high input level to another with a low input level.

Work around

When switching between input channels, discard the first conversion result after the switch. Subsequent conversions will not be affected.

Affected Silicon Revisions

| A5 | X |

1.5 Module: Windowed Watchdog Timer (WWDT)

1.5.1 Window Operation in DOZE Mode

When the Windowed mode of operation is enabled in DOZE mode, a window violation error is issued even though the window is open and has been armed. This condition occurs only when the window size is set to a value other than 100% open.

Work around

Method 1:

Use the Windowed mode of operation in any other than DOZE mode. If disabling the DOZE mode is not an option, use the WWDT module without the Window being enabled.
Method 2:
If the device is in DOZE mode, perform the arming process for the window in NORMAL mode and return to the DOZE mode.

Method 3:
If there is an ISR in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

## Affected Silicon Revisions

| A5 | X |

## 1.6 Module: Nonvolatile Memory (NVM)

### 1.6.1 NVMERR
When a Reset is issued while an NVM high voltage operation is in progress, the NVMERR bit in the NVMCON0 register is set as expected. After clearing the NVMERR bit, if a Reset reoccurs, the NVMERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the NVMERR condition.

#### Work around
None.

## Affected Silicon Revisions

| A5 | X |

### 1.6.2 PFM Writes above 100° Celsius
Do not perform write operations on the Program Flash Memory (PFM) when the temperature is above 100 degrees Celsius.

#### Work around
Perform PFM writes below 100 degrees Celsius.

## Affected Silicon Revisions

| A5 | X |
Module: Master Synchronous Serial Port (MSSP)

1.7.1 MSSP SPI Slave Mode

When operating in SPI Slave mode, if the incoming SCK clock signal arrives during any of the conditions below, the SSPBUF transmit Shift register may become corrupted. The transmitted slave byte cannot be ensured to be correct, and the state of the WCOL bit may or may not indicate a write collision.

These conditions include:
- A write to an SFR
- A write to RAM following an SFR read
- A write to RAM prior to an SFR read

Work around
Method 1 (Interrupt based using SSS):
1. Connect the SSS line to both the SSS input and either an INT or IOC input pin.
2. Enable INT or IOC interrupts (interrupt on falling edge if available, otherwise check that SSS == 0 when the interrupt occurs).
3. Load SSPBUF with the data to be transmitted.
4. Continue program execution.
5. When the Interrupt Service Routine (ISR) is invoked, do either of the following:
   5.1. Add a delay that ensures the first SCK clock will be complete, or
   5.2. Poll SSPSTAT.BF (while(BF == 0)) and wait for the transmission/reception to complete.

Method 2 (Bit polling based using SSS):
1. Load SSPBUF with the data to be transmitted.
2. Poll the SSS line and wait for the SSS to go active (while(!PORTx.SSS == 0)).
3. When SSS is active (SSS == 0), do either of the following:
   3.1. Add a delay that ensures the first SCK clock will be complete, or
   3.2. Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

Once one of these two methods are complete, it is safe to return to program execution.

Method 3 (SSS not available):
1. Load SSPBUF with the data to be transmitted.
2. Poll SSPSTAT.BF (while(BF == 0)), and wait for the transmission/reception to complete.

Affected Silicon Revisions

| A5 | X |

Module: Oscillator

1.8.1 Internal HFINTOSC Oscillator Varies Up To 5%

The internal HFINTOSC oscillator varies in frequency up to 5% over the voltage and temperature range.
Work around
For systems requiring more precision, use an external crystal or ceramic resonator in one of the External Oscillator modes.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A5</th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2. Data Sheet Clarifications

2.1 None

There are no known data sheet clarifications as of this publication date.
## 3. Revision History

<table>
<thead>
<tr>
<th>Doc Rev.</th>
<th>Date</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>B</td>
<td>05/2019</td>
<td>Added oscillator drift erratum. Removed data sheet clarifications.</td>
</tr>
<tr>
<td>A</td>
<td>03/2019</td>
<td>Initial document release.</td>
</tr>
</tbody>
</table>
Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

The Microchip Web Site

Microchip provides online support via our web site at http://www.microchip.com/. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user’s guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Customer Change Notification Service

Microchip’s customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.


Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
• Field Application Engineer (FAE)
• Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://www.microchip.com/support

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

• Microchip products meet the specification contained in their particular Microchip Data Sheet.
• Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
• There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
• Microchip is willing to work with the customer who is concerned about the integrity of their code.
• Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, Kleer, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTorch, SAM-BA, SpyNic, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.
ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.


SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2019, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

ISBN: 978-1-5224-4481-7

Quality Management System Certified by DNV

ISO/TS 16949
Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company’s quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001:2000 certified.
<table>
<thead>
<tr>
<th>AMERICAS</th>
<th>ASIA/PACIFIC</th>
<th>ASIA/PACIFIC</th>
<th>EUROPE</th>
</tr>
</thead>
</table>
| **Corporate Office**  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
http://www.microchip.com/support  
Web Address:  
www.microchip.com  
---  
**Atlanta**  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455  
**Austin, TX**  
Tel: 512-257-3370  
Fax: 512-257-3370  
**Chicago**  
Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075  
**Dallas**  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924  
**Detroit**  
Novi, MI  
Tel: 248-848-4000  
**Houston, TX**  
Tel: 281-894-5983  
**Indianapolis**  
Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453  
**Los Angeles**  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608  
**Raleigh, NC**  
Tel: 919-844-7510  
**New York, NY**  
Tel: 631-435-6000  
**San Jose, CA**  
Tel: 408-735-9110  
Tel: 408-436-4270  
**Canada - Toronto**  
Tel: 905-695-1980  
Fax: 905-695-2078  
---  
**Australia - Sydney**  
Tel: 61-2-9868-6733  
**China - Beijing**  
Tel: 86-10-8569-7000  
**China - Chengdu**  
Tel: 86-28-8665-5511  
**China - Chongqing**  
Tel: 86-23-8980-9588  
**China - Dongguan**  
Tel: 86-769-8702-9880  
**China - Guangzhou**  
Tel: 86-20-8755-8029  
**China - Hangzhou**  
Tel: 86-571-8792-8115  
**China - Hong Kong SAR**  
Tel: 852-2943-5100  
**China - Nanjing**  
Tel: 86-25-8473-2460  
**China - Qingdao**  
Tel: 86-632-8502-7355  
**China - Shanghai**  
Tel: 86-21-3326-8000  
**China - Shenyang**  
Tel: 86-24-2334-2829  
**China - Shenzhen**  
Tel: 86-755-8864-2200  
**China - Suzhou**  
Tel: 86-186-6233-1526  
**China - Wuhan**  
Tel: 86-27-5980-5300  
**China - Xian**  
Tel: 86-29-8833-7252  
**China - Xi men**  
Tel: 86-992-2388138  
**China - Zhuhai**  
Tel: 86-756-3210040  
**India - Bangalore**  
Tel: 91-80-3090-4444  
**India - New Delhi**  
Tel: 91-11-4160-8631  
**India - Pune**  
Tel: 91-20-4121-0141  
**Japan - Osaka**  
Tel: 81-6-6152-7160  
**Japan - Tokyo**  
Tel: 81-3-6880-3770  
**Korea - Daegu**  
Tel: 82-53-744-4301  
**Korea - Seoul**  
Tel: 82-2-554-7200  
**Malaysia - Kuala Lumpur**  
Tel: 60-3-7651-7906  
**Malaysia - Penang**  
Tel: 60-4-227-8870  
**Philippines - Manila**  
Tel: 63-2-634-9065  
**Singapore**  
Tel: 65-6334-8870  
**Taiwan - Hsin Chu**  
Tel: 886-3-577-8366  
**Taiwan - Kaohsiung**  
Tel: 886-7-213-7830  
**Taiwan - Taipei**  
Tel: 886-2-2508-8600  
**Thailand - Bangkok**  
Tel: 66-2-694-1351  
**Vietnam - Ho Chi Minh**  
Tel: 84-28-5448-2100  
---  
**Austria - Wels**  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393  
**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829  
**Finland - Espoo**  
Tel: 358-9-4520-820  
**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79  
**Germany - Garching**  
Tel: 49-8931-9700  
**Germany - Haan**  
Tel: 49-2128-3766400  
**Germany - Heilbronn**  
Tel: 49-7111-67-3636  
**Germany - Karlsruhe**  
Tel: 49-721-625370  
**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44  
**Germany - Rosenheim**  
Tel: 49-8031-354-560  
**Israel - Ra'anana**  
Tel: 972-9-744-7705  
**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-468781  
**Italy - Padova**  
Tel: 39-049-7625286  
**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340  
**Norway - Trondheim**  
Tel: 47-72884388  
**Poland - Warsaw**  
Tel: 48-22-3325737  
**Romania - Bucharest**  
Tel: 40-21-407-87-50  
**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91  
**Sweden - Gothenberg**  
Tel: 46-31-704-60-40  
**Sweden - Stockholm**  
Tel: 46-8-69000-4654  
**UK - Wokingham**  
Tel: 44-118-921-5800  
Fax: 44-118-921-5820