MXT57
Low Jitter, Temperature Compensated Crystal Oscillator

Features

• Output Frequency 2.5 MHz to 850 MHz
• Phase Noise as Low as 190 fs (fₒ = 156.25 MHz, Integration Bandwidth 1.875 MHz to 20 MHz)
• Ultra-Low Spurs (−100 dBc or Greater Typical)
• ±2.5 ppm over Voltage and Temperature
• Supports CMOS, LVPECL, LVDS, and HCSL Outputs
• 2.375V to 3.63V Supply Voltage
• Output Enable Option: Can be Ordered on Pin 1 or Pin 2
• Industry-Standard and Space-Saving 5.0 mm x 7.0 mm 6-Lead Package
• −40°C to +85°C Operating Temperature Range
• Pb-Free and RoHS Compliant
• Analog TCXO, No Phase Bumps during Temperature Transitions
• Short Production Lead Time

Applications

• 10/40/100G Ethernet
• SONET-Optical Communications
• PCIe Gen 3/4/5
• Fibre Channel/SAS
• CPRI/OBSAI, XAUI and Backplane SERDES

General Description

The MXT57 product line is a family of ultra-low jitter, industry standard TCXO that are designed to maximize performance in networking, storage, server, and telecommunications equipment.

The MXT57 is available in a 5 mm x 7 mm LLGA package. These devices are capable of ±2.5 ppm total stability across the −40°C to +85°C operating temperature range, using proven assembly methods that improve long term reliability and minimize aging drift compared to traditional TCXO assembly processes.

As a custom ASIC with programmable output format and OE options, these TCXOs can be configured to be footprint-compatible with any standard 6-pin TCXO available today. Standard options and frequencies are available.

Please visit http://clockworks.microchip.com/timing to select a combination of options to customize your product, print a specific data sheet, and order samples.

Functional Block Diagram
## Package Types

### MXT57 Pinout

<table>
<thead>
<tr>
<th>Pinout</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Enable Pin 1 Option</strong></td>
<td><strong>Enable Pin 2 Option</strong></td>
<td></td>
</tr>
<tr>
<td>OE</td>
<td>1</td>
<td>6</td>
</tr>
<tr>
<td>NC</td>
<td>2</td>
<td>5</td>
</tr>
<tr>
<td>GND</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>VDD</td>
<td>6</td>
<td>VDD</td>
</tr>
<tr>
<td>/Q</td>
<td>5</td>
<td>/Q</td>
</tr>
<tr>
<td>Q</td>
<td>4</td>
<td>Q</td>
</tr>
</tbody>
</table>
1.0  ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ......................................................................................................................................... –0.3V to + 4.0V
Input Voltage ......................................................................................................................................–0.3V to V_{DD} +0.3V
ESD Protection (HBM) .......................................................................................................................... 4 kV
ESD Protection (MM) .................................................................................................................................. 400V
ESD Protection (CDM) ........................................................................................................................... 1.5 kV

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

**TABLE 1-1: ELECTRICAL CHARACTERISTICS**

Electrical Characteristics: \( V_{DD} = 2.375\text{V} \) to 3.63V, \( T_A = –40°C \) to +85°C with output terminated per output logic type.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (^{\text{Note 1}})</td>
<td>( V_{DD} )</td>
<td>2.375</td>
<td>—</td>
<td>3.63</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>Supply Current</td>
<td>( I_{DD} )</td>
<td>—</td>
<td>—</td>
<td>95</td>
<td>mA</td>
<td>Output enabled LVCMOS (no load).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>120</td>
<td>130</td>
<td></td>
<td>LVPECL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>90</td>
<td>100</td>
<td></td>
<td>LVDS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>95</td>
<td>105</td>
<td></td>
<td>HCSL</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>60</td>
<td>—</td>
<td></td>
<td>Output disabled (Tri-state)</td>
</tr>
<tr>
<td>Frequency Stability</td>
<td>( \Delta f )</td>
<td>A = ±5</td>
<td>—</td>
<td>A = ±8</td>
<td>ppm</td>
<td>Inclusive of initial accuracy, temperature drift, aging, shock and vibration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>B = ±2.5</td>
<td>B = ±5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Start-up Time</td>
<td>( t_{SU} )</td>
<td>—</td>
<td>—</td>
<td>20</td>
<td>ms</td>
<td>From 90% ( V_{DD} ) to valid clock output, ( T = +25°C )</td>
</tr>
<tr>
<td>Input Logic Levels</td>
<td>( V_{IH} )</td>
<td>2</td>
<td>—</td>
<td>( V_{DD} +0.3 )</td>
<td>V</td>
<td>Input logic-high</td>
</tr>
<tr>
<td></td>
<td>( V_{IL} )</td>
<td>–0.3</td>
<td>—</td>
<td>0.8</td>
<td></td>
<td>Input logic-low</td>
</tr>
<tr>
<td>Enable Active High Option (^{\text{Note 2}})</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>kΩ</td>
<td>Pull-up resistor on Pin 1 or 2</td>
</tr>
<tr>
<td>Enable Active Low Option (^{\text{Note 3}})</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>—</td>
<td>kΩ</td>
<td>Pull-down resistor on Pin 1 or 2</td>
</tr>
<tr>
<td>LVCMOS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>( f_0 )</td>
<td>2.5</td>
<td>—</td>
<td>250</td>
<td>MHz</td>
<td>—</td>
</tr>
<tr>
<td>Integrated Phase Noise (Random)</td>
<td>( \phi_j )</td>
<td>—</td>
<td>450</td>
<td>—</td>
<td>( f_{\text{RMS}} )</td>
<td>12 kHz to 20 MHz @ 156.25 MHz</td>
</tr>
<tr>
<td>Output High Voltage</td>
<td>( V_{OH} )</td>
<td>( V_{DD} –0.8 )</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>( R_L = 50\Omega )</td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td>( V_{OL} )</td>
<td>—</td>
<td>—</td>
<td>0.6</td>
<td>mV</td>
<td>Single-ended</td>
</tr>
<tr>
<td>Output Rise/Fall Time</td>
<td>( t_r/t_f )</td>
<td>100</td>
<td>—</td>
<td>500</td>
<td>ps</td>
<td>—</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>SYM</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td>%</td>
<td>—</td>
</tr>
<tr>
<td>LVPECL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>( f_0 )</td>
<td>2.5</td>
<td>—</td>
<td>850</td>
<td>MHz</td>
<td>—</td>
</tr>
<tr>
<td>Integrated Phase Noise (Random)</td>
<td>( \phi_j )</td>
<td>—</td>
<td>480</td>
<td>—</td>
<td>( f_{\text{RMS}} )</td>
<td>12 kHz to 20 MHz @ 200 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>100</td>
<td>—</td>
<td></td>
<td>1.875 MHz to 20 MHz @ 200 MHz</td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Characteristics:** $V_{DD} = 2.375V$ to $3.63V$, $T_A = -40°C$ to $+85°C$ with output terminated per output logic type.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output High Voltage</td>
<td>$V_{OH}$</td>
<td>$V_{DD}-1.35$</td>
<td>$V_{DD}-1.01$</td>
<td>$V_{DD}-0.8$</td>
<td>V</td>
<td>$R_L = 50\Omega$</td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td>$V_{OL}$</td>
<td>$V_{DD}-2.0$</td>
<td>$V_{DD}-1.78$</td>
<td>$V_{DD}-1.6$</td>
<td>mV</td>
<td>Single-ended</td>
</tr>
<tr>
<td>Output Differential Voltage</td>
<td>$V_{OD}$</td>
<td>0.65</td>
<td>0.77</td>
<td>0.95</td>
<td>mV</td>
<td>—</td>
</tr>
<tr>
<td>Output Rise/Fall Time</td>
<td>$t_r/t_f$</td>
<td>85</td>
<td>—</td>
<td>350</td>
<td>ps</td>
<td>—</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>SYM</td>
<td>45</td>
<td>—</td>
<td>55</td>
<td>%</td>
<td>—</td>
</tr>
</tbody>
</table>

**LVDS**

- **Frequency** $f_0$ | 2.5 | — | 850 | MHz | — |
- **Integrated Phase Noise (Random)** $\phi_j$ | — | 430 | — | $f_{sRMS}$ |
- **Output High Voltage** $V_{OH}$ | 1.248 | 1.375 | 1.602 | V | — |
- **Output Low Voltage** $V_{OL}$ | 0.898 | 1.025 | 1.252 | mV | — |
- **Output Differential Voltage** $V_{OD}$ | 247 | 350 | 454 | mV | — |
- **Common Mode Output Voltage** $V_{CM}$ | 1.125 | 1.2 | 1.375 | mV | — |
- **Output Rise/Fall Time** $t_r/t_f$ | 100 | — | 400 | ps | — |
- **Duty Cycle** SYM | 45 | — | 55 | % | — |

**HCSL**

- **Frequency** $f_0$ | 2.5 | — | 850 | MHz | — |
- **Integrated Phase Noise (Random)** $\phi_j$ | — | 450 | — | $f_{sRMS}$ |
- **Output High Voltage** $V_{OH}$ | 660 | 700 | 850 | mV | — |
- **Output Low Voltage** $V_{OL}$ | — | 150 | 0 | 27 | mV | — |
- **Output Differential Voltage** $V_{OD}$ | — | 200 | 250 | mV | 20% to 80% |
- **Common Mode Output Voltage** $V_{CM}$ | 48 | — | 52 | mV | Differential |
- **Output Rise/Fall Time** $t_r/t_f$ | 150 | 300 | 450 | ps | — |
- **Duty Cycle** SYM | 48 | — | 52 | % | — |

**Note 1:** VDD Pin should have basic VDD filtering as shown in Figure Something.

2: Output is enabled if pad floated (not connected) or pulled high; output tri-stated if pulled low.

3: Output is enabled if pad floated (not connected) or pulled low; output tri-stated if pulled high.
### TEMPERATURE SPECIFICATIONS (Note 1)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Temperature Ranges</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$T_A$</td>
<td>–40</td>
<td>—</td>
<td>+85</td>
<td>°C</td>
<td>—</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>$T_J$</td>
<td>—</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td>—</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_S$</td>
<td>–65</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td>—</td>
</tr>
<tr>
<td>Soldering Temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>°C</td>
<td>10 sec. max.</td>
</tr>
<tr>
<td><strong>Package Thermal Resistance</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance from Junction to Ambient, LGA-6Ld</td>
<td>$\theta_{JA}$</td>
<td>—</td>
<td>53</td>
<td>°C/W</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., $T_A$, $T_J$, $\theta_{JA}$). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.
2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1 and Table 2-2.

### TABLE 2-1: PIN FUNCTION TABLE (ENABLE PIN 1 OPTION)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OE</td>
<td>I</td>
<td>Output Enable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Active-High and Active-Low options.</td>
</tr>
<tr>
<td>2</td>
<td>DNC</td>
<td>NC</td>
<td>Do not connect, leave floating.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground</td>
<td>Power supply ground.</td>
</tr>
<tr>
<td>4</td>
<td>Q</td>
<td>O</td>
<td>Clock output +.</td>
</tr>
<tr>
<td>5</td>
<td>/Q</td>
<td>O</td>
<td>Clock output –.</td>
</tr>
<tr>
<td>6</td>
<td>VDD</td>
<td>Power</td>
<td>Power supply.</td>
</tr>
</tbody>
</table>

### TABLE 2-2: PIN FUNCTION TABLE (ENABLE PIN 2 OPTION)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DNC</td>
<td>NC</td>
<td>Do not connect, leave floating.</td>
</tr>
<tr>
<td>2</td>
<td>OE</td>
<td>I</td>
<td>Output Enable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Active-High and Active-Low options.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground</td>
<td>Power supply ground.</td>
</tr>
<tr>
<td>4</td>
<td>Q</td>
<td>O</td>
<td>Clock output +.</td>
</tr>
<tr>
<td>5</td>
<td>/Q</td>
<td>O</td>
<td>Clock output –.</td>
</tr>
<tr>
<td>6</td>
<td>VDD</td>
<td>Power</td>
<td>Power supply.</td>
</tr>
</tbody>
</table>
3.0 PERFORMANCE CHARACTERISTICS

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

**FIGURE 3-1:** LVCMOS Output 125 MHz 1.875 MHz to 20 MHz, 154 fs.

**FIGURE 3-2:** LVCMOS Output 125 MHz 12 kHz to 20 MHz, 412 fs.
FIGURE 3-3: LVPECL Output 200 MHz 1.875 MHz to 20 MHz 169 fs.

FIGURE 3-4: LVPECL Output 200 MHz 12 kHz to 20 MHz, 428 fs.
**FIGURE 3-5:** HCSL Output 156.25 MHz 1.875 MHz to 20 MHz, 191 fs.

**FIGURE 3-6:** HCSL Output 156.25 MHz 12 kHz to 20 MHz, 449 fs.
FIGURE 3-7: Aging.

3-MXT573DBA-125M and 5-MXT573ABA-156.25M 6L MOLGA Frequency Monitor During Burn-In +85°C, 3.3V
4.0 OUTPUT WAVEFORM

FIGURE 4-1: Output Waveform: LVPECL, LVDS, HCSL, LVCMOS.

TABLE 4-1: OUTPUT VOLTAGE SWING

<table>
<thead>
<tr>
<th>Output Logic Protocol</th>
<th>Output Swing (Peak-to-Peak, Typical)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVCMOS</td>
<td>$V_{OH} - 3V, V_{OL} + 3V$</td>
</tr>
<tr>
<td>LVPECL</td>
<td>770 mV</td>
</tr>
<tr>
<td>LVDS</td>
<td>350 mV</td>
</tr>
<tr>
<td>HCSL</td>
<td>700 mV</td>
</tr>
</tbody>
</table>
5.0 SOLDER REFLOW PROFILE

FIGURE 5-1: Solder Reflow Profile.

TABLE 5-1: SOLDER REFLOW

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Refer to JSTD-020C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ramp-Up Rate (200°C to Peak Temp.)</td>
<td>3°C/sec. max.</td>
</tr>
<tr>
<td>Preheat Time 150°C to 200°C</td>
<td>60 to 180 sec.</td>
</tr>
<tr>
<td>Time Maintained above 217°C</td>
<td>60 to 150 sec.</td>
</tr>
<tr>
<td>Peak Temperature</td>
<td>255°C to 260°C</td>
</tr>
<tr>
<td>Time within 5°C of Actual Peak</td>
<td>20 to 40 sec.</td>
</tr>
<tr>
<td>Ramp-Down Rate</td>
<td>6°C/sec. max.</td>
</tr>
<tr>
<td>Time 25°C to Peak Temperature</td>
<td>8 minutes max.</td>
</tr>
</tbody>
</table>
## 6.0 ENVIRONMENTAL SPECIFICATIONS

### TABLE 6-1: ENVIRONMENTAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Shock</td>
<td>MIL-STD-883, Method 1011, Condition A</td>
</tr>
<tr>
<td>Moisture Resistance</td>
<td>MIL-STD-883, Method 1004</td>
</tr>
<tr>
<td>Mechanical Shock</td>
<td>MIL-STD-883, Method 2022, Condition C</td>
</tr>
<tr>
<td>Mechanical Vibration</td>
<td>MIL-STD-883, Method 2007, Condition B</td>
</tr>
<tr>
<td>Resistance to Soldering Heat</td>
<td>J-STD-020C, Table 5-2 Pb-free Devices (Except 2 Cycles Max)</td>
</tr>
<tr>
<td>Hazardous Substance</td>
<td>Pb-Free/RoHS/Green Compliant</td>
</tr>
<tr>
<td>Solderability</td>
<td>JESD22-B102-D Method 2 (Preconditioning E)</td>
</tr>
<tr>
<td>Terminal Strength</td>
<td>MIL-STD-883, Method 2004, Test Condition D</td>
</tr>
<tr>
<td>Gross Leak</td>
<td>MIL-STD-883, Method 1014, Condition C</td>
</tr>
<tr>
<td>Fine Leak</td>
<td>MIL-STD-883, Method 1014, Condition A2, $R_1 = 2 \times 10^{-8}$ ATM CC/S</td>
</tr>
<tr>
<td>Solvent Resistance</td>
<td>MIL-STD-202, Method 215</td>
</tr>
</tbody>
</table>
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

Legend:
- XX...X  Product code, customer-specific information, or frequency in MHz without printed decimal point
- Y  Year code (last digit of calendar year)
- YY  Year code (last 2 digits of calendar year)
- WW  Week code (week of January 1 is week ‘01’)
- NNN  Alphanumeric traceability code
- @3  Pb-free JEDEC® designator for Matte Tin (Sn)
- *  This package is Pb-free. The Pb-free JEDEC designator (@3) can be found on the outer packaging for this package.
- ●, ▲, ▼  Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (’') symbol may not be to scale.
6-Lead 7.0 mm x 5.0 mm LLGA Package Outline and Recommended Land Pattern

6-Lead Low Profile Land Grid Array [APA] - 7x5 mm Body (LLGA)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
6-Lead Low Profile Land Grid Array [APA] - 7x5 mm Body (LLGA)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

![Diagram of 6-Lead Low Profile Land Grid Array](image)

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension</td>
<td>LIMITS</td>
</tr>
<tr>
<td>Number of Terminals</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Substrate Thickness</td>
<td>A1</td>
</tr>
<tr>
<td>Mold Cap Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Pitch</td>
<td>E1</td>
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<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Terminal Width</td>
<td>b</td>
</tr>
<tr>
<td>Terminal Length</td>
<td>L</td>
</tr>
<tr>
<td>Pullback</td>
<td>L1</td>
</tr>
</tbody>
</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   - BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   - REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1071A Sheet 2 of 2
6-Lead Low Profile Land Grid Array [APA] - 7x5 mm Body (LLGA)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

Microchip Technology Drawing C04-3071A

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### Recommended Land Pattern

![Image of recommended land pattern]

### Dimension Limits

<table>
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<tr>
<th>Units</th>
<th>MILLIMETERS</th>
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<tbody>
<tr>
<td>Dimension Limits</td>
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<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width (X6)</td>
<td>X</td>
</tr>
<tr>
<td>Contact Pad Length (X6)</td>
<td>Y</td>
</tr>
<tr>
<td>Contact to Contact (X4)</td>
<td>G1</td>
</tr>
<tr>
<td>Contact to Contact (X3)</td>
<td>G2</td>
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</table>

### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
2. BSC: Basic Dimension. Theoretically exact value shown without tolerances.
APPENDIX A: REVISION HISTORY

Revision A (May 2018)

• Initial creation of MXT57 Microchip data sheet DS20006037A.
<table>
<thead>
<tr>
<th>PART NO.</th>
<th>XX</th>
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<th>XXXMXXX</th>
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<tr>
<td>Device</td>
<td>Crystal Frequency</td>
<td>Enable Pin Option</td>
<td>Output Logic Type</td>
<td>Output Frequency</td>
<td>Shipping</td>
</tr>
</tbody>
</table>

**Device:** MXT57: Low Jitter, Temperature Compensated Crystal Oscillator (6-Lead 7x5 LLGA)

**Crystal Frequency:** 5A (Example Only) = Selected by ClockWorks Configurator; Dependent on the ordered output frequency.

**Enable Pin Option:**
- B = Pin 1
- N = Pin 2

**Output Logic Type:**
(For Enable Pin 1)
- A = PECL (Active-High)
- B = LVDS (Active-High)
- C = CMOS (Active-High)
- D = HCSL (Active-High)
- F = PECL (Active-Low)
- G = LVDS (Active-Low)
- H = CMOS (Active-Low)
- J = HCSL (Active-Low)

(For Enable Pin 2)
- R = PECL (Active-High)
- S = LVDS (Active-High)
- T = CMOS (Active-High)
- U = HCSL (Active-High)
- L = PECL (Active-Low)
- M = LVDS (Active-Low)
- N = CMOS (Active-Low)
- P = HCSL (Active-Low)

**Output Frequency:** xxxMxxx = 2.5 MHz to 850 MHz

**Shipping:**
- TA = 43/Tube
- RA = 1,000/Reel

Please visit [http://clockworks.microchip.com/timing](http://clockworks.microchip.com/timing) to select a combination of options to customize your product, print a specific data sheet and order samples.

**Examples:**

a) MXT573ABF 100M000TA
   MXT57, 3A Crystal Frequency code, OE Pin 1, PECL (Active-Low), 100 MHz, 43/Tube.

b) MXT574DBC 33M5000RA
   MXT57, 4D Crystal Frequency code, OE Pin 1, CMOS (Active-High), 33.5 MHz, 1,000/Reel.

c) MXT575CNU 740M250TA
   MXT57, 5C Crystal Frequency code, OE Pin 2, HCSL (Active-High), 740.25 MHz, 43/Tube.

d) MXT577FNN 3M300000RA
   MXT57, 7F Crystal Frequency code, OE Pin 2, CMOS (Active-Low), 3.3 MHz, 1,000/Reel.

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
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