General Description

The Micrel MIC261201 is a constant-frequency, synchronous buck regulator featuring a unique adaptive on-time control architecture. The MIC261201 operates over an input supply range of 4.5V to 28V and provides a regulated output of up to 12A of output current. The output voltage is adjustable down to 0.8V with a guaranteed accuracy of ±1%, and the device operates at a switching frequency of 600kHz.

Micrel’s Hyper Speed Control™ architecture allows for ultra-fast transient response while reducing the output capacitance and also makes (High VIN)/(Low VOUT) operation possible. This adaptive tON ripple control architecture combines the advantages of fixed-frequency operation and fast transient response in a single device.

The MIC261201 offers a full suite of protection features to ensure protection of the IC during fault conditions. These include undervoltage lockout to ensure proper operation under power-sag conditions, internal soft-start to reduce inrush current, foldback current limit, “hiccup mode” short-circuit protection, and thermal shutdown. An open-drain Power Good (PG) pin is provided.

All support documentation can be found on Micrel’s web site at: www.micrel.com.

Features

- Hyper Speed Control™ architecture enables
  - High Delta V operation (VIN = 28V and VOUT = 0.8V)
  - Small output capacitance
- 4.5V to 28V voltage input
- 12A output current capability, up to 95% efficiency
- Adjustable output from 0.8V to 5.5V
- ±1% feedback accuracy
- Any Capacitor® Stable – zero-to-high ESR
- 600kHz switching frequency
- No external compensation
- Power Good (PG) output
- Foldback current-limit and “hiccup mode” short-circuit protection
- Supports safe startup into a pre-biased load
- −40°C to +125°C junction temperature range
- 28-pin 5mm × 6mm MLF® package

Applications

- Distributed power systems
- Communications/networking infrastructure
- Set-top box, gateways and routers
- Printers, scanners, graphic cards and video card

Typical Application

Efficiency (VIN = 12V) vs. Output Current

Hyper Speed Control, SuperSwitcher II, and Any Capacitor are trademarks of Micrel, Inc.
MLF and MicroLeadFrame are registered trademarks of Amkor Technology, Inc.
Ordering Information

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Voltage</th>
<th>Switching Frequency</th>
<th>Junction Temperature Range</th>
<th>Package</th>
<th>Lead Finish</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIC261201YJL</td>
<td>Adjustable</td>
<td>600kHz</td>
<td>-40°C to +125°C</td>
<td>28-Pin 5mm × 6mm MLF®</td>
<td>Pb-Free</td>
</tr>
</tbody>
</table>

Pin Configuration

![Pin Configuration Diagram]

Pin Description

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PVDD</td>
<td>5V Internal Linear Regulator (Output): PVDD supply is the power MOSFET gate drive supply voltage and created by internal LDO from VIN. When VIN &lt; +5.5V, PVDD should be tied to PVIN pins. A 2.2µF ceramic capacitor from the PVDD pin to PGND (pin 2) must be place next to the IC.</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>No Connect.</td>
</tr>
<tr>
<td>4, 9, 10, 11, 12</td>
<td>SW</td>
<td>Switch Node (Output): Internal connection for the high-side MOSFET source and low-side MOSFET drain. Due to the high speed switching on this pin, the SW pin should be routed away from sensitive nodes.</td>
</tr>
<tr>
<td>2, 5, 6, 7, 8, 21</td>
<td>PGND</td>
<td>Power Ground. PGND is the ground path for the MIC26903 buck converter power stage. The PGND pins connect to the low-side N-Channel internal MOSFET gate drive supply ground, the sources of the MOSFETs, the negative terminals of input capacitors, and the negative terminals of output capacitors. The loop for the power ground should be as small as possible and separate from the Signal ground (SGND) loop.</td>
</tr>
<tr>
<td>13,14,15,16,17,18,19</td>
<td>PVIN</td>
<td>High-Side N-internal MOSFET Drain Connection (Input): The PVIN operating voltage range is from 4.5V to 28V. Input capacitors between the PVIN pins and the power ground (PGND) are required and keep the connection short.</td>
</tr>
<tr>
<td>20</td>
<td>BST</td>
<td>Boost (Output): Bootstrapped voltage to the high-side N-channel MOSFET driver. A Schottky diode is connected between the PVDD pin and the BST pin. A boost capacitor of 0.1µF is connected between the BST pin and the SW pin. Adding a small resistor at the BST pin can slow down the turn-on time of high-side N-Channel MOSFETs.</td>
</tr>
<tr>
<td>22</td>
<td>CS</td>
<td>Current Sense (Input): The CS pin senses current by monitoring the voltage across the low-side MOSFET during the OFF-time. The current sensing is necessary for short circuit protection. In order to sense the current accurately, connect the low-side MOSFET drain to SW using a Kelvin connection. The CS pin is also the high-side MOSFET’s output driver return.</td>
</tr>
</tbody>
</table>
## Pin Description (Continued)

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>SGND</td>
<td>Signal ground. SGND must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer, see PCB layout guidelines for details.</td>
</tr>
<tr>
<td>24</td>
<td>FB</td>
<td>Feedback (Input): Input to the transconductance amplifier of the control loop. The FB pin is regulated to 0.8V. A resistor divider connecting the feedback to the output is used to adjust the desired output voltage.</td>
</tr>
<tr>
<td>25</td>
<td>PG</td>
<td>Power Good (Output): Open Drain Output. The PG pin is externally tied with a resistor to VDD. A high output is asserted when $V_{OUT} &gt; 92%$ of nominal.</td>
</tr>
<tr>
<td>26</td>
<td>EN</td>
<td>Enable (input): A logic level control of the output. The EN pin is CMOS-compatible. Logic high = enable, logic low = shutdown. In the off state, supply current of the device is greatly reduced (typically 5µA). The EN pin should not be left open.</td>
</tr>
<tr>
<td>27</td>
<td>VIN</td>
<td>Power Supply Voltage (Input): Requires bypass capacitor to SGND.</td>
</tr>
<tr>
<td>28</td>
<td>VDD</td>
<td>5V Internal Linear Regulator (Output): VDD supply is the power MOSFET gate drive supply voltage and the supply bus for the IC. VDD is created by internal LDO from $V_{IN}$. When $V_{IN} &lt; +5.5V$, VDD should be tied to PVIN pins. A 1.0µF ceramic capacitor from the VDD pin to PGND pins must be place next to the IC.</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings\(^{(1, 2)}\)

- \(P_{\text{Vin}}\) to \(P_{\text{GND}}\) \(-0.3\) V to +29 V
- \(V_{\text{IN}}\) to \(P_{\text{GND}}\) \(-0.3\) V to \(P_{\text{IN}}\)
- \(P_{\text{VDD}}, V_{\text{DD}}\) to \(P_{\text{GND}}\) \(-0.3\) V to +6 V
- \(V_{\text{SW}}, V_{\text{CS}}\) to \(P_{\text{GND}}\) \(-0.3\) V to \(P_{\text{IN}} + 0.3\) V
- \(V_{\text{BST}}\) to \(V_{\text{SW}}\) \(-0.3\) V to 6 V
- \(V_{\text{BST}}\) to \(P_{\text{GND}}\) \(-0.3\) V to 35 V
- \(V_{\text{FB}}, V_{\text{PG}}\) to \(P_{\text{GND}}\) \(-0.3\) V to \(V_{\text{DD}} + 0.3\) V
- \(P_{\text{GND}}\) to \(S_{\text{GND}}\) \(-0.3\) V to +0.3 V
- Junction Temperature \(+150^\circ\) C
- Storage Temperature \(T_{\text{S}}\) \(-65^\circ\) C to +150 \(^\circ\) C
- Lead Temperature (soldering, 10 sec) \(260^\circ\) C

Operating Ratings\(^{(3)}\)

- Supply Voltage \((\text{PVIN}, V_{\text{IN}})\) 4.5 V to 28 V
- \(P_{\text{VDD}}, V_{\text{DD}}\) Supply Voltage \((\text{PVDD}, V_{\text{DD}})\) 4.5 V to 5.5 V
- Enable Input \((V_{\text{EN}})\) \(0\) V to \(V_{\text{IN}}\)
- Junction Temperature \(T_{\text{J}}\) \(-40^\circ\) C to +125 \(^\circ\) C
- Maximum Power Dissipation \(\text{Note 4}\)
- Package Thermal Resistance\(^{(4)}\)
  5 mm x 6 mm MLF\(^{(5)}\) \((\theta_{Ja})\) \(28^\circ\) C/W

Electrical Characteristics\(^{(5)}\)

- \(P_{\text{Vin}} = V_{\text{IN}} = V_{\text{EN}} = 12\) V, \(V_{\text{BST}} - V_{\text{SW}} = 5\) V; \(T_{\text{A}} = 25^\circ\) C, unless noted. **Bold** values indicate \(-40^\circ\) C \(\leq T_{\text{J}} \leq +125^\circ\) C.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power Supply Input</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range ((\text{VIN}, \text{PVIN}))</td>
<td></td>
<td>4.5</td>
<td>28</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Quiescent Supply Current (V_{\text{FB}} = 1.5) V (non-switching)</td>
<td></td>
<td>730</td>
<td>1500</td>
<td>(\mu)A</td>
<td></td>
</tr>
<tr>
<td>Shutdown Supply Current (V_{\text{EN}} = 0) V</td>
<td></td>
<td>5</td>
<td>10</td>
<td>(\mu)A</td>
<td></td>
</tr>
<tr>
<td><strong>VDD Supply Voltage</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{\text{DD}}) Output Voltage (V_{\text{IN}} = 7) V to 28 V, (I_{\text{DD}} = 40) mA</td>
<td></td>
<td>4.8</td>
<td>5</td>
<td>5.4</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{DD}}) UVLO Threshold (V_{\text{DD}}) Rising</td>
<td></td>
<td>3.7</td>
<td>4.2</td>
<td>4.5</td>
<td>V</td>
</tr>
<tr>
<td>(V_{\text{DD}}) UVLO Hysteresis</td>
<td></td>
<td>400</td>
<td></td>
<td>mV</td>
<td></td>
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<tr>
<td>Dropout Voltage ((\text{VIN} - \text{VDD})) (I_{\text{DD}} = 25) mA</td>
<td></td>
<td>380</td>
<td>600</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td><strong>DC/DC Controller</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output-Voltage Adjust Range ((\text{VOUT}))</td>
<td></td>
<td>0.8</td>
<td></td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td><strong>Reference</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(0^\circ) C (\leq T_{\text{J}} \leq 85^\circ) C ((\pm)1.5%)</td>
<td></td>
<td>0.792</td>
<td></td>
<td>0.808</td>
<td>V</td>
</tr>
<tr>
<td>(-40^\circ) C (\leq T_{\text{J}} \leq 125^\circ) C ((\pm)2.0%)</td>
<td></td>
<td>0.788</td>
<td></td>
<td>0.812</td>
<td>V</td>
</tr>
<tr>
<td>Load Regulation (I_{\text{OUT}} = 0) A to 12 A (Continuous Mode)</td>
<td></td>
<td>0.25</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Line Regulation (V_{\text{IN}} = 4.5) V to 28 V</td>
<td></td>
<td>0.25</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>FB Bias Current (V_{\text{FB}} = 0.8) V</td>
<td></td>
<td>50</td>
<td></td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td><strong>Enable Control</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Logic Level High</td>
<td></td>
<td>1.8</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>EN Logic Level Low</td>
<td></td>
<td>0.6</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>EN Bias Current (V_{\text{EN}} = 12) V</td>
<td></td>
<td>6</td>
<td>30</td>
<td>(\mu)A</td>
<td></td>
</tr>
<tr>
<td><strong>Oscillator</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching Frequency ((\text{VFB} = 0) V)</td>
<td></td>
<td>450</td>
<td>600</td>
<td>750</td>
<td>kHz</td>
</tr>
<tr>
<td>Maximum Duty Cycle ((\text{VFB} = 1.0) V)</td>
<td></td>
<td>82</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Minimum Duty Cycle</td>
<td></td>
<td>0</td>
<td></td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Minimum Off-Time</td>
<td></td>
<td>300</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>
## Electrical Characteristics (Continued)

PVIN = VIN = VEN = 12V, VBST – VSW = 5V; TA = 25°C, unless noted. **Bold** values indicate –40°C ≤ TJ ≤ +125°C.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Soft-Start</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Soft-Start time</td>
<td></td>
<td></td>
<td>5</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td><strong>Short-Circuit Protection</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current-Limit Threshold</td>
<td>VFB = 0.8V, TJ = 25°C</td>
<td>18.75</td>
<td>26</td>
<td>33</td>
<td>A</td>
</tr>
<tr>
<td>Current-Limit Threshold</td>
<td>VFB = 0.8V, TJ = 125°C</td>
<td>17.36</td>
<td>26</td>
<td>33</td>
<td>A</td>
</tr>
<tr>
<td>Short-Circuit Current</td>
<td>VFB = 0V</td>
<td>6</td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td><strong>Internal FETs</strong></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Top-MOSFET RDS (ON)</td>
<td>ISW = 3A</td>
<td>13</td>
<td></td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>Bottom-MOSFET RDS (ON)</td>
<td>ISW = 3A</td>
<td>5.3</td>
<td></td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>SW Leakage Current</td>
<td>VEN = 0V</td>
<td>60</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>VIN Leakage Current</td>
<td>VEN = 0V</td>
<td>25</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td><strong>Power Good (PG)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PG Threshold Voltage</td>
<td>Sweep VFB from Low to High</td>
<td>85</td>
<td>92</td>
<td>95</td>
<td>%VOUT</td>
</tr>
<tr>
<td>PG Hysteresis</td>
<td>Sweep VFB from High to Low</td>
<td>5.5</td>
<td></td>
<td></td>
<td>%VOUT</td>
</tr>
<tr>
<td>PG Delay Time</td>
<td>Sweep VFB from Low to High</td>
<td>100</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>PG Low Voltage</td>
<td>Sweep VFB &lt; 0.9 x Vnom, IPG = 1mA</td>
<td>70</td>
<td>200</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td><strong>Thermal Protection</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Over-Temperature Shutdown</td>
<td>TJ Rising</td>
<td>160</td>
<td></td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Over-Temperature Shutdown Hysteresis</td>
<td></td>
<td></td>
<td>15</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

**Notes:**

1. Exceeding the absolute maximum rating may damage the device.
2. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
3. The device is not guaranteed to function outside operating range.
4. PD(ThetaJ) = (TJ(max) – TA)/ θJA, where θJA depends upon the printed circuit layout. A 5 square inch 4 layer, 0.62", FR-4 PCB with 2oz finish copper weight per layer is used for the θJA.
5. Specification for packaged product only.
6. Measured in test mode.
7. The maximum duty-cycle is limited by the fixed mandatory off-time tOFF of typically 300ns.
Typical Characteristics

- **VIN Operating Supply Current vs. Input Voltage**
- **VIN Shutdown Current vs. Input Voltage**
- **VDD Output Voltage vs. Input Voltage**
- **Feedback Voltage vs. Input Voltage**
- **Total Regulation vs. Input Voltage**
- **Current Limit vs. Input Voltage**
- **Switching Frequency vs. Input Voltage**
- **Enable Input Current vs. Input Voltage**
- **PG Threshold/VREF Ratio vs. Input Voltage**
Typical Characteristics (Continued)

**VIN Operating Supply Current vs. Temperature**

- **VIN** = 12V
- **VOUT** = 1.8V
- **IOUT** = 0A

**VIN Shutdown Current vs. Temperature**

- **VIN** = 12V
- **VOUT** = 0A
- **VEN** = 0V

**VIN UVLO Threshold vs. Temperature**

- **Rising**
- **Falling**
- **Hyst**

**Feedback Voltage vs. Temperature**

- **VIN** = 12V
- **VOUT** = 1.8V
- **IOUT** = 0A

**Load Regulation vs. Temperature**

- **VIN** = 12V
- **VOUT** = 1.8V
- **IOUT** = 0A to 12A

**Line Regulation vs. Temperature**

- **VIN** = 4.5V to 28V
- **VOUT** = 1.8V

**Switching Frequency vs. Temperature**

- **VIN** = 12V
- **VOUT** = 1.8V
- **IOUT** = 0A

**VDD vs. Temperature**

- **VIN** = 12V
- **VOUT** = 1.8V
- **IOUT** = 0A

**Current Limit vs. Temperature**

- **VIN** = 12V
- **VOUT** = 1.8V
Typical Characteristics (Continued)

**Efficiency vs. Output Current**

![Efficiency vs. Output Current Graph](image)

**Feedback Voltage vs. Output Current**

![Feedback Voltage vs. Output Current Graph](image)

**Output Voltage (VIN = 5V) vs. Output Current**

![Output Voltage vs. Output Current Graph](image)

**Line Regulation vs. Output Current**

![Line Regulation vs. Output Current Graph](image)

**Switching Frequency vs. Output Current**

![Switching Frequency vs. Output Current Graph](image)

**Output Voltage (VIN = 5V) vs. Output Current**

![Output Voltage vs. Output Current Graph](image)

**Efficiency (VIN = 5V) vs. Output Current**

![Efficiency vs. Output Current Graph](image)

**IC Power Dissipation (VIN = 5V) vs. Output Current**

![IC Power Dissipation vs. Output Current Graph](image)

**Die Temperature* (VIN = 5V) vs. Output Current**

![Die Temperature vs. Output Current Graph](image)
Typical Characteristics (Continued)

![Efficiency (VIN = 12V) vs. Output Current](image1)

![IC Power Dissipation (VIN = 12V) vs. Output Current](image2)

![Die Temperature* (VIN = 12V) vs. Output Current](image3)

![Efficiency (VIN = 24V) vs. Output Current](image4)

![IC Power Dissipation (VIN = 24V) vs. Output Current](image5)

![Die Temperature* (VIN = 24V) vs. Output Current](image6)

![Thermal Derating* vs. Ambient Temperature](image7)

![Thermal Derating* vs. Ambient Temperature](image8)

![Thermal Derating* vs. Ambient Temperature](image9)
Die Temperature*: The temperature measurement was taken at the hottest point on the MIC261201 case mounted on a 5 square inch 4 layer, 0.62", FR-4 PCB with 2oz finish copper weight per layer, see Thermal Measurement section. Actual results will depend upon the size of the PCB, ambient temperature and proximity to other heat emitting components.
Functional Characteristics
Functional Characteristics (Continued)

Enable Thresholds

Enable Thresholds

V_{IN} = 12V
V_{OUT} = 1.8V
I_{OUT} = 12A

V_{OUT} (1V/div)

V_{EN} (1V/div)

Time (10ms/div)

V_{IN} UVLO Thresholds

V_{IN} = 2V to 6V
V_{OUT} = 1.8V
I_{OUT} = 1A

V_{OUT} (1V/div)

V_{IN} (2V/div)

Time (20ms/div)

Power Up into Short Circuit

Power Up into Short Circuit

V_{IN} = 12V
V_{OUT} = 1.8V
I_{OUT} = Short

V_{OUT} (0.5V/div)

V_{IN} (10V/div)

I_{L} (5A/div)

Time (1ms/div)

Enabled into Short

Enabled into Short

V_{IN} = 12V
V_{OUT} = 1.8V
I_{OUT} = Short

V_{OUT} (0.5V/div)

V_{EN} (2V/div)

I_{L} (5A/div)

Time (400μs/div)

Short Circuit

Short Circuit

V_{IN} = 12V
V_{OUT} = 1.8V
I_{OUT} = 12A

V_{OUT} (1V/div)

I_{L} (5A/div)

Time (200μs/div)

Output Recovery from Short Circuit

Output Recovery from Short Circuit

V_{IN} = 12V
V_{OUT} = 1.8V
I_{OUT} = 12A

V_{OUT} (1V/div)

I_{L} (5A/div)

Time (2ms/div)
Functional Characteristics (Continued)

Peak Current Limit Threshold

Output Recovery from Thermal Shutdown

Switching Waveforms

Switching Waveforms; $I_{OUT} = 0A$

Transient Response

Time (40ms/div)

Time (2ms/div)

Time (1µs/div)

Time (1µs/div)

Time (200µs/div)
Functional Diagram

Figure 1. MIC261201 Block Diagram
Functional Description

The MIC261201 is an adaptive ON-time synchronous step-down DC/DC regulator with an internal 5V linear regulator and a Power Good (PG) output. It is designed to operate over a wide input voltage range from 4.5V to 28V and provides a regulated output voltage at up to 7A of output current. An adaptive ON-time control scheme is employed to obtain a constant switching frequency and to simplify the control compensation. Over-current protection is implemented without the use of an external sense resistor. The device includes an internal soft-start function which reduces the power supply input surge current at start-up by controlling the output voltage rise time.

Theory of Operation

The MIC261201 operates in a continuous mode as shown in Figure 1.

Continuous Mode

In continuous mode, the output voltage is sensed by the MIC261201 feedback (FB) pin via the voltage divider R1 and R2, and compared to a 0.8V reference voltage \( V_{REF} \) at the error comparator through a low gain transconductance (\( g_m \)) amplifier. If the feedback voltage decreases and the output of the \( g_m \) amplifier is below 0.8V, then the error comparator will trigger the control logic and generate an ON-time period. The ON-time period length is predetermined by the "FIXED \( t_{ON\_ESTIMATION} \) circuitry:

\[
t_{ON\_estimated} = \frac{V_{OUT}}{V_{IN} \times 600kHz}
\]

Eq. 1

where \( V_{OUT} \) is the output voltage and \( V_{IN} \) is the power stage input voltage.

At the end of the ON-time period, the internal high-side driver turns off the high-side MOSFET and the low-side driver turns on the low-side MOSFET. The OFF-time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the \( g_m \) amplifier is below 0.8V, the ON-time period is triggered and the OFF-time period ends. If the OFF-time period determined by the feedback voltage is less than the minimum OFF-time \( t_{OFF\( (min) \)} \), which is about 300ns, the MIC261201 control logic will apply the \( t_{OFF\( (min) \)} \) instead. \( t_{OFF\( (min) \)} \) is required to maintain enough energy in the boost capacitor (\( C_{BST} \)) to drive the high-side MOSFET.

The maximum duty cycle is obtained from the 300ns \( t_{OFF\( (min) \)} \):

\[
D_{max} = \frac{t_{S} \cdot t_{OFF\( (min) \)}}{t_{S}} = 1 \cdot \frac{300ns}{t_{S}}
\]

Eq. 2

where \( t_{S} = 1/600kHz = 1.66\mu s \).

It is not recommended to use MIC261201 with a OFF-time close to \( t_{OFF\( (min) \)} \) during steady-state operation. Also, as \( V_{OUT} \) increases, the internal ripple injection will increase and reduce the line regulation performance. Therefore, the maximum output voltage of the MIC261201 should be limited to 5.5V and the maximum external ripple injection should be limited to 200mV. Please refer to “Setting Output Voltage” subsection in Application Information for more details.

The actual ON-time and resulting switching frequency will vary with the part-to-part variation in the rise and fall times of the internal MOSFETs, the output load current, and variations in the \( V_{DD} \) voltage. Also, the minimum \( t_{ON} \) results in a lower switching frequency in high \( V_{IN} \) to \( V_{OUT} \) applications, such as 24V to 1.0V. The minimum \( t_{ON} \) measured on the MIC261201 evaluation board is about 100ns. During load transients, the switching frequency is changed due to the varying OFF-time.

To illustrate the control loop operation, we will analyze both the steady-state and load transient scenarios. Figure 2 shows the MIC261201 control loop timing during steady-state operation. During steady-state, the \( g_m \) amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple and the inductor current ripple, to trigger the ON-time period. The ON-time is predetermined by the \( t_{ON\_estimator} \). The termination of the OFF-time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when \( V_{FB} \) falls below \( V_{REF} \), the OFF period ends and the next ON-time period is triggered through the control logic circuitry.
Unlike true current-mode control, the MIC261201 uses the output voltage ripple to trigger an ON-time period. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough. The MIC261201 control loop has the advantage of eliminating the need for slope compensation.

In order to meet the stability requirements, the MIC261201 feedback voltage ripple should be in phase with the inductor current ripple and large enough to be sensed by the $g_m$ amplifier and the error comparator. The recommended feedback voltage ripple is 20mV~100mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the $g_m$ amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation. Please refer to “Ripple Injection” subsection in Application Information for more details about the ripple injection technique.

**V\textsubscript{DD} Regulator**

The MIC261201 provides a 5V regulated output for input voltage $V_{\text{IN}}$ ranging from 5.5V to 28V. When $V_{\text{IN}} < 5.5V$, $V_{\text{DD}}$ should be tied to PVIN pins to bypass the internal linear regulator.

**Soft-Start**

Soft-start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitor is charged up. A slower output rise time will draw a lower input surge current. The MIC261201 implements an internal digital soft-start by making the 0.8V reference voltage $V_{\text{REF}}$ ramp from 0 to 100% in about 5ms with 9.7mV steps. Therefore, the output voltage is controlled to increase slowly by a staircase $V_{\text{FB}}$ ramp. Once the soft-start cycle ends, the related circuitry is disabled to reduce current consumption. $V_{\text{DD}}$ must be powered up at the same time or after $V_{\text{IN}}$ to make the soft-start function correctly.

**Current Limit**

The MIC261201 uses the $R_{\text{DS(ON)}}$ of the internal low-side power MOSFET to sense over-current conditions. This method will avoid adding cost, board space and power losses taken by a discrete current sense resistor. The low-side MOSFET is used because it displays much lower parasitic oscillations during switching than the high-side MOSFET.
In each switching cycle of the MIC261201 converter, the inductor current is sensed by monitoring the low-side MOSFET in the OFF period. If the peak inductor current is greater than 26A, then the MIC261201 turns off the high-side MOSFET and a soft-start sequence is triggered. This mode of operation is called “hiccup mode” and its purpose is to protect the downstream load in case of a hard short. The load current-limit threshold has a fold back characteristic related to the feedback voltage as shown in Figure 4.

![Current Limit Threshold vs. Feedback Voltage](image)

**Figure 4. MIC261201 Current-Limit Foldback Characteristic**

**Power-Good (PG)**

The Power Good (PG) pin is an open drain output which indicates logic high when the output is nominally 92% of its steady state voltage. A pull-up resistor of more than 10kΩ should be connected from PG to VDD.

**MOSFET Gate Drive**

The Block Diagram (Figure 1) shows a bootstrap circuit, consisting of D1 (a Schottky diode is recommended) and C_{BST}. This circuit supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged, while the low-side MOSFET is on, and the voltage on the SW pin is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the MOSFET on. As the high-side MOSFET turns on, the voltage on the SW pin increases to approximately V_{IN}. Diode D1 is reverse biased and C_{BST} floats high while continuing to keep the high-side MOSFET on. The bias current of the high-side driver is less than 10mA so a 0.1μF to 1μF is sufficient to hold the gate voltage with minimal droop for the power stroke (high-side switching) cycle, i.e. ΔBST = 10mA x 1.67μs/0.1μF = 167mV. When the low-side MOSFET is turned back on, C_{BST} is recharged through D1.

A small resistor R_{G}, which is in series with C_{BST}, can be used to slow down the turn-on time of the high-side N-channel MOSFET.

The drive voltage is derived from the V_{DD} supply voltage. The nominal low-side gate drive voltage is V_{DD} and the nominal high-side gate drive voltage is approximately V_{DD} – V_{DIODE}, where V_{DIODE} is the voltage drop across D1. An approximate 30ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.
Application Information

Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak-to-peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak-to-peak ripple currents will also increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current. The inductance value is calculated by Equation 3:

\[
L = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{SW} \times 20\% \times I_{OUT(max)}} \quad \text{Eq. 3}
\]

where:

\[f_{SW} = \text{switching frequency, } 600\text{kHz}\]
\[20\% = \text{ratio of AC ripple current to DC output current}\]
\[V_{IN(max)} = \text{maximum power stage input voltage}\]

The peak-to-peak inductor current ripple is:

\[
\Delta L_{(pp)} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times f_{SW} \times L} \quad \text{Eq. 4}
\]

The peak inductor current is equal to the average output current plus one half of the peak-to-peak inductor current ripple.

\[
I_{L(pk)} = I_{OUT(max)} + 0.5 \times \Delta I_{L(pp)} \quad \text{Eq. 5}
\]

The RMS inductor current is used to calculate the \(i^2R\) losses in the inductor.

\[
I_{L(RMS)} = \sqrt{I_{OUT(max)}^2 + \frac{\Delta I_{L(pp)}^2}{12}} \quad \text{Eq. 6}
\]

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC261201 requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the copper losses can be a significant contributor. Core loss information is usually available from the magnetics vendor. Copper loss in the inductor is calculated by Equation 7:

\[
P_{INDUCTOR(Cu)} = I_{L(RMS)}^2 \times R_{WINDING} \quad \text{Eq. 7}
\]

The resistance of the copper wire, \(R_{WINDING}\), increases with the temperature. The value of the winding resistance used should be at the operating temperature.

\[
P_{WINDING(H)} = R_{WINDING(20°C)} \times (1 + 0.0042 \times (T_H - T_{20°C})) \quad \text{Eq. 8}
\]

where:

\(T_H = \text{temperature of wire under full load}\)
\(T_{20°C} = \text{ambient temperature}\)
\(R_{WINDING(20°C)} = \text{room temperature winding resistance (usually specified by the manufacturer)}\)

Output Capacitor Selection

The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Voltage and RMS current capability are two other important factors for selecting the output capacitor. Recommended capacitor types are ceramic, low-ESR aluminum electrolytic, OS-CON and POSCAP. The output capacitor's ESR is usually the main cause of the output ripple. The output capacitor ESR also affects the control loop from a stability point of view.
The maximum value of ESR is calculated:

\[
ESR_{\text{Cout}} \leq \frac{\Delta V_{\text{OUT(pp)}}}{\Delta I_{\text{L(pp)}}}
\]

Eq. 9

where:
\[
\Delta V_{\text{OUT(pp)}} = \text{peak-to-peak output voltage ripple}
\]
\[
\Delta I_{\text{L(pp)}} = \text{peak-to-peak inductor current ripple}
\]

The total output ripple is a combination of the ESR and output capacitance. The total ripple is calculated in Equation 10:

\[
\Delta V_{\text{OUT(pp)}} = \sqrt{\left(\frac{\Delta I_{\text{L(pp)}}}{C_{\text{OUT}} \times f_{\text{SW}} \times 8}\right)^2 + (\Delta I_{\text{L(pp)}} \times ESR_{\text{Cout}})^2}
\]

Eq. 10

where:
\[
D = \text{duty cycle}
\]
\[
C_{\text{OUT}} = \text{output capacitance value}
\]
\[
f_{\text{SW}} = \text{switching frequency}
\]

As described in the “Theory of Operation” subsection in the Functional Description section, the MIC261201 requires at least 20mV peak-to-peak ripple at the FB pin to make the \( g_m \) amplifier and the error comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitors value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection method should be applied to provide the enough feedback voltage ripple. Please refer to the “Ripple Injection” subsection for more details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic or OS-CON. The output capacitor RMS current is calculated in Equation 11:

\[
I_{\text{Cout(RMS)}} = \frac{\Delta I_{\text{L(pp)}}}{\sqrt{12}}
\]

Eq. 11

The power dissipated in the output capacitor is:

\[
P_{\text{DISS(Cout)}} = I_{\text{Cout(RMS)}}^2 \times ESR_{\text{Cout}}
\]

Eq. 12

Input Capacitor Selection

The input capacitor for the power stage input \( V_{\text{IN}} \) should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. A tantalum input capacitor’s voltage rating should be at least two times the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage de-rating. The input voltage ripple will primarily depend on the input capacitor’s ESR. The peak input current is equal to the peak inductor current, so:

\[
\Delta V_{\text{IN}} = I_{\text{L(pk)}} \times ESR_{\text{CIN}}
\]

Eq. 13

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak-to-peak inductor current ripple is low:

\[
I_{\text{CIN(RMS)}} \approx I_{\text{OUT(max)}} \times \sqrt{D \times (1-D)}
\]

Eq. 14

The power dissipated in the input capacitor is:

\[
P_{\text{DISS(CIN)}} = I_{\text{CIN(RMS)}}^2 \times ESR_{\text{CIN}}
\]

Eq. 15

Ripple Injection

The \( V_{FB} \) ripple required for proper operation of the MIC261201 \( g_m \) amplifier and error comparator is 20mV to 100mV. However, the output voltage ripple is generally designed as 1% to 2% of the output voltage. For a low output voltage, such as a 1V, the output voltage ripple is only 10mV to 20mV, and the feedback voltage ripple is less than 20mV. If the feedback voltage ripple is so small that the \( g_m \) amplifier and error comparator can’t sense it, then the MIC261201 will lose control and the output voltage is not regulated. In order to have some amount of \( V_{FB} \) ripple, a ripple injection method is applied for low output voltage ripple applications.
The applications are divided into three situations according to the amount of the feedback voltage ripple:

1. **Enough ripple at the feedback voltage due to the large ESR of the output capacitors.**

   As shown in Figure 5a, the converter is stable without any ripple injection. The feedback voltage ripple is:

   \[
   \Delta V_{FB(pp)} = \frac{R_2}{R_1 + R_2} \times ESR_{OUT} \times \Delta I_{L(pp)} \quad \text{Eq. 16}
   \]

   where \(\Delta I_{L(pp)}\) is the peak-to-peak value of the inductor current ripple.

2. **Inadequate ripple at the feedback voltage due to the small ESR of the output capacitors.**

   The output voltage ripple is fed into the FB pin through a feedforward capacitor \(C_{ff}\) in this situation, as shown in Figure 5b. The typical \(C_{ff}\) value is between 1nF and 100nF. With the feedforward capacitor, the feedback voltage ripple is very close to the output voltage ripple:

   \[
   \Delta V_{FB(pp)} \approx ESR \times \Delta I_{L(pp)} \quad \text{Eq. 17}
   \]

3. **Virtually no ripple at the FB pin voltage due to the very-low ESR of the output capacitors.**

   In this situation, the output voltage ripple is less than 20mV. Therefore, additional ripple is injected into the FB pin from the switching node SW via a resistor \(R_{inj}\) and a capacitor \(C_{inj}\), as shown in Figure 5c. The injected ripple is:

   \[
   \Delta V_{FB(pp)} = \frac{1}{f_{SW} \times \tau} \quad \text{Eq. 18}
   \]

   where:

   \(V_{IN}\) = Power stage input voltage
   \(D\) = duty cycle
   \(f_{SW}\) = switching frequency
   \(\tau\) = \((R_1/R_2/R_{inj}) \times C_{ff}\)

   In Equations 20 and 21, it is assumed that the time constant associated with \(C_{ff}\) must be much greater than the switching period:

   \[
   \frac{1}{f_{SW} \times \tau} = \frac{T}{\tau} \ll 1 \quad \text{Eq. 20}
   \]

   If the voltage divider resistors \(R_1\) and \(R_2\) are in the kΩ range, a \(C_{ff}\) of 1nF to 100nF can easily satisfy the large time constant requirements. Also, a 100nF injection capacitor \(C_{inj}\) is used in order to be considered as short for a wide range of the frequencies.
The process of sizing the ripple injection resistor and capacitors is:

**Step 1.** Select $C_{ff}$ to feed all output ripples into the feedback pin and make sure the large time constant assumption is satisfied. Typical choice of $C_{ff}$ is 1nF to 100nF if R1 and R2 are in kΩ range.

**Step 2.** Select $R_{inj}$ according to the expected feedback voltage ripple using Equation 22:

$$K_{div} = \frac{\Delta V_{FB(pp)}}{V_{IN}} \times \frac{f_{SW} \times \tau}{D \times (1-D)}$$

Eq. 21

Then the value of $R_{inj}$ is obtained as:

$$R_{inj} = (R1/R2) \times \left(1 - \frac{1}{K_{div}}\right)$$

Eq. 22

**Step 3.** Select $C_{inj}$ as 100nF, which could be considered as short for a wide range of the frequencies.

**Setting Output Voltage**

The MIC26603 requires two resistors to set the output voltage as shown in Figure 7.

The output voltage is determined by Equation 23:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

Eq. 23

where $V_{FB} = 0.8V$.

A typical value of R1 can be between 3kΩ and 10kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small, it will decrease the efficiency of the power supply, especially at light loads. Once R1 is selected, R2 can be calculated using:

$$R2 = \frac{V_{FB} \times R1}{V_{OUT} - V_{FB}}$$

Eq. 24

In addition to the external ripple injection added at the FB pin, internal ripple injection is added at the inverting input of the comparator inside the MIC261201, as shown in Figure 8. The inverting input voltage $V_{INJ}$ is clamped to 1.2V. As $V_{OUT}$ is increased, the swing of $V_{INJ}$ will be clamped. The clamped $V_{INJ}$ reduces the line regulation because it is reflected as a DC error on the FB terminal. Therefore, the maximum output voltage of the MIC261201 should be limited to 5.5V to avoid this problem.
Thermal Measurements
Measuring the IC’s case temperature is recommended to insure it is within its operating limits. Although this might seem like a very elementary task, it is easy to get erroneous results. The most common mistake is to use the standard thermal couple that comes with a thermal meter. This thermal couple wire gauge is large, typically 22 gauge, and behaves like a heatsink, resulting in a lower case measurement.

Two methods of temperature measurement are using a smaller thermal couple wire or an infrared thermometer. If a thermal couple wire is used, it must be constructed of 36 gauge wire or higher then (smaller wire size) to minimize the wire heat-sinking effect. In addition, the thermal couple tip must be covered in either thermal grease or thermal glue to make sure that the thermal couple junction is making good contact with the case of the IC. Omega brand thermal couple (5SC-TT-K-36-36) is adequate for most applications.

Wherever possible, an infrared thermometer is recommended. The measurement spot size of most infrared thermometers is too large for an accurate reading on a small form factor ICs. However, a IR thermometer from Optris has a 1mm spot size, which makes it a good choice for measuring the hottest point on the case. An optional stand makes it easy to hold the beam on the IC for long periods of time.
PCB Layout Guidelines

**Warning!!! To minimize EMI and output noise, follow these layout recommendations.**

PCB Layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal and return paths.

The following guidelines should be followed to insure proper operation of the MIC261201 regulator.

**IC**
- A 2.2\(\mu\)F ceramic capacitor, which is connected to the PVDD pin, must be located right at the IC. The PVDD pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the PVDD and PGND pins.
- A 1.0\(\mu\)F ceramic capacitor must be placed right between VDD and the signal ground SGND. The SGND must be connected directly to the ground planes. Do not route the SGND pin to the PGND Pad on the top layer.
- Place the IC close to the point-of-load (POL).
- Use fat traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

**Input Capacitor**
- Place the input capacitor next.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the PVIN pin and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In “Hot-Plug” applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the over-voltage spike seen on the input supply with power is suddenly applied.

**Inductor**
- Keep the inductor connection to the switch node (SW) short.
- Do not route any digital lines underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FB) pin.
- The CS pin should be connected directly to the SW pin to accurate sense the voltage across the low-side MOSFET.
- To minimize noise, place a ground plane underneath the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. It does not matter whether the IC or inductor is on the top or bottom as long as there is enough air flow to keep the power components within their temperature limits. The input and output capacitors must be placed on the same side of the board as the IC.

**Output Capacitor**
- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

**Optional RC Snubber**
- Place the RC snubber on either side of the board and as close to the SW pin as possible.
Figure 8. Schematic of MIC261201 Evaluation Board

(J11, R13, R15 are for testing purposes)
### Bill of Materials

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## Bill of Materials (Continued)

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<td>Micrel. Inc.(9)</td>
<td>28V, 12A Hyper Speed Control™ Synchronous DC/DC Buck Regulator</td>
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**Notes:**
1. AVX: [www.avx.com](http://www.avx.com).
3. TDK: [www.tdk.com](http://www.tdk.com).
4. EPCOS: [www.epcos.com](http://www.epcos.com).
5. SANYO: [www.sanyo.com](http://www.sanyo.com).
7. Vishay: [www.vishay.com](http://www.vishay.com).
8. Cooper Bussmann: [www.cooperbussmann.com](http://www.cooperbussmann.com).
PCB Layout Recommendations

Figure 9. MIC261201 Evaluation Board Top Layer

Figure 10. MIC261201 Evaluation Board Mid-Layer 1 (Ground Plane)
PCB Layout Recommendations (Continued)

Figure 11. MIC261201 Evaluation Board Mid-Layer 2

Figure 12. MIC261201 Evaluation Board Bottom Layer
Recommended Land and Solder Stencil Pattern

Red circle indicates Thermal Via. Size should be .300-.350 mm in diameter, 0.80 mm pitch, and it should be connected to GND plane for maximum thermal performance.

Green rectangle (with shaded area) indicates Solder Stencil Opening on exposed pad area. Sizes should be a) 1.55x1.20 mm, 1.75 mm pitch, b) 0.80x1.11 mm, 1.31 mm pitch, c) 0.50x1.11 mm, 1.31 mm pitch.
Package Information

28-Pin 5mm x 6mm MLF® (YJL)

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