MCP48CXBXX

8/10/12-Bit Digital-to-Analog Converters, 1 LSb INL
Single/Dual Voltage Outputs with SPI Interface

Features
• Memory Options:
  - Volatile Memory: MCP48CVBXX
  - Nonvolatile Memory: MCP48CMBXX
• Operating Voltage Range:
  - 2.7V to 5.5V – Full specifications
  - 1.8V to 2.7V – Reduced device specifications
• Output Voltage Resolutions:
  - 8-Bit: MCP48CXBX0X (256 steps)
  - 10-Bit: MCP48CXBX1X (1024 steps)
  - 12-Bit: MCP48CXBX2X (4096 steps)
• Nonvolatile Memory (MTP) Size: 32 Locations
• 1 LSb Integral Nonlinearity (INL) Specification
• DAC Voltage Reference Source Options:
  - Device VDD
  - External VREF pin (buffered or unbuffered)
  - Internal band gap (1.214V typical)
• Output Gain Options:
  - 1x (Unity)
  - 2x (available when not using internal VDD as voltage source)
• Power-on/Brown-out Reset (POR/BOR) Protection
• Power-Down Modes:
  - Disconnects output buffer (High-Impedance)
  - Selection of VOUT pull-down resistors (100 kΩ or 1 kΩ)
• SPI Interface:
  - Supports ‘00’ and ‘11’ modes
  - 50 MHz write speed
  - 25 MHz read speed
• Package Types:
  - Dual: 16-lead 3 x 3 QFN, 10-lead MSOP, 10-lead 3 x 3 DFN
  - Single: 16-lead 3 x 3 QFN, 10-lead MSOP, 10-lead 3 x 3 DFN
• Extended Temperature Range: -40°C to +125°C

Package Types

MCP48CXBX1 (Single)
MSOP-10, DFN-10 (3 x 3)

MCP48CXBX2 (Dual)
MSOP-10, DFN-10 (3 x 3)

QFN-16 (3 x 3)

Note 1: Exposed pad (substrate paddle).
2: This pin’s signal can be connected to DAC0 and/or DAC1.
MCP48CXBXX

General Description

The MCP48CXBXX are single and dual-channel 8-bit, 10-bit, and 12-bit buffered voltage output Digital-to-Analog Converters (DAC), with volatile or MTP memory and an SPI serial interface.

The MTP memory can be written by the user up to 32 times, for each specific register. It requires a high-voltage level on the HVC pin, typically 7.5V, in order to successfully program the desired memory location. The nonvolatile memory includes power-up output values, device configuration registers and general purpose memory.

The VREF pin, the device VDD or the internal band gap voltage can be selected as the DAC's reference voltage. When VDD is selected, VDD is internally connected to the DAC reference circuit.

When the VREF pin is used with an external voltage reference, the user can select between a gain of 1 or 2 and can have the reference buffer enabled or disabled. When the gain is 2, the VREF pin voltage should be limited to a maximum of VDD/2.

These devices have a four-wire SPI-compatible serial interface with speeds up to 50 MHz for write and 25 MHz for read operations.

Applications

• Set Point or Offset Trimming
• Sensor Calibration
• Low-Power Portable Instrumentation
• PC Peripherals
• Data Acquisition Systems

MCP48CVBX1 Block Diagram (Single-Channel Output)

Note 1: Available only on specific packages.
MCP48CXBXX

MCP48CVBX2 Block Diagram (Dual-Channel Output)

Note 1: Available only on specific packages.

2: On dual output devices, except those in a QFN16 package, the LAT0 pin is internally connected to LAT1 input of DAC1.

3: On dual output devices, except those in a QFN16 package, the VREF0 pin is internally connected to VREF1 input of DAC1.
## Family Device Features

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th># of Channels</th>
<th>Resolution (bits)</th>
<th>DAC Output POR/BOR Setting&lt;sup&gt;1&lt;/sup&gt;</th>
<th># of V&lt;sub&gt;REF&lt;/sub&gt; Inputs</th>
<th># of LAT&lt;sub&gt;Inputs&lt;/sub&gt;&lt;sup&gt;3&lt;/sup&gt;</th>
<th>Memory&lt;sup&gt;2&lt;/sup&gt;</th>
<th>GP MTP Locations</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP48CVB01</td>
<td>MSOP, QFN, DFN</td>
<td>1</td>
<td>8</td>
<td>7Fh</td>
<td>1</td>
<td>1</td>
<td>RAM</td>
<td>—</td>
</tr>
<tr>
<td>MCP48CVB11</td>
<td>MSOP, QFN, DFN</td>
<td>1</td>
<td>10</td>
<td>1FFh</td>
<td>1</td>
<td>1</td>
<td>RAM</td>
<td>—</td>
</tr>
<tr>
<td>MCP48CVB21</td>
<td>MSOP, QFN, DFN</td>
<td>1</td>
<td>12</td>
<td>7FFh</td>
<td>1</td>
<td>1</td>
<td>RAM</td>
<td>—</td>
</tr>
<tr>
<td>MCP48CVB02</td>
<td>QFN</td>
<td>2</td>
<td>8</td>
<td>7Fh</td>
<td>2</td>
<td>2</td>
<td>RAM</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>MSOP, DFN</td>
<td>2</td>
<td>8</td>
<td>7Fh</td>
<td>1</td>
<td>1</td>
<td>RAM</td>
<td>—</td>
</tr>
<tr>
<td>MCP48CVB12</td>
<td>QFN</td>
<td>2</td>
<td>10</td>
<td>1FFh</td>
<td>2</td>
<td>2</td>
<td>RAM</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>MSOP, DFN</td>
<td>2</td>
<td>10</td>
<td>1FFh</td>
<td>1</td>
<td>1</td>
<td>RAM</td>
<td>—</td>
</tr>
<tr>
<td>MCP48CVB22</td>
<td>QFN</td>
<td>2</td>
<td>12</td>
<td>7FFh</td>
<td>2</td>
<td>2</td>
<td>RAM</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>MSOP, DFN</td>
<td>2</td>
<td>12</td>
<td>7FFh</td>
<td>1</td>
<td>1</td>
<td>RAM</td>
<td>—</td>
</tr>
<tr>
<td>MCP48CMB01</td>
<td>MSOP, QFN, DFN</td>
<td>1</td>
<td>8</td>
<td>7Fh</td>
<td>1</td>
<td>1</td>
<td>MTP</td>
<td>8</td>
</tr>
<tr>
<td>MCP48CMB11</td>
<td>MSOP, QFN, DFN</td>
<td>1</td>
<td>10</td>
<td>1FFh</td>
<td>1</td>
<td>1</td>
<td>MTP</td>
<td>8</td>
</tr>
<tr>
<td>MCP48CMB21</td>
<td>MSOP, QFN, DFN</td>
<td>1</td>
<td>12</td>
<td>7FFh</td>
<td>1</td>
<td>1</td>
<td>MTP</td>
<td>8</td>
</tr>
<tr>
<td>MCP48CMB02</td>
<td>QFN</td>
<td>2</td>
<td>8</td>
<td>7Fh</td>
<td>2</td>
<td>2</td>
<td>MTP</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>MSOP, DFN</td>
<td>2</td>
<td>8</td>
<td>7Fh</td>
<td>1</td>
<td>1</td>
<td>MTP</td>
<td>8</td>
</tr>
<tr>
<td>MCP48CMB12</td>
<td>QFN</td>
<td>2</td>
<td>10</td>
<td>1FFh</td>
<td>2</td>
<td>2</td>
<td>MTP</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>MSOP, DFN</td>
<td>2</td>
<td>10</td>
<td>1FFh</td>
<td>1</td>
<td>1</td>
<td>MTP</td>
<td>8</td>
</tr>
<tr>
<td>MCP48CMB22</td>
<td>QFN</td>
<td>2</td>
<td>12</td>
<td>7FFh</td>
<td>2</td>
<td>2</td>
<td>MTP</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>MSOP, DFN</td>
<td>2</td>
<td>12</td>
<td>7FFh</td>
<td>1</td>
<td>1</td>
<td>MTP</td>
<td>8</td>
</tr>
</tbody>
</table>

**Note 1:** The factory default value.

**Note 2:** Each nonvolatile memory location can be written 32 times. For subsequent writes to the MTP, the device will ignore the commands and the memory will not be modified.

**Note 3:** If the product is a dual device and the package has only one LAT pin, it is associated with both DAC0 and DAC1.
1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

Voltage on VDD with respect to VSS ................................................................. -0.6V to +6.5V
Voltage on all pins with respect to VSS ......................................................... -0.6V to VDD+0.3V
Input Clamp Current, Iik (VI < 0, VI > VDD, VI > VPP on HV pins) ............. ±20 mA
Output Clamp Current, Iok (VO < 0 or VO > VDD) ........................................ ±20 mA
Maximum Current out of VSS pin (Single) .............................................. 50 mA
(Dual) ..................................................................................................... 100 mA
Maximum Current into VDD pin (Single) .............................................. 50 mA
(Dual) ..................................................................................................... 100 mA
Maximum Current sourced by the VOUT pin ........................................... 20 mA
Maximum Current sunk by the VOUT pin ............................................... 20 mA
Maximum Current sourced/sunk by the VREF(0) pin (in Band Gap mode) ......... 20 mA
Maximum Current sunk by the VREFx pin (when VREF is in Unbuffered mode) .... 175 µA
Maximum Current sourced by the VREFx pin ........................................... 20 µA
Maximum Current sunk by the VREF pin .................................................. 125 µA
Maximum Output Current sunk by SDO Output pin ................................. 25 mA
Maximum Output Current sourced by SDO Output pin .............................. 25 mA
Total Power Dissipation(†) ...................................................................... 400 mW
ESD Protection on all pins ................................................................. ≥ ±6 kV (HBM)
........................................................................................................ ≥ ±400V (MM)
........................................................................................................ ≥ ±2 kV (CDM)
Latch-Up (per JEDEC JESD78A) at +125°C ............................................ ±100 mA
Storage Temperature .......................................................................... -65°C to +150°C
Ambient Temperature with power applied ........................................... -55°C to +125°C
Soldering Temperature of leads (10 seconds) ................................................. +300°C
Maximum Junction Temperature (Tj) ...................................................... +150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is
a stress rating only and functional operation of the device at those or any other conditions above those indicated in the
operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods
may affect device reliability.

Note 1: Power dissipation is calculated as follows:
P_{DIS} = V_{DD} \times (I_{DD} - \sum I_{OH}) + \sum (V_{DD} - V_{OH}) \times I_{OH} + \sum (V_{OL} \times I_{OL})
### DC CHARACTERISTICS

**Standard Operating Conditions (unless otherwise specified):**
Operating Temperature: -40°C ≤ TA ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V<sub>DD</sub> = +2.7V to 5.5V, V<sub>REF</sub> = +1.000V to V<sub>DD</sub>, V<sub>SS</sub> = 0V, R<sub>L</sub> = 2 kΩ from V<sub>OUT</sub> to GND, C<sub>L</sub> = 100 pF.
Typical specifications represent values for V<sub>DD</sub> = 5.5V, T<sub>A</sub> = +25°C.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>2.7</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>DAC operation (reduced analog specifications) and Serial Interface</td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt; Voltage (rising) to ensure device Power-on Reset</td>
<td>V&lt;sub&gt;POR&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>1.75</td>
<td>V</td>
<td>RAM retention voltage (V&lt;sub&gt;RAM&lt;/sub&gt;) &lt; V&lt;sub&gt;POR&lt;/sub&gt; V&lt;sub&gt;DD&lt;/sub&gt; voltages greater than the V&lt;sub&gt;POR&lt;/sub&gt; limit ensure that the device is out of reset.</td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt; Voltage (falling) to ensure device Brown-out Reset</td>
<td>V&lt;sub&gt;BOR&lt;/sub&gt; V&lt;sub&gt;RAM&lt;/sub&gt;</td>
<td>—</td>
<td>1.61</td>
<td>V</td>
<td>RAM retention voltage (V&lt;sub&gt;RAM&lt;/sub&gt;) &lt; V&lt;sub&gt;BOR&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>V&lt;sub&gt;DD&lt;/sub&gt; Rise Rate to ensure Power-on Reset</td>
<td>V&lt;sub&gt;DDRR&lt;/sub&gt;</td>
<td>(Note 3)</td>
<td>V/ms</td>
<td>—</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; rising, V&lt;sub&gt;DD&lt;/sub&gt; &gt; V&lt;sub&gt;POR&lt;/sub&gt; Single Output</td>
<td></td>
</tr>
<tr>
<td>Power-on Reset to Output-Driven Delay (Note 2)</td>
<td>T&lt;sub&gt;POR2OD&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>130</td>
<td>µs</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; rising, V&lt;sub&gt;DD&lt;/sub&gt; &gt; V&lt;sub&gt;POR&lt;/sub&gt; Dual Output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>145</td>
<td>µs</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; rising, V&lt;sub&gt;DD&lt;/sub&gt; &gt; V&lt;sub&gt;POR&lt;/sub&gt; Dual Output</td>
</tr>
</tbody>
</table>

**Note 2** This parameter is ensured by characterization.
**Note 3** POR/BOR voltage trip point is not slope dependent. Hysteresis implemented with time delay.
**DC CHARACTERISTICS (CONTINUED)**

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_{DD} = +2.7V to 5.5V, V_{REF} = +1.000V to V_{DD}, V_{SS} = 0V,
R_L = 2 kΩ from V_{OUT} to GND, C_L = 100 pF.
Typical specifications represent values for V_{DD} = 5.5V, T_A = +25°C.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Current</td>
<td>I_{DD}</td>
<td>—</td>
<td>—</td>
<td>250</td>
<td>µA</td>
<td>Single 1 MHz, Serial Interface Active VRxB:VRxA = '10' (4), V_{OUT} is unloaded, V_{REF} = V_{DD} = 5.5V, Volatile DAC register = Midscale</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>700</td>
<td>µA</td>
<td>10 MHz (4), V_{OUT} is unloaded, V_{REF} = V_{DD} = 5.5V, Volatile DAC register = Midscale</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>2300</td>
<td>µA</td>
<td>50 MHz (4), V_{OUT} is unloaded, V_{REF} = V_{DD} = 5.5V, Volatile DAC register = Midscale</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>350</td>
<td>µA</td>
<td>Dual 1 MHz, V_{OUT} is unloaded, V_{REF} = V_{DD} = 5.5V, Volatile DAC register = Midscale</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>800</td>
<td>µA</td>
<td>10 MHz (4), V_{OUT} is unloaded, V_{REF} = V_{DD} = 5.5V, Volatile DAC register = Midscale</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>2400</td>
<td>µA</td>
<td>50 MHz (4), V_{OUT} is unloaded, V_{REF} = V_{DD} = 5.5V, Volatile DAC register = Midscale</td>
</tr>
<tr>
<td>LAT/HVC Pin Write Current (2)</td>
<td>I_{DD(MTP_WR)}</td>
<td>—</td>
<td>—</td>
<td>6.40</td>
<td>mA</td>
<td>Single 1 MHz, Serial Interface Inactive VRxB:VRxA = '10', V_{REF} = V_{DD} = 5.5V, SCK = SDI = V_{SS}, V_{OUT} is unloaded, Volatile DAC register = Midscale</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>6.40</td>
<td>mA</td>
<td>Dual 1 MHz, Serial Interface Inactive VRxB:VRxA = '10', V_{REF} = V_{DD} = 5.5V, SCK = SDI = V_{SS}, V_{OUT} is unloaded, Volatile DAC register = Midscale</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>6.40</td>
<td>mA</td>
<td>Dual 1 MHz, Serial Interface Inactive VRxB:VRxA = '10', V_{REF} = V_{DD} = 5.5V, SCK = SDI = V_{SS}, V_{OUT} is unloaded, Volatile DAC register = Midscale</td>
</tr>
</tbody>
</table>

**Note 2** This parameter is ensured by characterization.

**Note 4** Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = ‘10’.

**Note 5** The PDxB:PDxA = ‘01’, ‘10’, and ‘11’ configurations should have the same current.
### DC CHARACTERISTICS (CONTINUED)

**Standard Operating Conditions (unless otherwise specified):**
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.

- V_DD = +2.7V to 5.5V, V_REF = +1.000V to V_DD, V_SS = 0V,
- R_L = 2 kΩ from V_OUT to GND, C_L = 100 pF.

Typical specifications represent values for V_DD = 5.5V, T_A = +25°C.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor Ladder</td>
<td>R_L</td>
<td>63.9</td>
<td>71</td>
<td>78.1</td>
<td>kΩ</td>
<td>VRxB:VRxA = ‘10’, V_REF = V_DD</td>
</tr>
<tr>
<td>Resolution (# of Resistors and # of Taps) (see B.1 “Resolution”)</td>
<td>N</td>
<td>256</td>
<td>Taps</td>
<td>8-bit</td>
<td>No Missing Codes</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1024</td>
<td>Taps</td>
<td>10-bit</td>
<td>No Missing Codes</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4096</td>
<td>Taps</td>
<td>12-bit</td>
<td>No Missing Codes</td>
<td></td>
</tr>
<tr>
<td>Nominal V_OUT Match (see B.1 “Resolution”)</td>
<td></td>
<td>—</td>
<td>0.016</td>
<td>0.3%</td>
<td></td>
<td>1.8V ≤ V_DD ≤ 5.5V</td>
</tr>
<tr>
<td>V_OUT Tempco (see B.19 “VOUT Temperature Coefficient”)</td>
<td>ΔV_OUT/ΔT</td>
<td>—</td>
<td>3</td>
<td>ppm/°C</td>
<td>Code = Mid-scale (7Fh, 1FFh or 7FFh), VRxB:VRxA = ‘00’, ‘10’, and ‘11’</td>
<td></td>
</tr>
<tr>
<td>VREF Pin Input Voltage Range</td>
<td>V_REF</td>
<td>V_SS</td>
<td>V_DD</td>
<td>V</td>
<td>1.8V ≤ V_DD ≤ 5.5V (1)</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1**  This parameter is ensured by design.
**Note 2**  This parameter is ensured by characterization.
**Note 6**  Resistance is defined as the resistance between the V_REF pin (mode VRxB:VRxA = ‘10’) to V_SS pin. For dual-channel devices (MCP48CXBX2), this is the effective resistance of each resistor ladder. The resistance measurement is one of the two resistor ladders measured in parallel.
**Note 10**  Variation of one output voltage to mean output voltage for dual devices only.
### DC CHARACTERISTICS (CONTINUED)

**Standard Operating Conditions (unless otherwise specified):**
Operating Temperature: -40°C ≤ $T_A$ ≤ +125°C (Extended)

All parameters apply across the specified operating ranges unless noted.

$V_{DD}$ = +2.7V to 5.5V, $V_{REF}$ = +1.000V to $V_{DD}$, $V_{SS}$ = 0V,
$R_L$ = 2 kΩ from $V_{OUT}$ to GND, $C_L$ = 100 pF.

Typical specifications represent values for $V_{DD}$ = 5.5V, $T_A$ = +25°C.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zero-Scale Error (Code = 000h) (see B.5 “Zero-Scale Error (EZH)”)</td>
<td>$E_{ZS}$</td>
<td>—</td>
<td>—</td>
<td>0.375</td>
<td>LSb</td>
<td>8-bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>1.5</td>
<td>LSb</td>
<td>10-bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>6</td>
<td>LSb</td>
<td>12-bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 2.0 “Typical Performance Curves”</td>
</tr>
</tbody>
</table>

| Offset Error (see B.7 “Offset Error (EOS)”) | $E_{OS}$ | -6 | ±0.7 | +6 | mV | $V_{REF} = V_{DD}$, No Load. |

| Offset Voltage Temperature Coefficient$^{(2, 9)}$ | $V_{OSTC}$ | — | ±5 | — | μV/°C | |

| Full-Scale Error (see B.4 “Full-Scale Error (EFS)”) | $E_{FS}$ | — | — | 2.5 | LSb | 8-bit | $V_{REF} = V_{DD}$, No Load. |
| | | — | — | 9 | LSb | 10-bit | $V_{REF} = V_{DD}$, No Load. |
| | | — | — | 35 | LSb | 12-bit | $V_{REF} = V_{DD}$, No Load. |
| | | | | | | See Section 2.0 “Typical Performance Curves” |

| Gain Error (see B.9 “Gain Error (EG)”)$^{(7)}$ | $E_{G}$ | -1 | ±0.1 | +1 | % of FSR | 8-bit | $V_{REF} = V_{DD}$, No Load |
| | | -1 | ±0.1 | +1 | % of FSR | 10-bit | $V_{REF} = V_{DD}$, No Load |
| | | -1 | ±0.1 | +1 | % of FSR | 12-bit | $V_{REF} = V_{DD}$, No Load |

| Gain-Error Drift$^{(2)}$ (see B.10 “Gain Error Drift (EGD)”)$^{(9)}$ | $\Delta G/°C$ | — | -6 | — | ppm/°C | |

---

**Note 2** This parameter is ensured by characterization.

**Note 7** This gain error does not include the offset error.

**Note 9** Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.
DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ TA ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
VDD = +2.7V to 5.5V, VREF = +1.000V to VDD, VSS = 0V,
RL = 2 kΩ from VOUT to GND, CL = 100 pF.
Typical specifications represent values for VDD = 5.5V, TA = +25°C.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Unadjusted Error (see B.6 “Total Unadjusted Error (ET)”)[2, 9]</td>
<td>ET</td>
<td></td>
<td>0.75</td>
<td></td>
<td>LSb</td>
<td>8-bit VRxB:VRxA = ‘10’, G = ‘0’, VREF = VDD, No Load.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-2.5</td>
<td></td>
<td>0.75</td>
<td>LSb</td>
<td>8-bit VRxB:VRxA = ‘10’, G = ‘0’, VREF = VDD, No Load.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 2.0 “Typical Performance Curves”</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 2.0 “Typical Performance Curves”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-0.10</td>
<td></td>
<td></td>
<td>LSb</td>
<td>8-bit VRxB:VRxA = ‘10’, G = ‘0’, VREF = VDD, No Load.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+0.25</td>
<td></td>
<td>LSb</td>
<td>10-bit VRxB:VRxA = ‘10’, G = ‘0’, VREF = VDD, No Load.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 2.0 “Typical Performance Curves”</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 2.0 “Typical Performance Curves”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-0.1</td>
<td></td>
<td></td>
<td>LSb</td>
<td>8-bit VRxB:VRxA = ‘10’, G = ‘0’, VREF = VDD, No Load.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+0.25</td>
<td></td>
<td>LSb</td>
<td>10-bit VRxB:VRxA = ‘10’, G = ‘0’, VREF = VDD, No Load.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+1.0</td>
<td></td>
<td>LSb</td>
<td>12-bit VRxB:VRxA = ‘10’, G = ‘0’, VREF = VDD, No Load.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 2.0 “Typical Performance Curves”</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 2.0 “Typical Performance Curves”</td>
</tr>
</tbody>
</table>

Note 2  This parameter is ensured by characterization.
Note 9  Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.
DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
V_DD = +2.7V to 5.5V, V_REF = +1.000V to V_DD, V_SS = 0V,
R_L = 2 kΩ from V_OUT to GND, C_L = 100 pF.
Typical specifications represent values for V_DD = 5.5V, T_A = +25°C.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3 dB Bandwidth</td>
<td>BW</td>
<td>—</td>
<td>60</td>
<td>—</td>
<td>kHz</td>
<td>V_DD = 3.0V/+/-2V, V_REF = 3.0V/+/-2V, VRxB:VRxA = '1 0', Gx = '0'</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>35</td>
<td></td>
<td>kHz</td>
<td>V_DD = 3.5V/+/-1.5V, V_REF = 3.5V/+/-1.5V, VRxB:VRxA = '1 0', Gx = '1'</td>
</tr>
<tr>
<td>Output Amplifier (Op Amp)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Phase Margin(^{(1)})</td>
<td>PM</td>
<td>—</td>
<td>58</td>
<td>—</td>
<td>°C</td>
<td>R_L = ∞</td>
</tr>
<tr>
<td>Slew Rate</td>
<td>SR</td>
<td>—</td>
<td>0.15</td>
<td>—</td>
<td>V/µs</td>
<td>R_L = 2 kΩ</td>
</tr>
<tr>
<td>Load Regulation</td>
<td>—</td>
<td>—</td>
<td>130</td>
<td>—</td>
<td>µV/mA</td>
<td>1 mA &lt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>µV/mA</td>
<td>-6 mA &lt;</td>
</tr>
<tr>
<td>Short-Circuit Current</td>
<td>IS_C_OA</td>
<td>6</td>
<td>10</td>
<td>14</td>
<td>mA</td>
<td>Short to V_SS DAC code = Full Scale</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Settling Time(^{(8)})</td>
<td>I_SETTLING</td>
<td>—</td>
<td>16</td>
<td>—</td>
<td>µs</td>
<td>R_L = 2 kΩ</td>
</tr>
<tr>
<td>Internal Band Gap</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Band Gap Voltage</td>
<td>V_BG</td>
<td>1.180</td>
<td>1.214</td>
<td>1.260</td>
<td>V</td>
<td>1.8 &lt; V_DD &lt; 5.5V</td>
</tr>
<tr>
<td>Short Circuit Current</td>
<td>I_SC_BG</td>
<td>6</td>
<td>10</td>
<td>14</td>
<td>mA</td>
<td>Short to V_SS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Band Gap Voltage Temperature Coefficient</td>
<td>V_BGTC</td>
<td>—</td>
<td>16</td>
<td>—</td>
<td>ppm/°C</td>
<td>1.8V ≤ V_DD &lt; 5.5V</td>
</tr>
<tr>
<td>Band Gap mode V_REF pin load regulation</td>
<td>IBG</td>
<td>—</td>
<td>30</td>
<td>—</td>
<td>µV/mA</td>
<td>1 mA &lt;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>390</td>
<td>—</td>
<td>µV/mA</td>
<td>-6 mA &lt;</td>
</tr>
</tbody>
</table>

Note 1: This parameter is ensured by design.

Note 8: Within 1/2 LSb of the final value, when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in a 12-bit device.)
DC CHARACTERISTICS (CONTINUED)

Standard Operating Conditions (unless otherwise specified):
Operating Temperature: -40°C ≤ TA ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
VDD = +2.7V to 5.5V, VREF = +1.000V to VDD, VSS = 0V,
RL = 2 kΩ from VOUT to GND, CL = 100 pF.
Typical specifications represent values for VDD = 5.5V, TA = +25°C.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>External Reference (VREF)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Range(1)</td>
<td>VREF</td>
<td>VSS</td>
<td>—</td>
<td>VDD − 0.04</td>
<td>V</td>
<td>VRxB:VRxA = ‘10’ (Unbuffered mode)</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>CREF</td>
<td>—</td>
<td>—</td>
<td>29</td>
<td>pF</td>
<td>VRxB:VRxA = ‘10’ (Unbuffered mode)</td>
</tr>
<tr>
<td>Input Impedance</td>
<td>RL</td>
<td>—</td>
<td>—</td>
<td>See Resistor Ladder Resistance(6)</td>
<td>kΩ</td>
<td>2.7V &lt;= VDD &lt;= 5.5V, VRxB:VRxA = ‘10’ VREF = VDD</td>
</tr>
<tr>
<td>Current through VREF(1)</td>
<td>IREF</td>
<td>—</td>
<td>—</td>
<td>172.15</td>
<td>μA</td>
<td>Mathematically from RvREF(min) spec (at 5.5V)</td>
</tr>
<tr>
<td>Total Harmonic Distortion(1)</td>
<td>THD</td>
<td>—</td>
<td>-76</td>
<td>—</td>
<td>dB</td>
<td>VREF = 2.048V ± 0.1V, VRxB:VRxA = ‘10’, Gx = ‘0’, Frequency = 1 kHz</td>
</tr>
</tbody>
</table>

Dynamic Performance

| Major Code Transition Glitch (see B.14 “Major-Code Transition Glitch”) | —    | —    | 10   | —    | nV-s | 1 LSb change around major carry (7FFh to 800h) |
| Digital Feedthrough (see B.15 “Digital Feed-Through”)                 | —    | —    | <2   | —    | nV-s |                                               |

Note 1  This parameter is ensured by design.

Note 6  Resistance is defined as the resistance between the VREF pin (mode VRxB:VRxA = ‘10’) to VSS pin. For dual-channel devices (MCP48CXBX2), this is the effective resistance of each resistor ladder. The resistance measurement is one of the two resistor ladders measured in parallel.
**DC CHARACTERISTICS (CONTINUED)**

*Standard Operating Conditions (unless otherwise specified):*

Operating Temperature: \(-40°C \leq T_A \leq +125°C\) (Extended)

All parameters apply across the specified operating ranges unless noted.

\(V_{DD} = +2.7V\) to 5.5V, \(V_{REF} = +1.000V\) to \(V_{DD}\), \(V_{SS} = 0V\),

\(R_L = 2\ \text{k}\Omega\) from \(V_{OUT}\) to GND, \(C_L = 100\ \text{pF}\).

Typical specifications represent values for \(V_{DD} = 5.5V\), \(T_A = +25°C\).

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
</table>

| Schmitt Trigger High-Input Threshold | \(V_{IH}\) | 0.45 \(V_{DD}\) | — | — | \(V\) | 1.8V \(\leq V_{DD} \leq 5.5V\) (Allows 2.7V Digital \(V_{DD}\) with 5.5V Analog \(V_{DD}\) or 1.8V Digital \(V_{DD}\) with 3.0V Analog \(V_{DD}\)) |

| Schmitt Trigger Low-Input Threshold | \(V_{IL}\) | — | — | 0.2 \(V_{DD}\) | \(V\) |

| Hysteresis of Schmitt Trigger Inputs | \(V_{HYS}\) | — | 0.1 \(V_{DD}\) | — | \(V\) |

| Output Low Voltage (SDO) | \(V_{OL}\) | \(V_{SS}\) | — | 0.3 \(V_{DD}\) | \(V\) | \(I_{OL} = 200\ \mu A\) |

| Output High Voltage (SDO) | \(V_{OH}\) | 0.7 \(V_{DD}\) | — | \(V_{DD}\) | \(V\) | \(I_{OH} = -200\ \mu A\) |

| Input Leakage Current | \(I_{IL}\) | -1 | — | 1 | \(\mu A\) | \(V_{IN} = V_{DD}\) and \(V_{IN} = V_{SS}\) |

| Pin Capacitance | \(C_{IN}, C_{OUT}\) | — | 10 | — | \(pF\) |

**RAM Value**

<table>
<thead>
<tr>
<th>Value Range</th>
<th>N</th>
<th>0h</th>
<th>—</th>
<th>FFh</th>
<th>(\text{hex})</th>
<th>8-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0h</td>
<td>—</td>
<td>—</td>
<td>3FFh</td>
<td>(\text{hex})</td>
<td>10-bit</td>
</tr>
<tr>
<td></td>
<td>0h</td>
<td>—</td>
<td>—</td>
<td>FFFh</td>
<td>(\text{hex})</td>
<td>12-bit</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DAC Register POR/BOR Value</th>
<th>N</th>
<th>See Table 4-2</th>
<th>(\text{hex})</th>
<th>8-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>See Table 4-2</td>
<td>(\text{hex})</td>
<td>10-bit</td>
<td></td>
</tr>
<tr>
<td></td>
<td>See Table 4-2</td>
<td>(\text{hex})</td>
<td>12-bit</td>
<td></td>
</tr>
</tbody>
</table>

| PDCON Initial Factory Setting | — | See Table 4-2 | \(\text{hex}\) |

**Power Requirements**

<table>
<thead>
<tr>
<th>Power Supply Sensitivity (B.17 &quot;Power-Supply Sensitivity (PSS)&quot;)</th>
<th>PSS</th>
<th>—</th>
<th>0.001</th>
<th>0.0035</th>
<th>%/%</th>
<th>8-bit</th>
<th>Code = Midscale</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>10-bit</td>
<td>12-bit</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

© 2019 Microchip Technology Inc. DS20006160A-page 13
### DC CHARACTERISTICS (CONTINUED)

**Standard Operating Conditions (unless otherwise specified):**
Operating Temperature: -40°C ≤ TA ≤ +125°C (Extended)
All parameters apply across the specified operating ranges unless noted.
VDD = +2.7V to 5.5V, VREF = +1.000V to VDD, VSS = 0V,
RL = 2 kΩ from VOUT to GND, CL = 100 pF.
Typical specifications represent values for VDD = 5.5V, TA = +25°C.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>MTP Programming Voltage (Note 1)</td>
<td>VPG_MTP</td>
<td>2.0</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>HVC = VIH, -20°C ≤ TA ≤ +125°C</td>
</tr>
<tr>
<td>LAT/HVC pin Voltage for MTP Programming (High-Voltage Commands) (1)</td>
<td>VIHH</td>
<td>7.25</td>
<td>7.5</td>
<td>7.75V</td>
<td>V</td>
<td>The LAT/HVC pin will be at one of the three input levels (VIL, VIH or VIHH) (11) (\text{(1)})</td>
</tr>
<tr>
<td>Writes Cycles</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>32((12))</td>
<td>Cycles</td>
<td>Note 1</td>
</tr>
<tr>
<td>Data Retention</td>
<td>DR_MTP</td>
<td>10</td>
<td>—</td>
<td>—</td>
<td>Years</td>
<td>at +85°C ((1))</td>
</tr>
<tr>
<td>MTP Range</td>
<td>N</td>
<td>0h</td>
<td>—</td>
<td>FFh</td>
<td>hex</td>
<td>8-bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0h</td>
<td>—</td>
<td>3FFh</td>
<td>hex</td>
<td>10-bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0h</td>
<td>—</td>
<td>FFFh</td>
<td>hex</td>
<td>12-bit</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0000h</td>
<td>—</td>
<td>7FFFh</td>
<td>hex</td>
<td>All General Purpose Memory</td>
</tr>
<tr>
<td>Initial Factory Setting</td>
<td>N</td>
<td>See Table 4-2</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>MTP Programming Write Cycle Time</td>
<td>tWC(\text{(MTP)})</td>
<td>—</td>
<td>—</td>
<td>250</td>
<td>us</td>
<td>VDD = +2.0V to 5.5V, -20°C ≤ TA ≤ +125°C (\text{(Note 1)})</td>
</tr>
</tbody>
</table>

**Note 1** This parameter is ensured by design.

**Note 11** High voltage on the LAT/HVC pin must be limited to the command + programming time. After the programming cycle, the LAT/HVC pin voltage must be returned to 5.5V or lower.

**Note 12** After 32 MTP write cycles, writes are inhibited and the 32nd write value is retained (not corrupted).
DC Notes:

1. This parameter is ensured by design.
2. This parameter is ensured by characterization.
3. POR/BOR voltage trip point is not slope dependent. Hysteresis implemented with time delay.
4. Supply current is independent of current through the resistor ladder in mode VRxB:VRxA = ‘10’.
5. The PDxB:PDxA = ‘01’, ‘10’, and ‘11’ configurations should have the same current.
6. Resistance is defined as the resistance between the VREF pin (mode VRxB:VRxA = ‘10’) to VSS pin. For dual-channel devices (MCP48CXBX2), this is the effective resistance of each resistor ladder. The resistance measurement is one of the two resistor ladders measured in parallel.
7. This gain error does not include the offset error.
8. Within 1/2 LSb of the final value, when code changes from 1/4 to 3/4 of FSR. (Example: 400h to C00h in a 12-bit device.)
9. Code range dependent on resolution: 8-bit, codes 4 to 252; 10-bit, codes 16 to 1008; 12-bit, codes 64 to 4032.
10. Variation of one output voltage to mean output voltage for dual devices only.
11. High voltage on the LAT/HVC pin must be limited to the command + programming time. After the programming cycle, the LAT/HVC pin voltage must be returned to 5.5V or lower.
12. After 32 MTP write cycles, writes are inhibited and the 32nd write value is retained (not corrupted).
1.1 Timing Waveforms and Requirements

1.1.1 WIPER SETTLING TIME

**FIGURE 1-1:** $V_{OUT}$ Settling Time Waveforms.

**TABLE 1-1:** WIPER SETTLING TIMING

| Timing Characteristics | Standard Operating Conditions (unless otherwise specified):
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Operating Temperature: $-40°C \leq T_A \leq +125°C$ (Extended)</td>
</tr>
<tr>
<td></td>
<td>All parameters apply across the specified operating ranges unless noted.</td>
</tr>
<tr>
<td></td>
<td>$V_{DD} = +2.7\text{V}$ to $5.5\text{V}$, $V_{SS} = 0\text{V}$, $R_L = 2,$kΩ from $V_{OUT}$ to GND, $C_L = 100,$pF.</td>
</tr>
<tr>
<td></td>
<td>Typical specifications represent values for $V_{DD} = 5.5\text{V}$, $T_A = +25°C$.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OUT}$ Settling Time (see B.13 “Settling Time”)</td>
<td>$t_S$</td>
<td>—</td>
<td>16</td>
<td>—</td>
<td>µs</td>
<td>12-bit Code = 400h → C00h; C00h → 400h (Note 1)</td>
</tr>
</tbody>
</table>

**Note 1:** Within 1/2 LSb of final value when code changes from 1/4 to 3/4 of FSR.

1.1.2 LATCH PIN (LAT) TIMING

**FIGURE 1-2:** LAT Pin Waveforms.

**TABLE 1-2:** LAT PIN TIMING

| Timing Characteristics | Standard Operating Conditions (unless otherwise specified):
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Operating Temperature: $-40°C \leq T_A \leq +125°C$ (Extended)</td>
</tr>
<tr>
<td></td>
<td>All parameters apply across the specified operating ranges unless noted.</td>
</tr>
<tr>
<td></td>
<td>$V_{DD} = +2.7\text{V}$ to $5.5\text{V}$, $V_{SS} = 0\text{V}$, $R_L = 2,$kΩ from $V_{OUT}$ to GND, $C_L = 100,$pF.</td>
</tr>
<tr>
<td></td>
<td>Typical specifications represent values for $V_{DD} = 5.5\text{V}$, $T_A = +25°C$.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>LATx Pin Pulse Width</td>
<td>$t_{LAT}$</td>
<td>20</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>
1.1.3 RESET AND POWER-DOWN TIMING

**FIGURE 1-3:** Power-on and Brown-out Reset Waveforms.

**FIGURE 1-4:** SPI Power-Down Waveforms.

**TABLE 1-3: RESET AND POWER-DOWN TIMING**

| Timing Characteristics                  | Standard Operating Conditions (unless otherwise specified):  
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Operating Temperature: -40°C ≤ T_A ≤ +125°C (Extended)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>All parameters apply across the specified operating ranges unless noted. V_DD = +2.7V to 5.5V, V_SS = 0V, RL = 2 kΩ from V_OUT to GND, C_L = 100 pF. Typical specifications represent values for V_DD = 5.5V, T_A = +25°C.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
<th>Conditions</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power-on Reset Delay</td>
<td><em>TPOR2SIA</em></td>
<td>—</td>
<td>—</td>
<td>130</td>
<td>µs</td>
<td>Single V_DD transitions from V_DD(MIN) → V_POR</td>
<td>V_OUT disabled to V_OUT driven</td>
<td></td>
</tr>
<tr>
<td>(Note 1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Brown-out Reset Delay</td>
<td><em>tBORD</em></td>
<td>30</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td>V_DD transitions from V_DD(normal operation)→ &lt; V_BOR</td>
<td>V_OUT driven to V_OUT disabled</td>
<td></td>
</tr>
<tr>
<td>Power-Down Output</td>
<td><em>TPDE</em></td>
<td>—</td>
<td>1.5</td>
<td>—</td>
<td>µs</td>
<td>PDxB:PDxA = ‘11’, ‘10’, or ‘01’ → “00” started from the rising edge of the 24th SCK clock cycle; Volatile DAC Register = FFFh, V_OUT = 10 mV; V_OUT not connected.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enable Time Delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power-Down Output</td>
<td><em>TPDD</em></td>
<td>—</td>
<td>0.025</td>
<td>—</td>
<td>µs</td>
<td>PDxB:PDxA = “00” → ‘11’, ‘10’, or ‘01’ started from the rising edge of the 24th SCK clock cycle; V_OUT = V_OUT - 10 mV; V_OUT not connected.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Disable Time Delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: This parameter is ensured by characterization.
1.2 SPI Mode Timing Waveforms and Requirements

![SPI Timing Waveform](image)

**FIGURE 1-5:** SPI Timing Waveform (Mode = ‘11’).

**TABLE 1-4: SPI REQUIREMENTS (MODE = ‘11’)**

<table>
<thead>
<tr>
<th>#</th>
<th>Characteristic (2)</th>
<th>Sym.</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>SCK Input Frequency</td>
<td>F_{SCK}</td>
<td>—</td>
<td>25</td>
<td>MHz</td>
<td>(V_{DD} = 2.7 \text{V} to 5.5 \text{V} - \text{Read command, } C_L = 20 \text{pF})</td>
</tr>
<tr>
<td>—</td>
<td></td>
<td></td>
<td>—</td>
<td>50</td>
<td>MHz</td>
<td>(V_{DD} = 2.7 \text{V to 5.5 \text{V} - \text{Write commands, } C_L = 20 \text{pF}})</td>
</tr>
<tr>
<td>—</td>
<td></td>
<td></td>
<td>—</td>
<td>10</td>
<td>MHz</td>
<td>(V_{DD} = 1.8 \text{V to 2.7} \text{V})</td>
</tr>
<tr>
<td>70</td>
<td>CS Active (VIL) to SCK↑ Input</td>
<td>TcsA2scH</td>
<td>15</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>71</td>
<td>SCK Input High Time</td>
<td>TscH</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td>(V_{DD} = 2.7 \text{V to 5.5 \text{V}})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>—</td>
<td>ns</td>
<td>(V_{DD} = 1.8 \text{V to 2.7} \text{V})</td>
</tr>
<tr>
<td>72</td>
<td>SCK Input Low Time</td>
<td>TscL</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td>(V_{DD} = 2.7 \text{V to 5.5 \text{V}})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>—</td>
<td>ns</td>
<td>(V_{DD} = 1.8 \text{V to 2.7} \text{V})</td>
</tr>
<tr>
<td>73</td>
<td>SDI Input Valid to SCK↑ Edge (Setup Time)</td>
<td>TdiV2scH</td>
<td>5</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>74</td>
<td>SCK↑ Edge to SDI Input Invalid (Hold Time)</td>
<td>TscH2diL</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>77</td>
<td>CS Inactive (Vih) to SDO Output High-Impedance</td>
<td>TcsH2doZ</td>
<td>—</td>
<td>20</td>
<td>ns</td>
<td>\textbf{Note 1}</td>
</tr>
<tr>
<td>80</td>
<td>SCK↓ Edge to SDO Data Output Valid</td>
<td>TscL2dOV</td>
<td>—</td>
<td>20</td>
<td>ns</td>
<td>(V_{DD} = 2.7 \text{V to 5.5 \text{V}})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>35</td>
<td>ns</td>
<td>(V_{DD} = 1.8 \text{V to 2.7} \text{V})</td>
</tr>
<tr>
<td>83</td>
<td>SCK↑ Edge to CS Inactive (Vih) (Hold Time)</td>
<td>TscH2csI</td>
<td>15</td>
<td>—</td>
<td>ns</td>
<td>(V_{DD} = 2.7 \text{V to 5.5 \text{V}})</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>—</td>
<td>ns</td>
<td>(V_{DD} = 1.8 \text{V to 2.7} \text{V})</td>
</tr>
<tr>
<td>84</td>
<td>CS Input High Time</td>
<td>TcsA2csI</td>
<td>30</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>89</td>
<td>Delay from HVC VihH to First Command Byte (1)</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** This specification is ensured by design.

**Note 2:** This parameter is ensured by characterization.
### FIGURE 1-6: SPI Timing Waveform (Mode = 00).

### TABLE 1-5: SPI REQUIREMENTS (MODE = 00)

<table>
<thead>
<tr>
<th>#</th>
<th>Characteristic(2)</th>
<th>Sym.</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>SCK Input Frequency</td>
<td>( F_{SCK} )</td>
<td>—</td>
<td>25</td>
<td>MHz</td>
<td>( V_{DD} = 2.7\text{V} \text{ to } 5.5\text{V} \text{ - Read command, } C_L = 20 \text{ pF} )</td>
</tr>
<tr>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>MHz</td>
<td>( V_{DD} = 2.7\text{V} \text{ to } 5.5\text{V} \text{ - Write commands, } C_L = 20 \text{ pF} )</td>
</tr>
<tr>
<td>—</td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>MHz</td>
<td>( V_{DD} = 1.8\text{V} \text{ to } 2.7\text{V} )</td>
</tr>
<tr>
<td>70</td>
<td>CS Active (( V_{IL} ) or ( V_{IH} )) to SCK(^\uparrow) Input</td>
<td>( T_{csA2sCH} )</td>
<td>15</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>71</td>
<td>SCK Input High Time</td>
<td>( T_{scH} )</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td>( V_{DD} = 2.7\text{V} \text{ to } 5.5\text{V} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>—</td>
<td>ns</td>
<td>( V_{DD} = 1.8\text{V} \text{ to } 2.7\text{V} )</td>
</tr>
<tr>
<td>72</td>
<td>SCK Input Low Time</td>
<td>( T_{scL} )</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td>( V_{DD} = 2.7\text{V} \text{ to } 5.5\text{V} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>—</td>
<td>ns</td>
<td>( V_{DD} = 1.8\text{V} \text{ to } 2.7\text{V} )</td>
</tr>
<tr>
<td>73</td>
<td>SDI Input Valid to SCK(^\uparrow) Edge (Setup Time)</td>
<td>( T_{diV2sCH} )</td>
<td>5</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>74</td>
<td>SCK(^\downarrow) Edge to SDI Input Invalid (Hold Time)</td>
<td>( T_{sclH2diL} )</td>
<td>10</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>77</td>
<td>CS Inactive (( V_{IH} )) to SDO Output High-Impedance</td>
<td>( T_{csH2DOZ} )</td>
<td>—</td>
<td>20</td>
<td>ns</td>
<td><strong>Note 1</strong></td>
</tr>
<tr>
<td>80</td>
<td>SCK(^\downarrow) Edge to SDO Data Output Valid</td>
<td>( T_{sclL2DOV} )</td>
<td>—</td>
<td>20</td>
<td>ns</td>
<td>( V_{DD} = 2.7\text{V} \text{ to } 5.5\text{V} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>35</td>
<td>ns</td>
<td>( V_{DD} = 1.8\text{V} \text{ to } 2.7\text{V} )</td>
</tr>
<tr>
<td>82</td>
<td>CS Active (( V_{IL} )) to SDO Data Output Valid</td>
<td>( T_{csL2DOV} )</td>
<td>—</td>
<td>20</td>
<td>ns</td>
<td>( 2.7\text{V} \text{ to } 5.5\text{V} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>35</td>
<td>ns</td>
<td>( 1.8\text{V} \text{ to } 2.7\text{V} )</td>
</tr>
<tr>
<td>83</td>
<td>SCK(^\downarrow) Edge to CS Inactive (( V_{IH} )) (Hold Time)</td>
<td>( T_{sclH2csI} )</td>
<td>15</td>
<td>—</td>
<td>ns</td>
<td>( V_{DD} = 2.7\text{V} \text{ to } 5.5\text{V} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>—</td>
<td>ns</td>
<td>( V_{DD} = 1.8\text{V} \text{ to } 2.7\text{V} )</td>
</tr>
<tr>
<td>84</td>
<td>CS Input High Time</td>
<td>( T_{csA2csI} )</td>
<td>30</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>89</td>
<td>Delay from HVC ( V_{IH} ) to First Command Byte(1)</td>
<td></td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note 1:** This specification is ensured by design.

**Note 2:** This parameter is ensured by characterization.
## TEMPERATURE SPECIFICATIONS

**Electrical Specifications:** Unless otherwise indicated, $V_{DD} = +2.7V$ to $+5.5V$, $V_{SS} = GND$.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Sym.</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Specified Temperature Range</td>
<td>$T_A$</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$T_A$</td>
<td>-40</td>
<td>—</td>
<td>+125</td>
<td>°C</td>
<td><strong>Note 1</strong></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$T_A$</td>
<td>-65</td>
<td>—</td>
<td>+150</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

**Thermal Package Resistances**

<table>
<thead>
<tr>
<th>Thermal Resistance, 10L-MSOP</th>
<th>$\theta_{JA}$</th>
<th></th>
<th>206</th>
<th></th>
<th>°C/W</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance, 10L-DFN (3 x 3)</td>
<td>$\theta_{JA}$</td>
<td></td>
<td>91</td>
<td></td>
<td>°C/W</td>
<td></td>
</tr>
<tr>
<td>Thermal Resistance, 16L-QFN</td>
<td>$\theta_{JA}$</td>
<td></td>
<td>58</td>
<td></td>
<td>°C/W</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** The MCP48CXBXX devices operate over this extended temperature range, but with reduced performance. Operation in this range must not cause $T_J$ to exceed the Maximum Junction Temperature of $+150°C$. 
2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

2.1 Electrical Data

Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5.5V$.

**FIGURE 2-1:** Average Device Supply Current vs. $F_{SCK}$ Frequency, Voltage and Temperature - Active Interface, $VRxB:VRxA = '00'$ (VDD Mode).

**FIGURE 2-2:** Average Device Supply Current vs. $F_{SCK}$ Frequency, Voltage and Temperature - Active Interface, $VRxB:VRxA = '01'$ (Band Gap Mode).

**FIGURE 2-3:** Average Device Supply Current vs. $F_{SCK}$ Frequency, Voltage and Temperature - Active Interface, $VRxB:VRxA = '11'$ (VREF Buffered Mode).

**FIGURE 2-4:** Average Device Supply Current - Inactive Interface ($SCK = VH$ or $VL$) vs. Voltage and Temperature, $VRxB:VRxA = '00'$ (VDD Mode).

**FIGURE 2-5:** Average Device Supply Current - Inactive Interface ($SCK = VH$ or $VL$) vs. Voltage and Temperature, $VRxB:VRxA = '01'$ (Band Gap Mode).

**FIGURE 2-6:** Average Device Supply Current - Inactive Interface ($SCK = VH$ or $VL$) vs. Voltage and Temperature, $VRxB:VRxA = '11'$ (VREF Buffered Mode).
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5.5V$.

**FIGURE 2-7:** Average Device Supply Current vs. $F_{SCK}$ Frequency, Voltage and Temperature - Active Interface, $VRxB:VRxA = '10'$ ($V_{REF}$ Unbuffered Mode).

**FIGURE 2-8:** Average Device Supply Active Current ($I_{DAA}$) (at 5.5V and $F_{SCK} = 50$ MHz) vs. Temperature and DAC Reference Voltage Mode.

**FIGURE 2-9:** Average Device Supply Current - Inactive Interface ($SCK = V_{IH}$ or $V_{IL}$) vs. Voltage and Temperature, $VRxB:VRxA = '10'$ ($V_{REF}$ Unbuffered Mode).
2.2 Linearity Data

2.2.1 TOTAL UNADJUSTED ERROR (TUE) - MCP48CXB2X (12-BIT), V\textsubscript{REF} = V\textsubscript{DD}
(V\textsubscript{RXB}:V\textsubscript{RXA} = '00'), GAIN = 1X, CODE 64-4032

Note: Unless otherwise indicated: T\textsubscript{A} = +25\degree C, V\textsubscript{DD} = 5.5V

FIGURE 2-10: Total Unadjusted Error (V\textsubscript{OUT}) vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), V\textsubscript{DD} = 5.5V.

FIGURE 2-11: Total Unadjusted Error (V\textsubscript{OUT}) vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), V\textsubscript{DD} = 2.7V.

FIGURE 2-12: Total Unadjusted Error (V\textsubscript{OUT}) vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), V\textsubscript{DD} = 1.8V.

FIGURE 2-13: Total Unadjusted Error (V\textsubscript{OUT}) vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), V\textsubscript{DD} = 5.5V.

FIGURE 2-14: Total Unadjusted Error (V\textsubscript{OUT}) vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), V\textsubscript{DD} = 2.7V.

FIGURE 2-15: Total Unadjusted Error (V\textsubscript{OUT}) vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), V\textsubscript{DD} = 1.8V.
2.2.2 INTEGRAL NONLINEARITY (INL) - MCP48CXB2X (12-BIT), $V_{\text{REF}} = V_{\text{DD}}$ ($VRXB:VRXA = '00'$), $GAIN = 1X$, CODE 64-4032

**Note:** Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{\text{DD}} = 5.5\text{V}$.

**FIGURE 2-16:** INL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{\text{DD}} = 5.5\text{V}$.

**FIGURE 2-17:** INL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{\text{DD}} = 2.7\text{V}$.

**FIGURE 2-18:** INL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{\text{DD}} = 1.8\text{V}$.

**FIGURE 2-19:** INL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{\text{DD}} = 5.5\text{V}$.

**FIGURE 2-20:** INL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{\text{DD}} = 2.7\text{V}$.

**FIGURE 2-21:** INL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{\text{DD}} = 1.8\text{V}$.
2.2.3 DIFFERENTIAL NONLINEARITY (DNL) - MCP48CXB2X (12-BIT), $V_{REF} = V_{DD}$

(VRXB:VRXA = '00'), GAIN = 1X, CODE 64 - 4032

Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5.5V$.

**FIGURE 2-22:** DNL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{DD} = 5.5V$.

**FIGURE 2-23:** DNL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{DD} = 2.7V$.

**FIGURE 2-24:** DNL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{DD} = 1.8V$.

**FIGURE 2-25:** DNL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{DD} = 5.5V$.

**FIGURE 2-26:** DNL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{DD} = 2.7V$.

**FIGURE 2-27:** DNL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{DD} = 1.8V$. 
2.2.4 TOTAL UNADJUSTED ERROR (TUE) - MCP48CXB2X (12-BIT), EXTERNAL $V_{REF} = 0.5 \times V_{DD}$ ($VRXB:VRXA = '10')$, UNBUFFERED, CODE 64 - 4032

Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5.5V$.

**FIGURE 2-28:** Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{REF} = 0.5 \times V_{DD} = 2.75V$, Gain = 2X.

**FIGURE 2-29:** Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{REF} = 0.5 \times V_{DD} = 1.35V$, Gain = 2X.

**FIGURE 2-30:** Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{REF} = 0.5 \times V_{DD} = 2.75V$, Gain = 2X.

**FIGURE 2-31:** Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{REF} = 0.5 \times V_{DD} = 1.35V$, Gain = 2X.
2.2.5 INTEGRAL NONLINEARITY (INL) - MCP48CXB2X (12-BIT), EXTERNAL $V_{REF} = 0.5 \times V_{DD}$ ($VRXB:VRXA = '10'$), UNBUFFERED, CODE 64 - 4032

Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5.5V$.

**FIGURE 2-32:** INL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{REF} = 0.5 \times V_{DD} = 2.75V$, Gain = 2X.

**FIGURE 2-33:** INL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{REF} = 0.5 \times V_{DD} = 1.35V$, Gain = 2X.

**FIGURE 2-34:** INL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{REF} = 0.5 \times V_{DD} = 2.75V$, Gain = 2X.

**FIGURE 2-35:** INL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{REF} = 0.5 \times V_{DD} = 1.35V$, Gain = 2X.
Differential Nonlinearity Error (DNL) - MCP48CXB2X (12-BIT), EXTERNAL

VREF = 0.5VDD (VRXB:VRXA = 10), UNBUFFERED, CODE 64 - 4032

Note: Unless otherwise indicated, TA = +25°C, VDD = 5.5V.

FIGURE 2-36: DNL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), VDD = 5.5V, VREF = 0.5 x VDD = 2.75V.

FIGURE 2-37: DNL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), VDD = 5.5V, VREF = 0.5 x VDD = 1.35V.

FIGURE 2-38: DNL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), VDD = 5.5V, VREF = 0.5 x VDD = 2.75V.

FIGURE 2-39: DNL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), VDD = 5.5V, VREF = 0.5 x VDD = 1.35V.
2.2.7 TOTAL UNADJUSTED ERROR (TUE) - MCP48CXB2X (12-BIT), \( V_{REF} = \) INTERNAL BAND GAP (VRXB:VRXA = ‘01’), CODE 64 - 4032

Note: Unless otherwise indicated, \( T_A = +25^\circ C \), \( V_{DD} = 5.5V \).

FIGURE 2-40: Total Unadjusted Error (\( V_{OUT} \)) vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), \( V_{DD} = 5.5V \), Gain = 1X.

FIGURE 2-43: Total Unadjusted Error (\( V_{OUT} \)) vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), \( V_{DD} = 5.5V \), Gain = 1X.

FIGURE 2-41: Total Unadjusted Error (\( V_{OUT} \)) vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), \( V_{DD} = 5.5V \), Gain = 2X.

FIGURE 2-44: Total Unadjusted Error (\( V_{OUT} \)) vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), \( V_{DD} = 5.5V \), Gain = 2X.

FIGURE 2-42: Total Unadjusted Error (\( V_{OUT} \)) vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), \( V_{DD} = 2.7V \), Gain = 1X.

FIGURE 2-45: Total Unadjusted Error (\( V_{OUT} \)) vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), \( V_{DD} = 2.7V \), Gain = 1X.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5.5V$.

FIGURE 2-46: Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{DD} = 2.7V$, Gain = 2X.

FIGURE 2-47: Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{DD} = 1.8V$, Gain = 1X.

FIGURE 2-48: Total Unadjusted Error ($V_{OUT}$) vs. DAC Code, $+25^\circ C$, Gain = 1X.

FIGURE 2-49: Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{DD} = 2.7V$, Gain = 2X.

FIGURE 2-50: Total Unadjusted Error ($V_{OUT}$) vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{DD} = 1.8V$, Gain = 1X.

FIGURE 2-51: Total Unadjusted Error ($V_{OUT}$) vs. DAC Code, $+25^\circ C$, Gain = 2X.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5.5V$.

**FIGURE 2-52:** Total Unadjusted Error ($V_{OUT}$) vs. DAC Code, +25°C, Gain = 1X and 2X.
2.2.8 INTEGRAL NONLINEARITY ERROR (INL) - MCP48CXB2X (12-BIT), $V_{\text{REF}} =$ INTERNAL BAND GAP ($V_{\text{RXB}}:V_{\text{RXA}} = '01'$), CODE 64-4032

**Note:** Unless otherwise indicated, $T_A = +25^\circ \text{C}$, $V_{\text{DD}} = 5.5\text{V}$.

**FIGURE 2-53:** INL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{\text{DD}} = 5.5\text{V}, \text{Gain} = 1\text{X}$.

**FIGURE 2-54:** INL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{\text{DD}} = 5.5\text{V}, \text{Gain} = 2\text{X}$.

**FIGURE 2-55:** INL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{\text{DD}} = 2.7\text{V}, \text{Gain} = 1\text{X}$.

**FIGURE 2-56:** INL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{\text{DD}} = 5.5\text{V}, \text{Gain} = 1\text{X}$.

**FIGURE 2-57:** INL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{\text{DD}} = 5.5\text{V}, \text{Gain} = 2\text{X}$.

**FIGURE 2-58:** INL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{\text{DD}} = 2.7\text{V}, \text{Gain} = 1\text{X}$.
Note: Unless otherwise indicated, $T_A = +25°C$, $V_{DD} = 5.5V$. 

**FIGURE 2-59:** INL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{DD} = 2.7V$, Gain = 2X.

**FIGURE 2-60:** INL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{DD} = 1.8V$, Gain = 1X.

**FIGURE 2-61:** INL Error vs. DAC Code, $+25°C$, Gain = 1X.

**FIGURE 2-62:** INL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{DD} = 2.7V$, Gain = 2X.

**FIGURE 2-63:** INL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{DD} = 1.8V$, Gain = 1X.

**FIGURE 2-64:** INL Error vs. DAC Code, $+25°C$, Gain = 2X.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5.5V$.

**FIGURE 2-65:** INL Error vs. DAC Code, $+25^\circ C$, Gain = 1X and 2X.
2.2.9 DIFFERENTIAL NONLINEARITY ERROR (DNL) - MCP48CXB2X (12-BIT), $V_{\text{REF}} = \text{INTERNAL BAND GAP} (V_{\text{RXB}}:V_{\text{RXA}} = \{'011')$, CODE 64-4032

Note: Unless otherwise indicated, $T_A = +25^\circ\text{C}$, $V_{\text{DD}} = 5.5\text{V}$.

FIGURE 2-66: DNL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{\text{DD}} = 5.5\text{V}$, Gain = 1X.

FIGURE 2-67: DNL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{\text{DD}} = 5.5\text{V}$, Gain = 2X.

FIGURE 2-68: DNL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{\text{DD}} = 2.7\text{V}$, Gain = 1X.

FIGURE 2-69: DNL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{\text{DD}} = 5.5\text{V}$, Gain = 1X.

FIGURE 2-70: DNL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{\text{DD}} = 5.5\text{V}$, Gain = 2X.

FIGURE 2-71: DNL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{\text{DD}} = 2.7\text{V}$, Gain = 1X.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5.5V$.

FIGURE 2-72: DNL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{DD} = 2.7V$, Gain = 2X.

FIGURE 2-73: DNL Error vs. DAC Code and Temperature (Single-Channel - MCP48CXB21), $V_{DD} = 1.8V$, Gain = 1X.

FIGURE 2-74: DNL Error vs. DAC Code, $+25^\circ C$, Gain = 1X.

FIGURE 2-75: DNL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{DD} = 2.7V$, Gain = 2X.

FIGURE 2-76: DNL Error vs. DAC Code and Temperature (Dual-Channel - MCP48CXB22), $V_{DD} = 1.8V$, Gain = 1X.

FIGURE 2-77: DNL Error vs. DAC Code, $+25^\circ C$, Gain = 2X.
Note: Unless otherwise indicated, $T_A = +25^\circ C$, $V_{DD} = 5.5V$.

**FIGURE 2-78:** DNL Error vs. DAC Code, $+25^\circ C$, Gain = 1X and 2X.
3.0 PIN DESCRIPTIONS

Overviews of the pin functions are provided from Section 3.1 to Section 3.10. The descriptions of the pins for the single-DAC output device are listed in Table 3-1, and descriptions for the dual-DAC output device are listed in Table 3-2.

### TABLE 3-1: MCP48CXBX1 (SINGLE-DAC) PIN FUNCTION TABLE

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>I/O</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V_DD</td>
<td>—</td>
<td>P</td>
<td>Supply Voltage</td>
</tr>
<tr>
<td>2</td>
<td>CS</td>
<td>I</td>
<td>ST</td>
<td>SPI Chip Select</td>
</tr>
<tr>
<td>3</td>
<td>V_REF</td>
<td>A</td>
<td>Analog</td>
<td>Voltage Reference Input/Output</td>
</tr>
<tr>
<td>4</td>
<td>V_OUT</td>
<td>A</td>
<td>Analog</td>
<td>Buffered Analog Voltage Output</td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td>—</td>
<td>—</td>
<td>Not Internally Connected</td>
</tr>
<tr>
<td>6</td>
<td>LAT/HVC</td>
<td>I</td>
<td>ST</td>
<td>DAC Wiper Register Latch/High-Voltage Command Pin</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The Latch Pin allows the value in the volatile DAC registers (wiper and configuration bits) to be transferred to the DAC output (V_OUT).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>High-Voltage commands allow the User MTP configuration bits to be written.</td>
</tr>
<tr>
<td>7</td>
<td>V_SS</td>
<td>—</td>
<td>P</td>
<td>Ground Reference for all circuitries on the device</td>
</tr>
<tr>
<td>8</td>
<td>SDO</td>
<td>O</td>
<td>ST</td>
<td>SPI Serial Data Output</td>
</tr>
<tr>
<td>9</td>
<td>SCK</td>
<td>I</td>
<td>ST</td>
<td>SPI Serial Clock</td>
</tr>
<tr>
<td>10</td>
<td>SDI</td>
<td>I</td>
<td>ST</td>
<td>SPI Serial Data Input</td>
</tr>
<tr>
<td>—</td>
<td>EP</td>
<td>—</td>
<td>P</td>
<td>Exposed Thermal Pad, must be connected to V_SS</td>
</tr>
</tbody>
</table>

**Note 1:** A = Analog, I = Input, ST = Schmitt Trigger, O = Output, I/O = Input/Output, P = Power
## TABLE 3-2: MCP48CXBX2 (DUAL-DAC) PIN FUNCTION TABLE

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>I/O</th>
<th>Buffer Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V_DD</td>
<td>—</td>
<td>P</td>
<td>Supply Voltage</td>
</tr>
<tr>
<td>2</td>
<td>CS</td>
<td>I</td>
<td>ST</td>
<td>SPI Chip Select</td>
</tr>
<tr>
<td>3</td>
<td>VREF</td>
<td>A</td>
<td>Analog</td>
<td>Voltage Reference Input/Output</td>
</tr>
<tr>
<td>—</td>
<td>VREF0</td>
<td>A</td>
<td>Analog</td>
<td>Voltage Reference Input/Output for DAC0</td>
</tr>
<tr>
<td>—</td>
<td>VREF1</td>
<td>A</td>
<td>Analog</td>
<td>Voltage Reference Input/Output for DAC1</td>
</tr>
<tr>
<td>4</td>
<td>VOUT0</td>
<td>A</td>
<td>Analog</td>
<td>Buffered Analog Voltage Output 0</td>
</tr>
<tr>
<td>5</td>
<td>VOUT1</td>
<td>A</td>
<td>Analog</td>
<td>Buffered Analog Voltage Output 1</td>
</tr>
<tr>
<td>—</td>
<td>6,7,14,15</td>
<td>NC</td>
<td>—</td>
<td>Not Internally Connected</td>
</tr>
<tr>
<td>6</td>
<td>LAT/HVC</td>
<td>I</td>
<td>ST</td>
<td>DAC Wiper Register Latch/High-Voltage Command Pin. The Latch Pin allows the value in the volatile DAC registers (wiper and configuration bits) to be transferred to the DAC output (VOUT). High-Voltage commands allow the User MTP configuration bits to be written.</td>
</tr>
<tr>
<td>—</td>
<td>LAT0/HVC</td>
<td>I</td>
<td>ST</td>
<td>DAC0 Wiper Register Latch/High-Voltage Command Pin. The Latch Pin allows the value in the volatile DAC0 registers (wiper and configuration bits) to be transferred to the DAC0 output (VOUT0). High-Voltage commands allow the User MTP configuration bits to be written.</td>
</tr>
<tr>
<td>—</td>
<td>LAT1</td>
<td>I</td>
<td>ST</td>
<td>DAC1 Wiper Register Latch. The Latch Pin allows the value in the volatile DAC1 registers (wiper and configuration bits) to be transferred to the DAC1 output (VOUT1).</td>
</tr>
<tr>
<td>7</td>
<td>V_SS</td>
<td>—</td>
<td>P</td>
<td>Ground Reference for all circuitries on the device</td>
</tr>
<tr>
<td>8</td>
<td>SDO</td>
<td>O</td>
<td>ST</td>
<td>SPI Serial Data Output</td>
</tr>
<tr>
<td>9</td>
<td>SCK</td>
<td>I</td>
<td>ST</td>
<td>SPI Serial Clock</td>
</tr>
<tr>
<td>10</td>
<td>SDI</td>
<td>I</td>
<td>ST</td>
<td>SPI Serial Data Input</td>
</tr>
<tr>
<td>—</td>
<td>EP</td>
<td>—</td>
<td>P</td>
<td>Exposed Thermal Pad, must be connected to V_SS</td>
</tr>
</tbody>
</table>

**Note 1:** A = Analog, I = Input, ST = Schmitt Trigger, O = Output, I/O = Input/Output, P = Power
3.1 Positive Power Supply Input (VDD)

VDD is the positive supply voltage input pin. The input supply voltage is relative to VSS.

The power supply at the VDD pin should be as clean as possible for good DAC performance. It is recommended to use an appropriate bypass capacitor of about 0.1 µF (ceramic) to ground as close as possible to the pin. An additional 10 µF capacitor (tantalum) in parallel is also recommended to further attenuate noise present in application boards.

3.2 Ground (VSS)

The VSS pin is the device ground reference.

The user must connect the VSS pin to a ground plane through a low-impedance connection. If an analog ground path is available in the application PCB (Printed Circuit Board), it is highly recommended that the VSS pin be tied to the analog ground path or isolated within an analog ground plane of the circuit board.

3.3 Voltage Reference Pin (VREF)

The VREF pin is either an input or an output. When the DAC’s voltage reference is configured as the VREF pin, the pin is an input. When the DAC’s voltage reference is configured as the internal band gap, the pin is an output.

When the DAC’s voltage reference is configured as the VREF pin, there are two options for this voltage input: VREF pin voltage is buffered or unbuffered. The buffered option is offered in cases where the external reference voltage does not have sufficient current capability to not drop its voltage when connected to the internal resistor ladder circuit.

When the DAC’s voltage reference is configured as the device VDD, the VREF pin is disconnected from the internal circuit.

When the DAC’s voltage reference is configured as the internal band gap, the VREF pin’s drive capability is minimal, so the output signal should be buffered.

See Section 5.2 “Voltage Reference Selection” and Register 4-2 for more details on the configuration bits.

3.4 No Connect (NC)

The NC pin is not internally connected to the device.

3.5 Analog Output Voltage Pins (VOUT0, VOUT1)

VOUT0 and VOUT1 are the DAC analog voltage output pins. Each DAC output has an output amplifier. The DAC output range depends on the selection of the voltage reference source (and potential Output Gain selection). These are:

- Device VDD - The full-scale range of the DAC output is from VSS to approximately VDD.
- VREF pin - The full-scale range of the DAC output is from VSS to G x VRL, where G is the gain selection option (1X or 2X).
- Internal Band Gap - The full-scale range of the DAC output is from VSS to G x VBG, where G is the gain selection option (1X or 2X).

In Normal mode, the DC impedance of the output pin is about 1 Ω. In Power-Down mode, the output pin is internally connected to a known pull-down resistor of 1 kΩ, 100 kΩ, or open. The Power-Down selection bits settings are shown in Register 4-3 (Table 5-5).

3.6 Latch/High-Voltage Command Pin (LAT/HVC)

The DAC output value update event can be controlled and synchronized using the LAT pin, for one or both channels, on a single or different devices.

The LAT pin controls the effect of the volatile wiper registers, VRxB:VRxA, PDxB:PDxA and Gx bits on the DAC output.

If the LAT pin is held at VHH, the values sent to the volatile wiper registers and configuration bits have no effect on the DAC outputs.

Once voltage on the pin transitions to VIL, the values in the volatile wiper registers and configuration bits are transferred to the DAC outputs.

The pin is level-sensitive, so writing to the volatile wiper registers and configuration bits, while it is being held at VIL, will trigger an immediate change in the outputs.

For dual output devices in MSOP and DFN packages, the LAT pin controls both channels at the same time.

The HVC pin allows the device’s MTP memory to be programmed for the MCP48CMBXX devices. The programming voltage supply should provide 7.5V and at least 6.4 mA.

Note: The HVC pin should have voltages greater than 5.5V present only during the MTP programming operation. Using voltages greater than 5.5V for an extended time on the pin may cause device reliability issues.
3.7 SPI - Chip Select Pin (CS)

The CS pin enables/disables the serial interface (SDI, SDO, and SCK). The serial interface must be enabled for the device to receive any serial commands.

Refer to Section 6.4 “Interface Pins (CS, SCK, SDI, SDO, and LAT/HVC)” for more details regarding the SPI serial interface communication.

3.8 SPI - Serial Clock Pin (SCK)

The SCK pin is the serial clock pin of the SPI interface. The MCP48CXBXX SPI Interface only accepts external serial clocks.

3.9 SPI - Serial Data In Pin (SDI)

The SDI pin is the serial data input pin of the SPI interface. The SDI pin is used to write the DAC wiper registers and configuration bits.

3.10 SPI - Serial Data Out Pin (SDO)

The SDO pin is the serial data output pin of the SPI interface. The SDO pin is used to read the DAC wiper registers and configuration bits.
4.0 GENERAL DESCRIPTION

The MCP48CXBX1 devices are single-channel voltage output devices. The MCP48CXBX2 devices are dual-channel voltage output devices. These devices are offered with 8-bit (MCP48CXB0X), 10-bit (MCP48CXB1X) and 12-bit (MCP48CXB2X) resolutions.

The family offers two memory options: the MCP48CVBXX devices have a volatile memory, while the MCP48CMBXX have a 32-times programmable nonvolatile memory (MTP).

All devices include an SPI serial interface and a write latch (LAT) pin to control the update of the analog output voltage value from the value written in the volatile DAC output register.

The devices use a resistor ladder architecture. The resistor ladder DAC is driven from a software-selectable voltage reference source. The source can be either the device’s internal V DD, an external VREF pin voltage (buffered or unbuffered) or an internal band gap voltage source.

The DAC output is buffered with a low power and precision output amplifier. This output amplifier provides a rail-to-rail output with low offset voltage and low noise. The gain (1X or 2X) of the output buffer is software configurable.

The devices operate from a single supply voltage. This voltage is specified from 2.7V to 5.5V for full specified operation, and from 1.8V to 5.5V for digital operation.

The MCP48CMBXX devices also have user-programmable nonvolatile configuration memory (MTP). This allows the device’s desired POR values to be saved. The device also has general purpose MTP memory locations for storing system specific information (calibration data, serial numbers, system ID information). A high-voltage requirement for programming the nonvolatile locations on the HVC pin ensures that these device settings are not accidentally modified during normal system operation. Therefore, it is recommended that the MTP memory should be only programmed at the user’s factory.

The main functional blocks are:

- Power-on Reset/Brown-out Reset (POR/BOR)
- Device Memory
- Resistor Ladder
- Output Buffer/VOUT Operation
- SPI Serial Interface Module

4.1 Power-on Reset/Brown-out Reset (POR/BOR)

The internal Power-on Reset (POR)/Brown-out Reset (BOR) circuit monitors the power supply voltage (VDD) during operation. This circuit ensures correct device start-up at system power-up and power-down events.

The device’s RAM retention voltage (VRAM) is lower than the POR/BOR voltage trip point (VPOR/VBOR). The maximum VPOR/VBOR voltage is less than 1.8V.

The POR and BOR trip points are at the same voltage, and the condition is determined by whether the VDD voltage is rising or falling (see Figure 4-1). What occurs is different depending on whether the reset is a POR or BOR reset.

POR occurs as the voltage rises (typically from 0V), while BOR occurs as the voltage falls (typically from VDD(MIN) or higher).

When VPOR/VBOR < VDD < 2.7V, the electrical performance may not meet the data sheet specifications. In this region, the device is capable of reading and writing to its volatile memory if the proper serial command is executed.

4.1.1 POWER-ON RESET

The Power-on Reset is the case where the device’s VDD has power applied to it from the VSS voltage level. As the device powers-up, the VOUT pin floats to an unknown value. When the device’s VDD is above the transistor threshold voltage of the device, the output starts to be pulled low.

After the VDD is above the POR/BOR trip point (VBOR/VPOR), the resistor network’s wiper is loaded with the POR value. The POR value is either mid-scale (MCP48CVBXX) or the user’s MTP programmed value (MCP48CMBXX).

**Note:** In order to have the MCP48CMBXX devices load the values from nonvolatile memory locations at POR, they have to be programmed at least once by the user; otherwise, the loaded values will be the default ones. After MTP programming, a POR event is required to load the written values from the nonvolatile memory.

Volatile memory determines the analog output (VOUT) pin voltage. After the device is powered-up, the user can update the device memory.
When the rising \( V_{DD} \) voltage crosses the \( V_{POR} \) trip point, the following occurs:

- The default DAC POR value is latched into the volatile DAC register.
- The default DAC POR Configuration bit values are latched into the volatile configuration bits.
- POR Status bit is set (‘1’).
- The Reset Delay Timer \( t_{PORD} \) starts; when the reset delay timer \( t_{PORD} \) times out, the SPI serial interface is operational. During this delay time, the SPI interface will not accept commands.
- The Device Memory Address pointer is forced to 00h.

The analog output \( (V_{OUT}) \) state is determined by the state of the volatile configuration bits and the DAC register. This is called a Power-on Reset (event).

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

**FIGURE 4-1:** Power-on Reset Operation.
4.1.2 BROWN-OUT RESET

A Brown-out Reset occurs when a device had power applied to it and that power (voltage) drops below the specified range.

When the falling $V_{DD}$ voltage crosses the $V_{POR}$ trip point (BOR event), the following occurs:

- Serial Interface is disabled.
- MTP Writes are disabled.
- Device is forced into a Power-Down state ($PDxB:PDxA = '11$'). Analog circuitry is turned off.
- Volatile DAC register is forced to 000h.

Volatile configuration bits VRxB:VRxA and GX are forced to '0'.

If the $V_{DD}$ voltage decreases below the $V_{RAM}$ voltage, all volatile memory may become corrupted.

As the voltage recovers above the $V_{POR}/V_{BOR}$ voltage, see Section 4.1.1 “Power-on Reset” for further details.

Serial commands not completed due to a brown-out condition may cause the memory location to become corrupted.

Figure 4-1 illustrates the conditions for power-up and power-down events under typical conditions.

4.2 Device Memory

User memory includes the following types:

- **Volatile Register Memory (RAM)**
- **Nonvolatile Register Memory (MTP)**

MTP memory is present just for the MCP48CMBXX devices and has three groupings:

- NV DAC Output Values (loaded on POR event)
- Device Configuration Memory
- General Purpose NV Memory

Each memory location is up to 16 bits wide. The memory mapped register space is shown in Table 4-1. The SPI interface depends on how this memory is read and written. Refer to Section 6.0 “SPI Serial Interface Module” and Section 7.0 “Device Commands” for more details on reading and writing the device’s memory.

4.2.1 VOLATILE REGISTER MEMORY (RAM)

The MCP48CXBXX devices have volatile memory to directly control the operation of the DACs. There are up to five volatile memory locations:

- DAC0 and DAC1 Output Value registers
- $V_{REF}$ Select register
- Power-Down Configuration register
- Gain and Status register

The volatile memory starts functioning when the device $V_{DD}$ is at (or above) the RAM retention voltage ($V_{RAM}$). The volatile memory will be loaded with the default device values when the $V_{DD}$ rises across the $V_{POR}/V_{BOR}$ voltage trip point.

After the device is powered-up, the user can update the device memory. Table 4-2 shows the volatile memory locations and their interaction due to a POR event.

4.2.2 NONVOLATILE REGISTER MEMORY (MTP)

This memory option is available only for the MCP48CMBXX devices.

MTP memory starts functioning below the device’s $V_{POR}/V_{BOR}$ trip point and, once the $V_{POR}$ event occurs, the volatile memory registers are loaded with the corresponding MTP register memory values.

Memory addresses 0Ch through 1Fh are nonvolatile memory locations. These locations contain the DAC POR/BOR Wiper values, the DAC POR/BOR configuration bits and 8 general purpose memory locations for storing user-defined data as calibration constants or identification numbers.

The nonvolatile wiper registers and configuration bits determine the DAC Output and Configuration values at the POR event.

These nonvolatile values will overwrite the factory default values. If these MTP addresses are unprogrammed, the factory default values define the output state.

To program nonvolatile memory locations, a high-voltage source on the LAT/HVC pin is required. Each register/MTP location can be programmed 32 times. After 32 writes, a new write operation will not be possible and the last successful value written will remain associated with the memory location.

The device starts writing the MTP memory cells at the completion of the serial interface command. The high voltage should remain present on the LAT/HVC pin until the write cycle is complete; otherwise, the write is unsuccessful and the location is compromised (cannot be used again and the number of available writes decreases by one).

To recover from an aborted MTP write operation, the following procedure must be used:

- Write any valid value to the same address again
- Force a POR condition
- Write the desired value to the MTP location again
It is recommended to keep high voltage on only during the MTP Write command and programming cycle; otherwise, the reliability of the device could be affected.

4.2.3 UNIMPLEMENTED LOCATIONS

4.2.3.1 Unimplemented Register Bits

When issuing Read commands to a valid memory location with unimplemented bits, the unimplemented bits will be read as ‘0’.

4.2.4 UNIMPLEMENTED (RESERVED) LOCATIONS

There are a number of unimplemented memory locations that are reserved for future use. Normal (Voltage) commands (Read or Write) to any unimplemented memory address will result in a Command Error condition (SPI Command Error - CMDERR). High-Voltage commands to any unimplemented configuration bit(s) will also result in a Command Error condition.

4.2.5 POR/BOR OPERATION WITH WIPERLOCK TECHNOLOGY ENABLED

Regardless of the WiperLock Technology state, a POR event will load the Volatile DACx Wiper register value with the Nonvolatile DACx Wiper register value. Refer to Section 4.1 “Power-on Reset/Brown-out Reset (POR/BOR)” for further information.

### TABLE 4-1: MCP48CXBXX MEMORY MAP (16-BIT)

<table>
<thead>
<tr>
<th>Address</th>
<th>Function</th>
<th>Single</th>
<th>Dual</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>Volatile DAC Wiper Register 0</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>01h</td>
<td>Volatile DAC Wiper Register 1</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>02h</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>03h</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>04h</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>05h</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>06h</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>07h</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>08h</td>
<td>Volatile VREF Register</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>09h</td>
<td>Volatile Power-Down Register</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>0Ah</td>
<td>Volatile Gain and Status Register</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>0Bh</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>0Ch</td>
<td>General Purpose MTP</td>
<td>(1)</td>
<td></td>
</tr>
<tr>
<td>0Dh</td>
<td>General Purpose MTP</td>
<td>(1)</td>
<td></td>
</tr>
<tr>
<td>0Eh</td>
<td>General Purpose MTP</td>
<td>(1)</td>
<td></td>
</tr>
<tr>
<td>0Fh</td>
<td>General Purpose MTP</td>
<td>(1)</td>
<td></td>
</tr>
<tr>
<td>10h</td>
<td>Nonvolatile DAC Wiper Register 0</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>11h</td>
<td>Nonvolatile DAC Wiper Register 1</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>12h</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>13h</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>14h</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>15h</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>16h</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>17h</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>18h</td>
<td>Nonvolatile VREF Register</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>19h</td>
<td>Nonvolatile Power-Down Register</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>1Ah</td>
<td>NV Gain</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>1Bh</td>
<td>NV WiperLock™ Technology Register</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>1Ch</td>
<td>General Purpose MTP</td>
<td>(1)</td>
<td></td>
</tr>
<tr>
<td>1Dh</td>
<td>General Purpose MTP</td>
<td>(1)</td>
<td></td>
</tr>
<tr>
<td>1 Eh</td>
<td>General Purpose MTP</td>
<td>(1)</td>
<td></td>
</tr>
<tr>
<td>1Fh</td>
<td>General Purpose MTP</td>
<td>(1)</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- Volatile Memory addresses
- MTP Memory addresses
- Memory locations not implemented on this device family

**Note 1:** On nonvolatile memory devices only (MCP48CMBXX)
## TABLE 4-2: FACTORY DEFAULT POR/BOR VALUES (MTP MEMORY UNPROGRAMMED)

<table>
<thead>
<tr>
<th>Address</th>
<th>Function</th>
<th>POR/BOR Value</th>
<th>Address</th>
<th>Function</th>
<th>POR/BOR Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>Volatile DAC0 Register</td>
<td>7Fh 1FFh 7FFh</td>
<td>10h</td>
<td>Nonvolatile DAC0 Wiper Register (1)</td>
<td>7Fh 1FFh 7FFh</td>
</tr>
<tr>
<td>01h</td>
<td>Volatile DAC1 Register</td>
<td>7Fh 1FFh 7FFh</td>
<td>11h</td>
<td>Nonvolatile DAC1 Wiper Register (1)</td>
<td>7Fh 1FFh 7FFh</td>
</tr>
<tr>
<td>02h</td>
<td>Reserved</td>
<td>— — —</td>
<td>12h</td>
<td>Reserved</td>
<td>— — —</td>
</tr>
<tr>
<td>03h</td>
<td>Reserved</td>
<td>— — —</td>
<td>13h</td>
<td>Reserved</td>
<td>— — —</td>
</tr>
<tr>
<td>04h</td>
<td>Reserved</td>
<td>— — —</td>
<td>14h</td>
<td>Reserved</td>
<td>— — —</td>
</tr>
<tr>
<td>05h</td>
<td>Reserved</td>
<td>— — —</td>
<td>15h</td>
<td>Reserved</td>
<td>— — —</td>
</tr>
<tr>
<td>06h</td>
<td>Reserved</td>
<td>— — —</td>
<td>16h</td>
<td>Reserved</td>
<td>— — —</td>
</tr>
<tr>
<td>07h</td>
<td>Reserved</td>
<td>— — —</td>
<td>17h</td>
<td>Reserved</td>
<td>— — —</td>
</tr>
<tr>
<td>08h</td>
<td>Volatile VREF Register</td>
<td>0000h 0000h 0000h</td>
<td>18h</td>
<td>Nonvolatile VREF register (1)</td>
<td>0000h 0000h 0000h</td>
</tr>
<tr>
<td>09h</td>
<td>Volatile Power-Down Register</td>
<td>0000h 0000h 0000h</td>
<td>19h</td>
<td>Nonvolatile Power-Down Register (1)</td>
<td>0000h 0000h 0000h</td>
</tr>
<tr>
<td>0Ah</td>
<td>Volatile Gain and Status Register (2)</td>
<td>0080h 0080h 0080h</td>
<td>1Ah</td>
<td>NV Gain (1)</td>
<td>0000h 0000h 0000h</td>
</tr>
<tr>
<td>0Bh</td>
<td>Reserved</td>
<td>0000h 0000h 0000h</td>
<td>1Bh</td>
<td>NV WiperLock™ Technology Register (1)</td>
<td>0000h 0000h 0000h</td>
</tr>
<tr>
<td>0Ch</td>
<td>General Purpose MTP (1)</td>
<td>— — —</td>
<td>1Ch</td>
<td>General Purpose MTP (1)</td>
<td>0000h 0000h 0000h</td>
</tr>
<tr>
<td>0Dh</td>
<td>General Purpose MTP (1)</td>
<td>0000h 0000h 0000h</td>
<td>1Dh</td>
<td>General Purpose MTP (1)</td>
<td>0000h 0000h 0000h</td>
</tr>
<tr>
<td>0 Eh</td>
<td>General Purpose MTP (1)</td>
<td>0000h 0000h 0000h</td>
<td>1 Eh</td>
<td>General Purpose MTP (1)</td>
<td>0000h 0000h 0000h</td>
</tr>
<tr>
<td>0Fh</td>
<td>General Purpose MTP (1)</td>
<td>0000h 0000h 0000h</td>
<td>1Fh</td>
<td>General Purpose MTP (1)</td>
<td>0000h 0000h 0000h</td>
</tr>
</tbody>
</table>

**Legend:**
- **Volatile Memory address range**
- **Nonvolatile Memory address range**
- **Not implemented**

**Note 1:** On nonvolatile devices only (MCP48CMBXX).

**Note 2:** The “1” bit is the POR status bit, which is set after the POR event and cleared after address 0Ah is read.
### 4.2.6 DEVICE REGISTERS

Register 4-1 shows the format of the DAC Output Value registers for the volatile memory locations. These registers will be either 8 bits, 10 bits, or 12 bits wide. The values are right justified.

**REGISTER 4-1: DAC0 (00H/10H) AND DAC1 (01H/11H) OUTPUT VALUE REGISTERS (VOLATILE/NONVOLATILE)**

<table>
<thead>
<tr>
<th>Bit 15</th>
<th>Bit 14</th>
<th>Bit 13</th>
<th>Bit 12</th>
<th>Bit 11</th>
<th>Bit 10</th>
<th>Bit 9</th>
<th>Bit 8</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-n</td>
<td>R/W-n</td>
<td>R/W-n</td>
<td>R/W-n</td>
<td>R/W-n</td>
<td>R/W-n</td>
<td>R/W-n</td>
<td>R/W-n</td>
<td>R/W-n</td>
<td>R/W-n</td>
<td>R/W-n</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>12-bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>D11</td>
<td>D10</td>
<td>D09</td>
<td>D08</td>
<td>D07</td>
<td>D06</td>
<td>D05</td>
<td>D04</td>
<td>D03</td>
<td>D02</td>
<td>D01</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>10-bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>D09</td>
<td>D08</td>
<td>D07</td>
<td>D06</td>
<td>D05</td>
<td>D04</td>
<td>D03</td>
<td>D02</td>
<td>D01</td>
<td>D00</td>
<td>—</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>8-bit</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**Legend:**
- **12-bit**
- **10-bit**
- **8-bit**

**Unimplemented:** Read as ‘0’

<table>
<thead>
<tr>
<th>Bit 11-0</th>
<th>Bit 9-0</th>
<th>Bit 7-0</th>
<th><strong>D11-D00:</strong> DAC Output value - 12-bit devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>FFFh = Full-Scale output value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>7FFh = Mid-Scale output value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000h = Zero-Scale output value</td>
</tr>
</tbody>
</table>

| — | Bit 9-0 | — | **D09-D00:** DAC Output value - 10-bit devices |
| — | — | — | 3FFh = Full-Scale output value                  |
| — | — | — | 1FFh = Mid-Scale output value                   |
| — | — | — | 000h = Zero-Scale output value                  |

| — | — | — | **D07-D00:** DAC Output value - 8-bit devices |
| — | — | — | FFh = Full-Scale output value                    |
| — | — | — | 7Fh = Mid-Scale output value                     |
| — | — | — | 00h = Zero-Scale output value                    |

**Note 1:** Unimplemented bit, read as ‘0’.
Register 4-2 shows the format of the Voltage Reference Control register. Each DAC has two bits to control the source of the voltage reference of the DAC. This register is for the volatile memory locations. The width of this register is 2 times the number of DACs for the device.

### REGISTER 4-2: VOLTAGE REFERENCE (VREF) CONTROL REGISTERS (08h/18h) (VOLATILE/NONVOLATILE)

<table>
<thead>
<tr>
<th>Single</th>
<th>Dual</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 15-2</td>
<td>bit 15-4</td>
</tr>
<tr>
<td>VRxB-VRxA: DAC Voltage Reference Control bits</td>
<td></td>
</tr>
<tr>
<td>11 = VREF pin (Buffered); VREF buffer enabled</td>
<td></td>
</tr>
<tr>
<td>10 = VREF pin (Unbuffered); VREF buffer disabled</td>
<td></td>
</tr>
<tr>
<td>01 = Internal Band Gap (1.214V typical); VREF buffer enabled. VREF voltage driven when powered-down.</td>
<td></td>
</tr>
<tr>
<td>00 = VDD (Unbuffered); VREF buffer disabled. Use this state with power-down bits for lowest current.</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W =Writable bit
- U = Unimplemented bit, read as '0'
- -n = Value at POR
- '1' = Bit is set
- '0' = Bit is cleared
- x = Bit is unknown
- = Single-channel device
- = Dual-channel device

**Note 1:** Unimplemented bit, read as '0'.

**Note 2:** When the Internal Band Gap is selected, the band gap voltage source will continue to output the voltage on the VREF pin in any of the Power-Down modes. To reduce the power consumption to its lowest level (Band Gap disabled), after selecting the desired Power-Down mode, the voltage reference should be changed to VDD or VREF pin unbuffered ('00' or '10'), which turns off the Internal Band Gap circuitry. After wake-up, the user needs to reselect the Internal Band Gap ('01') for the voltage reference source.
Register 4-3 shows the format of the Power-Down Control register. Each DAC has two bits to control the Power-Down state of the DAC. This register is for the volatile memory locations and the nonvolatile memory locations. The width of this register is 2 times the number of DACs for the device.

**REGISTER 4-3: POWER-DOWN CONTROL REGISTERS (09h/19h)**

(VOLATILE/NONVOLATILE)

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-n</th>
<th>R/W-n</th>
<th>R/W-n</th>
<th>R/W-n</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- **‘1’** = Bit is set
- **‘0’** = Bit is cleared
- **x** = Bit is unknown

= Single-channel device

= Dual-channel device

**Single**

bit 15-2

bit 1-0

**Dual**

bit 15-4

bit 3-0

Unimplemented: Read as ‘0’

**PDxB-PDxA**: DAC Power-Down Control bits

11 = Powered-Down - $V_{OUT}$ is open circuit

10 = Powered-Down - $V_{OUT}$ is loaded with a 100 kΩ resistor to ground

01 = Powered-Down - $V_{OUT}$ is loaded with a 1 kΩ resistor to ground

00 = Normal Operation (Not powered-down)

**Note 1:** Unimplemented bit, read as ‘0’.

2: See Table 5-5 for more details.
**MCP48CXBXX**

Register 4-4 shows the format of the Gain Control and System Status register. Each DAC has one bit to control the gain of the DAC and two Status bits.

**REGISTER 4-4: GAIN CONTROL AND SYSTEM STATUS REGISTER (0Ah)**

<table>
<thead>
<tr>
<th>Single Channel</th>
<th>Dual Channel</th>
<th>Volatile</th>
</tr>
</thead>
<tbody>
<tr>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Legend:
- R = Readable bit
- W = Writable bit
- C = Clearable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

**Single**

- **bit 15**: Dual
  - **Unimplemented**: Read as ‘0’

- **bit 14 - 10**: Dual
  - **Unimplemented**: Read as ‘0’

- **bit 9**: Single
  - **G1**: DAC1 Output Driver Gain control bits
    - 1 = 2x Gain. Not applicable when VDD is used as VRL
    - 0 = 1x Gain

- **bit 8**: Single
  - **G0**: DAC0 Output Driver Gain control bits
    - 1 = 2x Gain. Not applicable when VDD is used as VRL
    - 0 = 1x Gain

- **bit 7**: Single
  - **POR**: Power-on Reset (Brown-out Reset) Status bit
    - This bit indicates if a POR or BOR event has occurred since the last Read command of this register. Reading this register clears the state of the POR Status bit.
    - 1 = A POR (BOR) event occurred since the last read of this register. Reading this register clears this bit.
    - 0 = A POR (BOR) event has not occurred since the last read of this register.

- **bit 6**: Single
  - **MTPMA**: MTP Memory Access Status bit
    - This bit indicates if the MTP Memory Access is occurring.
    - 1 = An MTP Memory Access is currently occurring (during the POR MTP read cycle or an MTP write cycle is occurring). Only serial commands addressing the volatile memory are allowed.
    - 0 = An MTP memory Access is NOT currently occurring

**Dual**

- **bit 15 - 10**: Dual
  - **Unimplemented**: Read as ‘0’

**Note 1:** Unimplemented bit, read as ‘0’.

**Note 2:** The DAC’s Gain bit is ignored, and the gain is forced to 1X (GX = “0”) when the DAC Voltage Reference is selected as VDD (VRxB:VRxA = “00”).

**Note 3:** For devices configured as volatile memory, this bit is read as ‘0’.
Register 4-5 shows the format of the Nonvolatile Gain Control register. Each DAC has one bit to control the gain of the DAC.

**Register 4-5: GAIN CONTROL REGISTER (1Ah) (NONVOLATILE)**

<table>
<thead>
<tr>
<th>Single</th>
<th>Dual</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 15</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 14</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 13</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 12</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 11</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 10</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 9</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 8</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 7</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 6</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 5</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 4</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 3</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 2</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 1</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>bit 0</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Legend:
- **R** = Readable bit
- **W** = Writable bit
- **C** = Clearable bit
- **U** = Unimplemented bit, read as ‘0’
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **-n** = Value at POR
- **x** = Bit is unknown

**Single**: Single-channel device  
**Dual**: Dual-channel device

- **Unimplemented**: Read as ‘0’

- **GX**\(^{(1)}\): DAC Output Driver Gain control bits
  - 1 = 2X Gain
  - 0 = 1X Gain

**Note 1**: When the DAC Voltage Reference is selected as \(V_{DD}\) (\(VRxB:VRxA = "00"\)), the DAC’s Gain bit is ignored and the gain is forced to 1X (\(GX = "0"\)).
Register 4-6 shows the format of the DAC WiperLock Technology Status Register. The width of this register is 2 times the number of DACs for the device.

WiperLock Technology bits only control access to volatile memory. Nonvolatile memory write access is controlled by the requirement of high voltage on the HVC pin, which is recommended to not be available during normal device operation.

### REGISTER 4-6: WIPERLOCK TECHNOLOGY CONTROL REGISTER (1BH) (NONVOLATILE)

<table>
<thead>
<tr>
<th>Single</th>
<th>Dual</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 15</td>
<td>bit 0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>U-0</th>
<th>R/W-n</th>
<th>R/W-n</th>
<th>R/W-n</th>
<th>R/W-n</th>
</tr>
</thead>
<tbody>
<tr>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td><a href="1"> </a></td>
<td><a href="1"> </a></td>
<td>WL0B</td>
<td>WL0A</td>
</tr>
<tr>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
<td>[ ]</td>
</tr>
</tbody>
</table>

**Legend:**
- **R** = Readable bit
- **W** = Writable bit
- **C** = Clearable bit
- **U** = Unimplemented bit, read as '0'
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown
- [ ] = Single-channel device
- [ ] = Dual-channel device

**Single**
- bit 15-2
- bit 1-0

**Dual**
- bit 15-4
- Unimplemented: Read as ‘0’
- bit 3-0

**WLXB-WLXA:** WiperLock™ Technology Status bits\(^{(2)}\)
- 11 = Vol. DAC Wiper Register and Vol. DAC configuration bits are locked
- 10 = Vol. DAC Wiper Register is locked, and Vol. DAC configuration bits are unlocked
- 01 = Vol. DAC Wiper Register is unlocked, and Vol. DAC configuration bits are locked
- 00 = Vol. DAC Wiper Register and Vol. DAC configuration bits are unlocked

**Note 1:** Unimplemented bit, read as ‘0’.

**Note 2:** The volatile PDxB:PDxAA bits are NOT locked due to the requirement of being able to exit Power-Down mode.
5.0 DAC CIRCUITRY

The Digital to Analog Converter circuitry converts a digital value into its analog representation. The description describes the functional operation of the device.

The DAC Circuit uses a resistor ladder implementation. Devices have up to two DACs. Figure 5-1 shows the functional block diagram for the MCP48CXBXX DAC circuitry.

The functional blocks of the DAC include:
- Resistor Ladder
- Voltage Reference Selection
- Output Buffer/VOUT Operation
- Latch Pin (LAT)
- Power-Down Operation

![Figure 5-1: MCP48CXBXX DAC Module Block Diagram.](image-url)

Where:
- \( V_W = \frac{\text{DAC Register Value}}{\# \text{Resistor in Resistor Ladder}} \times V_{RL} \)
- \( \# \text{Resistors in Resistor Ladder} = 256 \) (MCP48CXB0X)
- \( \# \text{Resistors in Resistor Ladder} = 1024 \) (MCP48CXB1X)
- \( \# \text{Resistors in Resistor Ladder} = 4096 \) (MCP48CXB2X)
5.1 Resistor Ladder

The resistor ladder is a digital potentiometer with the A Terminal connected to the selected reference voltage and the B Terminal internally grounded (see Figure 5-2). The volatile DAC register controls the wiper position. The wiper voltage \( V_W \) is proportional to the DAC register value divided by the number of resistor elements \( R_S \) in the ladder (256, 1024 or 4096) related to the \( V_{RL} \) voltage.

The output of the resistor network will drive the input of an output buffer.

The Resistor Network is made up of three parts:
- Resistor Ladder (string of \( R_S \) elements)
- Wiper switches
- DAC register decode

The resistor ladder has a typical impedance \( R_{RL} \) of approximately 71 kΩ. This resistor ladder resistance \( R_{RL} \) may vary from device to device up to ±10%. Since this is a voltage divider configuration, the actual \( R_{RL} \) resistance does not affect the output, given a fixed voltage at \( V_{RL} \).

Equation 5-1 shows the calculation for the step resistance.

Equation 5-1: \( R_S \) Calculation

\[
R_S = \frac{R_{RL}}{2^{n}}
\]

Note: The maximum wiper position is \( 2^n - 1 \), while the number of resistors in the resistor ladder is \( 2^n \). This means that when the DAC register is at full scale, there is one resistor element \( R_S \) between the wiper and the \( V_{RL} \) voltage.

If the unbuffered \( V_{REF} \) pin is used as the \( V_{RL} \) voltage source, the external voltage source should have a low output impedance.

When the DAC is powered down, the resistor ladder is disconnected from the selected reference voltage.

Note 1: The analog switch resistance \( R_W \) does not affect performance due to the voltage divider configuration.

FIGURE 5-2: Resistor Ladder Model Block Diagram.
5.2 Voltage Reference Selection

The resistor ladder has up to four sources for the reference voltage. The selection of the voltage reference source is specified with the volatile VREF1:VREF0 configuration bits (see Register 4-2). The selected voltage source is connected to the VRL node (see Figure 5-3 and Figure 5-4).

The four voltage source options for the Resistor Ladder are:

1. VDD pin voltage
2. Internal band gap voltage reference (VBG)
3. VREF pin voltage - unbuffered
4. VREF pin voltage - internally buffered

On a POR/BOR event, the default configuration state or the value written in the nonvolatile register is latched into the volatile VREF1:VREF0 configuration bits.

If the VREF pin is used with an external voltage source, then the user must select between Buffered or Unbuffered mode.

5.2.1 USING VDD AS VREF

When the user selects the VDD as reference, the VREF pin voltage is not connected to the Resistor Ladder. The VDD voltage is internally connected to the Resistor Ladder.

5.2.2 USING AN EXTERNAL VREF SOURCE IN UNBUFFERED MODE

In this case, the VREF pin voltage may vary from VSS to VDD. The voltage source should have a low-output impedance. If the voltage source has a high-output impedance, then the voltage on the VREF pin could be lower than expected. The resistor ladder has a typical impedance of 71 kΩ and a typical capacitance of 29 pF.

If a single VREF pin is supplying multiple DACs, the VREF pin source must have adequate current capability to support the number of DACs. It must be assumed that the resistor ladder resistance (RRL) of each DAC is at the minimum specified resistance and these resistances are in parallel.

If the VREF pin is tied to the VDD voltage, selecting the VDD Reference mode (VREF1:VREF0 = ‘00’) is recommended.

5.2.3 USING AN EXTERNAL VREF SOURCE IN BUFFERED MODE

The VREF pin voltage may be from 0V to VDD. The input buffer (amplifier) provides low offset voltage, low noise, and a very high input impedance, with only minor limitations on the input range and frequency response.

Any variation or noises on the reference source can directly affect the DAC output. The reference voltage needs to be as clean as possible for accurate DAC performance.

Note 1: The Band Gap voltage (VBG) is 1.214V typical. The band gap output goes through the buffer with a 2X gain to create the VRL voltage. See Table 5-1 for additional information on the band gap circuit.
5.2.4 USING THE INTERNAL BAND GAP AS VOLTAGE REFERENCE

The Internal Band Gap is designed to drive the Resistor Ladder Buffer.

If the Internal Band Gap is selected, then the band gap voltage source will drive the external VREF pins. The VREF1 pin must be left unloaded in this mode. The voltage reference source can be independently selected on devices with two DAC channels, but restrictions apply:

- The VDD mode can be used without issues on any channel.
- When the Internal Band Gap is selected as the voltage source, all the VREF pins are connected to its output. The use of the Unbuffered mode is only possible on VREF0, because it's the only one that can be loaded.
- When using the Internal Band Gap mode on channel 0, channel 1 must be put in Buffered External VREF mode or VDD Reference mode and the VREF1 pin must be left unloaded.

The resistance of the resistor ladder (RRL) is targeted to be 71 kΩ (±10%), which means a minimum resistance of 63.9 kΩ.

The band gap selection can be used across the VDD voltages while maximizing the VOUT voltage ranges. For VDD voltages below the Gain*VBG voltage, the output for the upper codes will be clipped to the VDD voltage. Table 5-4 shows the maximum DAC register code given device VDD and Gain bit setting.

<table>
<thead>
<tr>
<th>VDD</th>
<th>DAC Gain</th>
<th>Max DAC Code(1)</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>5.5</td>
<td>1</td>
<td>FFFh 3FFh FFFh</td>
<td>VOUT(max) = 1.214V</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>FFFh FFFh 3FFh</td>
<td>VOUT(max) = 2.428V</td>
</tr>
<tr>
<td>2.7</td>
<td>1</td>
<td>FFFh 3FFh FFFh</td>
<td>VOUT(max) = 1.214V</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>FFFh FFFh 3FFh</td>
<td>VOUT(max) = 2.428V</td>
</tr>
<tr>
<td>1.8</td>
<td>1</td>
<td>FFFh 3FFh FFFh</td>
<td>VOUT(max) = 1.214V</td>
</tr>
<tr>
<td></td>
<td>2(4)</td>
<td>BBCh 2EFh BBh</td>
<td>1.8V</td>
</tr>
</tbody>
</table>

Note 1: Without the VOUT pin voltage being clipped.
Note 2: Recommended to use the Gain = 1 setting.
Note 3: When VBG = 1.214V typical.

5.3 Output Buffer/VOUT Operation

The Output Driver buffers the wiper voltage (VW) of the Resistor Ladder.

The DAC output is buffered with a low-power, precision output amplifier with selectable gain. This amplifier provides a rail-to-rail output with low offset voltage and low noise. The amplifier’s output can drive the resistive and high-capacitive loads without oscillation. The amplifier provides a maximum load current which is enough for most programmable voltage reference applications. Refer to Section 1.0 “Electrical Characteristics” for the specifications of the output amplifier.

**Note:** The load resistance must be kept higher than 2 kΩ to maintain stability of the analog output and have it meet electrical specifications.

**Figure 5-5** shows a block diagram of the output driver circuit.

---

**FIGURE 5-5:** Output Driver Block Diagram.

Power-Down logic also controls the output buffer operation (see Section 5.5 “Power-Down Operation” for additional information on Power-Down). In any of the three Power-Down modes, the output amplifier is powered down and its output becomes a high impedance to the VOUT pin.

5.3.1 PROGRAMMABLE GAIN

The amplifier’s gain is controlled by the Gain (G) Configuration bit (see Register 4-4) and the VRL reference selection (see Register 4-2).

The Gain options are:

a) Gain of 1, with either the VDD or VREF pin used as reference voltage.

b) Gain of 2, only when the VREF pin or the Internal Band Gap is used as reference voltage. The VREF pin voltage should be limited to VDD/2. When the reference voltage selection (VRL) is the device’s VDD voltage, the G bit is ignored and a gain of 1 is used.

Table 5-2 shows the gain bit operation.
The volatile G bit value can be modified by:
- POR event
- BOR event
- SPI Write commands

### 5.3.2 OUTPUT VOLTAGE

The volatile DAC register values, along with the device’s configuration bits, control the analog V_{OUT} voltage. The volatile DAC register’s value is unsigned binary. The formula for the output voltage is provided in Equation 5-2. Examples of volatile DAC register values and the corresponding theoretical V_{OUT} voltage for the MCP48CXBXX devices are shown in Table 5-6.

**EQUATION 5-2: CALCULATING OUTPUT VOLTAGE (V_{OUT})**

\[
V_{OUT} = \frac{V_{RL} \times DAC \text{ Register Value}}{\# \text{ Resistor in Resistor Ladder}} \times Gain
\]

Where:
- \# Resistors in R-Ladder = 4096 (MCP48CXB2X)
- 1024 (MCP48CXB1X)
- 256 (MCP48CXB0X)

When Gain = 2 (V_{RL} = V_{REF}), if V_{REF} > V_{DD}/2, the V_{OUT} voltage is limited to V_{DD}. So if V_{REF} = V_{DD}, the V_{OUT} voltage does not change for volatile DAC register values mid-scale and greater, since the output amplifier is at full-scale output.

The following events update the DAC register value and therefore the analog voltage output (V_{OUT}):
- Power-on Reset
- Brown-out Reset
- SPI Write command (to volatile registers)

Next, the V_{OUT} voltage starts driving to the new value after the event has occurred.

### 5.3.3 OUTPUT SLEW RATE

Figure 5-6 shows an example of the slew rate of the V_{OUT} pin. The slew rate can be affected by the characteristics of the circuit connected to the V_{OUT} pin.

**FIGURE 5-6: V_{OUT} Pin Slew Rate.**

**5.3.3.1 Small Capacitive Load**

With a small capacitive load, the output buffer’s current is not affected by the capacitive load (C_L). But still, the V_{OUT} pin’s voltage is not a step transition from one output value (DAC register value) to the next output value. The change of the V_{OUT} voltage is limited by the output buffer’s characteristics, so the V_{OUT} pin voltage will have a slope from the old voltage to the new voltage. This slope is fixed for the output buffer, and is referred to as the buffer slew rate (SR_{BUF}).

**5.3.3.2 Large Capacitive Load**

With a larger capacitive load, the slew rate is determined by two factors:
- The output buffer’s short-circuit current (I_{SC})
- The V_{OUT} pin’s external load

I_{OUT} cannot exceed the output buffer’s short-circuit current (I_{SC}), which fixes the output buffer slew rate (SR_{BUF}). The voltage on the capacitive load (C_L), V_{CL} changes at a rate proportional to I_{OUT}, which fixes a capacitive load slew rate (SR_{CL}).

So the V_{CL} voltage slew rate is limited to the slower of the output buffer’s internally set slew rate (SR_{BUF}) and the capacitive load slew rate (SR_{CL}).

### 5.3.4 DRIVING RESISTIVE AND CAPACITIVE LOADS

The V_{OUT} pin can drive up to 100 pF of capacitive load in parallel with a 5 kΩ resistive load (to meet electrical specifications). V_{OUT} drops slowly as the load resistance decreases after about 3.5 kΩ. It is recommended to use a load with R_L greater than 2 kΩ.

Refer to the Characterization Data documents for a detailed V_{OUT} vs. Resistive Load characterization graph.
Driving large capacitive loads can cause stability problems for voltage feedback output amplifiers. As the load capacitance increases, the feedback loop’s phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response with overshoot and ringing in the step response. That is, since the V\text{OUT} pin’s voltage does not quickly follow the buffer’s input voltage (due to the large capacitive load), the output buffer will overshoot the desired target voltage. Once the driver detects this overshoot, it compensates by forcing it to a voltage below the target. This causes voltage ringing on the V\text{OUT} pin.

So, when driving large capacitive loads with the output buffer, a small series resistor (R\text{ISO}) at the output (see Figure 5-7) improves the output buffer’s stability (feedback loop’s phase margin) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitive load.

A method to evaluate the system’s performance is to inject a step voltage on the V\text{REF} pin and observe the V\text{OUT} pin’s characteristics.

**FIGURE 5-7:** Circuit to Stabilize Output Buffer for Large Capacitive Loads (C\text{L}).

The R\text{ISO} resistor value for your circuit needs to be selected. The resulting frequency response peaking and step response overshoot for this R\text{ISO} resistor value should be verified on the bench. Modify the R\text{ISO}'s resistance value until the output characteristics meet your requirements.

**TABLE 5-3:** THEORETICAL STEP VOLTAGE (V\text{S})\(^{(1)}\)

<table>
<thead>
<tr>
<th>Step Voltage</th>
<th>V\text{REF}</th>
<th>#bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\text{S}</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.0</td>
<td>1.22 mV</td>
<td>439 uV</td>
</tr>
<tr>
<td></td>
<td>4.88 mV</td>
<td>1.76 mV</td>
</tr>
<tr>
<td></td>
<td>19.5 mV</td>
<td>7.03 mV</td>
</tr>
</tbody>
</table>

Note 1: When Gain = 1X, V\text{FS} = V\text{RL}, and V\text{ZS} = 0V.

5.3.5 STEP VOLTAGE (V\text{S})

The Step Voltage depends on the device resolution and the calculated output voltage range. 1 LSb is defined as the ideal voltage difference between two successive codes. The step voltage can easily be calculated by using Equation 5-3 (the DAC register value is equal to 1). Theoretical Step Voltages are shown in Table 5-3 for several V\text{REF} voltages.

**EQUATION 5-3:** \(V\text{S} = \frac{V\text{RL}}{\# \text{Resistor in Resistor Ladder}} \times \text{Gain}\)

Where:

\# Resistor in R-Ladder = 4096 (12-bit)
1024 (10-bit)
256 (8-bit)
5.4 Latch Pin (\textit{LAT})

The Latch pin controls when the volatile DAC register value is transferred to the DAC wiper. This is useful for applications that need to synchronize the wiper(s) updates to an external event, such as zero crossing or updates to the other wipers on the device. The \textit{LAT} pin is asynchronous to the serial interface operation.

When the \textit{LAT} pin is high, transfers from the volatile DAC register to the DAC wiper are inhibited. The volatile DAC register value(s) can continue to be updated. When the \textit{LAT} pin is low, the volatile DAC register value is transferred to the DAC wiper.

\textbf{Note:} This allows both the volatile DAC0 and DAC1 registers to be updated while the \textit{LAT} pin is high, and to have outputs synchronously updated as the \textit{LAT} pin is driven low.

\textbf{FIGURE 5-8:} \textit{LAT} and DAC Interaction.

Since the DAC wiper \(x\) is updated from the volatile DAC register \(x\), all DACs that are associated with a given \textit{LAT} pin can be updated synchronously.

If the application does not require synchronization, then this signal should be tied low.

\textbf{FIGURE 5-9:} Example Use of \textit{LAT} Pin Operation.

5.5 Power-Down Operation

To allow the application to conserve power when DAC operation is not required, three Power-Down modes are available. On devices with multiple DACs, each DAC’s Power-Down mode is individually controllable.

All Power-Down modes do the following:
- Retain the value of the volatile DAC register and configuration bits

Depending on the selected Power-Down mode, the following will occur:
- \(V_{\text{OUT}}\) pin is switched to one of the two resistive pull-downs:
  - 100 k\(\Omega\) (typical)
  - 1 k\(\Omega\) (typical)
The Power-Down configuration bits (PD1:PD0) control the power-down operation (Table 5-4).

**TABLE 5-4: POWER-DOWN BITS AND OUTPUT RESISTIVE LOAD**

<table>
<thead>
<tr>
<th>PD1</th>
<th>PD0</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Normal operation</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1 kΩ resistor to ground</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>100 kΩ resistor to ground</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Open circuit</td>
</tr>
</tbody>
</table>

There is a delay (TPDD) between the PD1:PD0 bits changing from '00' to either '01', '10' or '11' and the op amp no longer driving the VOUT output, and the pull-down resistors sinking current.

In any of the Power-Down modes where the VOUT pin is not externally connected (sinking or sourcing current), as the number of DACs increases, the device’s power-down current will also increase.

Table 5-6 shows the current sources for the DAC based on the selected source of the DAC’s reference voltage and if the device is in normal operating mode or one of the Power-Down modes.

**TABLE 5-5: DAC CURRENT SOURCES**

<table>
<thead>
<tr>
<th>Device VDD Current Source</th>
<th>PDxB:xA = '00', VREFxB:xA =</th>
<th>PDxB:xA ≠ '00', VREFxB:xA =</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>00</td>
<td>01</td>
</tr>
<tr>
<td>Output Op Amp</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Resistive Ladder</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>VREF Selection Buffer</td>
<td>N</td>
<td>Y</td>
</tr>
<tr>
<td>Band Gap</td>
<td>N</td>
<td>Y</td>
</tr>
</tbody>
</table>

**Note 1:** The current is sourced from the VREF pin, not the device VDD.

**Note 2:** If DAC0 and DAC1 are in one of the Power-Down modes, MTP write operations are not recommended.

The power-down bits are modified by using a write command to the volatile Power-Down register or a POR event, which transfers the nonvolatile Power-Down Register to the volatile Power-Down Register.

Section 7.0 “Device Commands” describes the SPI command for writing the power-down bits.

---

**Note 1:** The SPI serial interface circuit is not affected by the Power-Down mode. This circuit remains active in order to receive any command that might come from the SPI Master device.

**5.5.1 EXITING POWER-DOWN**

The following event changes the PD1:PD0 bits to ‘00’ and therefore exits the Power-Down mode. This is any SPI Write command where the PD1:PD0 bits are ‘00’.

When the device exits Power-Down mode, the following occurs:

- Disabled internal circuits are turned on
- Resistor ladder is connected to the selected reference voltage (VRL)
- Selected pull-down resistor is disconnected
- The VOUT output is driven to the voltage represented by the volatile DAC register’s value and configuration bits

DAC Wiper register and DAC Wiper value may be different due to the DAC Wiper register being modified while the LAT pin was driven to (and remaining at) VIL.

The VOUT output signal requires time as these circuits are powered-up and the output voltage is driven to the specified value as determined by the volatile DAC register and configuration bits.

**Note:** Since the op amp and Resistor Ladder were powered off (0V), the op amp’s input voltage (VW) can be considered 0V. There is a delay (TPDE) between the PD1:PD0 bits updating to ‘00’ and the op amp driving the VOUT output. The op amp’s settling time (from 0V) needs to be taken into account to ensure the VOUT voltage reflects the selected value.
# TABLE 5-6: DAC INPUT CODE VS. CALCULATED ANALOG OUTPUT (V\text{OUT}) (V\text{DD} = 5.0V)

<table>
<thead>
<tr>
<th>Device</th>
<th>Volatile DAC Register Value</th>
<th>V\text{RL} (1)</th>
<th>LSb Gain Selection (2)</th>
<th>V\text{OUT} (3)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Equation</td>
<td>(\mu\text{V})</td>
<td>Equation</td>
</tr>
<tr>
<td><strong>MCP48CVBXX</strong> (12-bit)</td>
<td>1111 1111 1111 1111</td>
<td>5.0V</td>
<td>1,220.7 1x V\text{RL} * (4095/4096) * 1</td>
<td>4.998779</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V</td>
<td>610.4     1x V\text{RL} * (4095/4096) * 1</td>
<td>2.499390</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2x(4) V\text{RL} * (4095/4096) * 2</td>
<td>4.998779</td>
</tr>
<tr>
<td></td>
<td>0111 1111 1111 1111</td>
<td>5.0V</td>
<td>1,220.7 1x V\text{RL} * (2047/4096) * 1</td>
<td>2.498779</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V</td>
<td>610.4     1x V\text{RL} * (2047/4096) * 1</td>
<td>1.249390</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2x(4) V\text{RL} * (2047/4096) * 2</td>
<td>2.498779</td>
</tr>
<tr>
<td></td>
<td>0011 1111 1111 1111</td>
<td>5.0V</td>
<td>1,220.7 1x V\text{RL} * (1023/4096) * 1</td>
<td>1.248779</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V</td>
<td>610.4     1x V\text{RL} * (1023/4096) * 1</td>
<td>0.624390</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2x(4) V\text{RL} * (1023/4096) * 2</td>
<td>1.248779</td>
</tr>
<tr>
<td></td>
<td>0000 0000 0000 0000</td>
<td>5.0V</td>
<td>1,220.7 1x V\text{RL} * (0/4096) * 1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V</td>
<td>610.4     1x V\text{RL} * (0/4096) * 1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2x(4) V\text{RL} * (0/4096) * 2</td>
<td>0</td>
</tr>
<tr>
<td><strong>MCP48CVBXX</strong> (10-bit)</td>
<td>11 1111 1111 1111</td>
<td>5.0V</td>
<td>4,882.8 1x V\text{RL} * (1023/1024) * 1</td>
<td>4.995117</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V</td>
<td>2,441.4   1x V\text{RL} * (1023/1024) * 1</td>
<td>2.497559</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2x(4) V\text{RL} * (1023/1024) * 2</td>
<td>4.995117</td>
</tr>
<tr>
<td></td>
<td>01 1111 1111 1111</td>
<td>5.0V</td>
<td>4,882.8 1x V\text{RL} * (511/1024) * 1</td>
<td>2.495117</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V</td>
<td>2,441.4   1x V\text{RL} * (511/1024) * 1</td>
<td>1.247559</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2x(4) V\text{RL} * (511/1024) * 2</td>
<td>2.495117</td>
</tr>
<tr>
<td></td>
<td>00 1111 1111 1111</td>
<td>5.0V</td>
<td>4,882.8 1x V\text{RL} * (255/1024) * 1</td>
<td>1.245117</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V</td>
<td>2,441.4   1x V\text{RL} * (255/1024) * 1</td>
<td>0.622559</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2x(4) V\text{RL} * (255/1024) * 2</td>
<td>1.245117</td>
</tr>
<tr>
<td></td>
<td>00 0000 0000 0000</td>
<td>5.0V</td>
<td>4,882.8 1x V\text{RL} * (0/1024) * 1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V</td>
<td>2,441.4   1x V\text{RL} * (0/1024) * 1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2x(4) V\text{RL} * (0/1024) * 2</td>
<td>0</td>
</tr>
<tr>
<td><strong>MCP48CVBXX</strong> (8-bit)</td>
<td>1111 1111 1111</td>
<td>5.0V</td>
<td>19,531.3 1x V\text{RL} * (255/256) * 1</td>
<td>4.980469</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V</td>
<td>9,765.6   1x V\text{RL} * (255/256) * 1</td>
<td>2.490234</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2x(4) V\text{RL} * (255/256) * 2</td>
<td>4.980469</td>
</tr>
<tr>
<td></td>
<td>0111 1111 1111</td>
<td>5.0V</td>
<td>19,531.3 1x V\text{RL} * (127/256) * 1</td>
<td>2.480469</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V</td>
<td>9,765.6   1x V\text{RL} * (127/256) * 1</td>
<td>1.240234</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2x(4) V\text{RL} * (127/256) * 2</td>
<td>2.480469</td>
</tr>
<tr>
<td></td>
<td>0011 1111 1111</td>
<td>5.0V</td>
<td>19,531.3 1x V\text{RL} * (63/256) * 1</td>
<td>1.230469</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V</td>
<td>9,765.6   1x V\text{RL} * (63/256) * 1</td>
<td>0.615234</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2x(4) V\text{RL} * (63/256) * 2</td>
<td>1.230469</td>
</tr>
<tr>
<td></td>
<td>0000 0000 0000</td>
<td>5.0V</td>
<td>19,531.3 1x V\text{RL} * (0/256) * 1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5V</td>
<td>9,765.6   1x V\text{RL} * (0/256) * 1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2x(4) V\text{RL} * (0/256) * 2</td>
<td>0</td>
</tr>
</tbody>
</table>

**Note 1:** V\text{RL} is the resistor ladder’s reference voltage. It is independent of the V\text{REF1}:V\text{REF0} selection.

**Note 2:** Gain selection of 2X (GX = ‘1’) requires the voltage reference source to come from the V\text{REF} pin (V\text{REF1}:V\text{REF0} = ‘10’ or ‘11’) and requires V\text{REF} pin voltage (or V\text{RL}) \leq V\text{DD}/2 or from the internal band gap (V\text{REF1}:V\text{REF0} = ‘01’).

**Note 3:** These theoretical calculations do not take into account the Offset, Gain and Nonlinearity errors.
6.0 SPI SERIAL INTERFACE MODULE

The MCP48CXBXX’s SPI Serial Interface Module is a 4-wire interface. The devices operate only as slaves (do not generate the master clock). Figure 6-1 shows a typical SPI interface connection.

![Figure 6-1: Typical SPI Interface](image)

The frame content (commands) for the MCP48CXBXX are defined in Section 7.0 “Device Commands”.

6.1 Overview

This section discusses some of the specific characteristics of the MCP48CXBXX’s SPI Serial Interface Module. This is to assist in the development of your application.

The following sections discuss some of these device-specific characteristics:

- **Communication Data Rates**
- **POR/BOR**
- **Interface Pins (CS, SCK, SDI, SDO, and LAT/HVC)**
- **Device Memory Address**
- **SPI Modes**

The MCP48CXBXX devices support the SPI serial protocol. This SPI operates in Slave mode (does not generate the serial clock).

The SPI interface uses four pins. These are:

- **CS** - Chip Select
- **SCK** - Serial Clock
- **SDI** - Serial Data In
- **SDO** - Serial Data Out

A fifth pin is used if a write is being done in the MTP memory. This pin is HVC - High Voltage Command (customer manufacturing only, multiplexed with LAT0 functionality).

The HVC pin is high-voltage tolerant. To enter a high voltage command, the HVC pin must be greater than the VIH voltage.

Typical SPI Interfaces are shown in Figure 6-1. In the SPI interface, the Master’s Output pin is connected to the Slave’s Input pin, and the Master’s Input pin is connected to the Slave’s Output pin.

The MCP48CXBXX SPI module supports two (of the four) standard SPI modes. These are Mode 0, 0 and 1, 1. The SPI mode is determined by the state of the SCK pin (VIH or VIL) when the CS pin transitions from inactive (VIH) to active (VIL).

6.2 Communication Data Rates

The MCP48CXBXX supports clock rates (bit rates) of up to 25 MHz for read, and 50 MHz for Write commands.

For most applications, the write time will be considered more important, since that is how the device operation is controlled.

6.3 POR/BOR

On a POR/BOR event, the SPI Serial Interface Module state machine is reset, which includes forcing the device’s Memory Address pointer to 00h.

6.4 Interface Pins (CS, SCK, SDI, SDO, and LAT/HVC)

- **SERIAL DATA IN (SDI)**
  
  The Serial Data In (SDI) signal is the data signal in the device. The value on this pin is latched on the rising edge of the SCK signal.

- **SERIAL DATA OUT (SDO)**
  
  The Serial Data Out (SDO) signal is the data signal out of the device. The value on this pin is driven on the falling edge of the SCK signal.

6.4.3 SERIAL CLOCK (SCK)

- **SPI FREQUENCY OF OPERATION**

The SPI interface is specified to operate up to 50 MHz for Write commands and 25 MHz for read commands. The actual clock rate depends on the configuration of the system and the serial command used. Table 6-1 shows the SCK frequency for different configurations.
TABLE 6-1: SCK FREQUENCY

<table>
<thead>
<tr>
<th>Memory Type Access</th>
<th>Command</th>
<th>Read</th>
<th>Write</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nonvolatile Memory</td>
<td>SDI, SDO</td>
<td>25 MHz</td>
<td>50 MHz (^{(1)})</td>
</tr>
<tr>
<td>Volatile Memory</td>
<td>SDI, SDO</td>
<td>25 MHz</td>
<td>50 MHz (^{(1)})</td>
</tr>
</tbody>
</table>

Note 1: After issuing a Write command to the NV locations, the internal write cycle must be completed before the next SPI command addressing the NV locations is received \(t_{\text{wc}}\).

6.4.4 THE CS SIGNAL

The CS signal is used to select the device and frame a command sequence. To start a command, or sequence of commands, the CS signal must transition from the inactive state \(V_{IH}\) to an active state \(V_{IL}\).

After the CS signal has gone active, the SDO pin is driven and the clock bit counter is reset.

Note: There is a required delay after the CS pin goes active to the 1st edge of the SCK pin.

If an error condition occurs for an SPI command, then the Command byte’s Command Error (CMDERR) bit (on the SDO pin) will be driven low \(V_{IL}\). To exit the error condition, the user must take the CS pin to the \(V_{IH}\) level.

When the CS pin returns to the inactive state \(V_{IH}\), the SPI module resets (including the address pointer). While the CS pin is in the inactive state \(V_{IH}\), the serial interface is ignored. This allows the Host Controller to interface to other SPI devices using the same SDI, SDO, and SCK signals.

6.4.5 THE HVC SIGNAL

The high voltage requirement of the HVC pin for programming MTP registers ensure that a device in normal operation does not corrupt the values.

6.5 Device Memory Address

The memory address is the 5-bit value that specifies the location in the device’s memory that the specified command will operate on.

On a POR/BOR event, the device’s Memory Address pointer is forced to 00h.

6.6 SPI Modes

The SPI module supports two (of the four) standard SPI modes. These are Mode 0,0 and 1,1. The MCP48CXBXX’s SPI mode is automatically determined based on the Master’s configured mode.
6.6.1 OPERATION IN SPI MODE 0, 0

In SPI Mode 0, 0:
- SCK idle state = Low (V\textsubscript{IL})
- Data is clocked in on the SDI pin on the rising edge of SCK
- Data is clocked out on the SDO pin on the falling edge of SCK

6.6.2 OPERATION IN SPI MODE 1, 1

In SPI Mode 1, 1:
- SCK idle state = High (V\textsubscript{IH})
- Data is clocked in on the SDI pin on the rising edge of SCK
- Data is clocked out on the SDO pin on the falling edge of SCK

FIGURE 6-2: 24-Bit Commands (Write, Read) - SPI Waveform (Mode 0,0).

FIGURE 6-3: 24-Bit Commands (Write, Read) - SPI Waveform (Mode 1,1).
7.0 DEVICE COMMANDS

The MCP48CXBXX's SPI command format supports 32 memory address locations and two commands. The command may have two modes. These are:

- Normal Serial Commands
- MTP Programming (HV) Serial Commands

Normal serial commands are those where the HVC pin is driven to either \( V_{IH} \) or \( V_{IL} \). With High-Voltage Serial commands, the HVC pin is driven to 7.5V. These commands are shown in Table 7-1.

Table 7-2 shows an overview of all the SPI commands and their interaction with other device features.

The 24-bit commands (Read Command and Write Command) contain a Command Byte and a Data Word. The Command Byte contains one reserved bit, see Figure 7-1.

<table>
<thead>
<tr>
<th>Bit States C1:C0</th>
<th>Command</th>
<th># of Bits</th>
<th>Normal or HV</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>Read Data</td>
<td>24-Bits</td>
<td>Normal only(1)</td>
</tr>
<tr>
<td>00</td>
<td>Write Data</td>
<td>24-Bits</td>
<td>Both</td>
</tr>
<tr>
<td>01</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>10</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Note 1: Reading from the NV memory locations will return the shadow RAM value of the NV memory, not the NV memory contents. Once a write cycle starts, no other commands accessing NV memory locations are allowed.

![FIGURE 7-1: 24-bit SPI Command Format.](image)

### TABLE 7-1: COMMAND BITS OVERVIEW

<table>
<thead>
<tr>
<th>Bit States C1:C0</th>
<th>Command</th>
<th># of Bits</th>
<th>Normal or HV</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>Read Data</td>
<td>24-Bits</td>
<td>Normal only(1)</td>
</tr>
<tr>
<td>00</td>
<td>Write Data</td>
<td>24-Bits</td>
<td>Both</td>
</tr>
<tr>
<td>01</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>10</td>
<td>Reserved</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

Note 1: Reading from the NV memory locations will return the shadow RAM value of the NV memory, not the NV memory contents. Once a write cycle starts, no other commands accessing NV memory locations are allowed.

### TABLE 7-2: SPI COMMANDS - NUMBER OF CLOCKS

<table>
<thead>
<tr>
<th>Command</th>
<th>Operation</th>
<th>Code</th>
<th>Mode (1)</th>
<th># of Bit Clocks(2)</th>
<th>Data Update Rate (8-bit/10-bit/12-bit) (Data Words/Second)</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Write Command(4,5)</td>
<td>0 0</td>
<td>Y</td>
<td>Single</td>
<td>24</td>
<td>41,666</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 0</td>
<td>N</td>
<td>Continuous</td>
<td>24 * n</td>
<td>41,666</td>
</tr>
<tr>
<td></td>
<td>Read Command(6)</td>
<td>1 1</td>
<td>N</td>
<td>Random</td>
<td>24</td>
<td>41,666</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 1</td>
<td>N</td>
<td>Continuous</td>
<td>24 * n</td>
<td>41,666</td>
</tr>
</tbody>
</table>

Note 1: Nonvolatile registers can only use the Single mode.

2: "n" indicates the number of times the command operation is to be repeated.

3: The registers are updated after the 24th clock bit or after the \( \overline{CS} \) rising, depending on mode.

4: If the state of the HVC pin is \( V_{IH} \), then the command is ignored, but a Command Error condition (CMDERR) will NOT be generated.

5: This command is useful to determine when an MTP programming cycle has completed.

6: This command can be either normal voltage or high voltage.

7: The MTP write cycle starts after the \( \overline{CS} \) rising edge. A High-Voltage command requires the HVC pin to be at \( V_{IH} \) for the entire command, until the completion of the MTP write cycle.
7.1 Command Byte

The Command Byte has three fields, the Address (5 bits), the Command (2 bits), and 1 Reserved bit, see Figure 7-1.

The device memory is accessed when the master sends a proper Command Byte to select the desired operation. The memory location getting accessed is contained in the Command Byte’s AD4:AD0 bits. The action desired is contained in the Command Byte’s C1:C0 bits, see Figure 7-5. C1:C0 determines if the desired memory location will be read or written.

As the Command Byte is loaded into the device (on the SDI pin), the device’s SDO pin drives. The SDO pin will output high bits for the first seven bits of that command. On the 8th bit, the SDO pin will output the CMDERR bit state.

7.2 Data Bytes

The Read and Write commands use Data Bytes, see Figure 7-1. The D16 bit is currently unused, and corresponds to the position on the SDO data of the CMDERR bit.

7.3 Error Condition

The CMDERR bit indicates if the five address bits received (AD4:AD0) and the two command bits received (C1:C0) are a valid combination. The CMDERR bit is high if the combination is valid and low if the combination is invalid.

The command error bit will also be low if a write to a nonvolatile address has been specified and another SPI command occurs before the CS pin is driven inactive (V\text{IH}).

SPI commands that do not have a multiple of 24 clocks are ignored.

Once an error condition has occurred, any following commands are ignored. All following SDO bits will be low until the CMDERR condition is cleared by forcing the CS pin to the Inactive state (V\text{Ih}) or doing a POR.

7.3.1 ABORTING A TRANSMISSION

All SPI transmissions must have the correct number of SCK pulses to be executed. The command is not executed until the complete number of clocks have been received. Some commands also require the CS pin to be forced inactive (V\text{IH}). If the CS pin is forced to the Inactive state (V\text{IH}), the serial interface is reset. Partial commands are not executed.

Note 1: When the MCP48CXBXX does not receive data, it is recommended that the CS pin be forced to the inactive level (V\text{IL}).

7.4 Continuous Commands

The device supports the ability to execute commands continuously. While the CS pin is in Active state (V\text{IL}), any sequence of valid commands may be received.

The following example is a valid sequence of events:

1. CS pin driven active (V\text{IL})
2. Read command
3. Write command (Volatile memory)
4. Write command (Nonvolatile memory)
5. CS pin driven inactive (V\text{IH})

Note 1: While the CS pin is active, only one type of command should be issued. When changing commands, it is recommended to take the CS pin inactive then force it back to the active state.

Note 2: Long command strings should be broken down into shorter command strings. This reduces the probability of noise on the SCK pin corrupting the desired SPI command string.

7.5 Write Command

The Write command is a 24-bit command. The Write command can be issued to both the volatile and nonvolatile memory locations. The format of the command is shown in Figure 7-2.

A Write command to a volatile memory location changes that location after a properly formatted Write command (24-clock) has been received.

A Write command to a nonvolatile memory location will only start a write cycle after a properly formatted Write command (24-clock) has been received and the CS pin transitions to the Inactive state (V\text{IH}).

Note: Writes to volatile memory locations depend on the state of the WiperLock™ Technology bits.
7.5.1 SINGLE WRITE TO VOLATILE MEMORY

The write operation requires that the CS pin be in the Active state (V\text{IL}). Typically, the CS pin is in the Inactive state (V\text{IH}) and is driven to the Active state (V\text{IL}). The 24-bit Write command (Command Byte and Data Bytes) is then clocked in on the SCK and SDI pins. Once all 24 bits have been received, the specified volatile address is updated. A write will not occur if the Write command isn’t exactly 24 clocks pulses. This protects against system issues from corrupting the nonvolatile memory locations.

Figure 7-2 shows the waveform for a single write.

7.5.2 SINGLE WRITE TO NONVOLATILE MEMORY

The sequence to write to a single nonvolatile memory location is the same as a single write to volatile memory with the exception that before the command, the HVC pin must be driven to V\text{IH}. After the command, the CS pin is driven inactive (V\text{IH}), which then starts the MTP write cycle (t\text{wc}). The HVC pin must remain at the V\text{IH} level until the completion of the MTP write cycle.

A write cycle will not start if the write command isn’t exactly 24 clock’s pulses. This protects against system issues from corrupting the nonvolatile memory locations.

After the CS pin is driven inactive (V\text{IH}), the serial interface may immediately be re-enabled by driving the CS pin to the Active state (V\text{IL}).

During an MTP write cycle, only serial commands to volatile memory are accepted. All other serial commands are ignored until the MTP write cycle (t\text{wc}) is completed. The MTPMA bit in the Status register indicates the status of an MTP Write Cycle.

Once a Write command to a nonvolatile memory location has been received, NO other SPI commands should be received before the CS pin transitions to the Inactive state (V\text{IH}) or a Command Error (CMDERR) on the current SPI command occurs.

The write to a Nonvolatile Memory command has the same format as the write to a Volatile Memory command (see Figure 7-2).

<table>
<thead>
<tr>
<th>SDI</th>
<th>SDO</th>
<th>CMDERR</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD4</td>
<td>AD3</td>
<td>AD2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Note 1: For Write commands addressing the DAC Wiper Registers, the Data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00, and 8-bit = D07:D00. Data are right justified for easy Host Controller operation (no data manipulation before transmitting the desired value). The unimplemented bits are ignored.

2: After a valid memory address and a Write command byte are received (CMDERR = ‘1’), all the following SDO bits will be output as ‘1’.

3: If an Error Condition occurs (CMDERR = ‘0’), all the following SDO bits will be output as ‘0’ until the CMDERR condition is cleared (the CS pin is forced to the Inactive state).

FIGURE 7-2: Write Single Memory Location Command - SDI and SDO States.
7.5.3 CONTINUOUS WRITES TO VOLATILE MEMORY

Continuous writes are possible only when writing to the volatile memory registers. Figure 7-3 shows the sequence for three continuous writes. The writes do not need to be to the same volatile memory address.

7.5.4 CONTINUOUS WRITES TO NONVOLATILE MEMORY

Continuous writes to nonvolatile memory are not allowed, and attempts to do so will result in a command error (CMDERR) condition.

Note 1: For Write commands addressing the DAC Wiper Registers, the Data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00, and 8-bit = D07:D00. Data are right justified for easy Host Controller operation (no data manipulation before transmitting the desired value). The unimplemented bits are ignored.

2: After a valid memory address and a Write command byte are received (CMDERR = ‘1’), all the following SDO bits will be output as ‘1’.

3: If an Error Condition occurs (CMDERR = ‘0’), all the following SDO bits will be output as ‘0’ until the CMDERR condition is cleared (the CS pin is forced to the Inactive state).

4: This CMDERR bit will be forced to ‘0’, regardless if this Address + Command combination is valid. This command will not be completed and requires the CS pin to return to VIH to clear the CMDERR condition.

**FIGURE 7-3:** Continuous Write Sequence (Volatile Memory Only).
7.6 Read Command

The Read command is a 24-bit command. The Read command can be issued to both the volatile and nonvolatile memory locations. The format of the command is shown in Figure 7-4.

The first 7 bits of the Read command determine the address and the command. The 8th clock will output the CMDERR bit on the SDO pin. For the remaining 16 clocks, the device will transmit the data bits of the specified address (AD4:AD0).

Figure 7-4 shows the SDI and SDO information for a Read command.

During an MTP write cycle, the Read command can only be issued to the volatile memory locations. By reading the Status register, the Host Controller can determine when the write cycle has been completed (via the state of the MTPMA bit).

7.6.1 SINGLE READ

The read operation requires that the CS pin be in the Active state (VIL). Typically, the CS pin will be in the Inactive state (VIH) and is driven to the Active state (VIL). The 24-bit Read command (Command Byte and Data Word) is then clocked in on the SCK and SDI pins. The SDO pin starts driving high (VIH) when the CS goes active and starts driving data on the 8th bit (CMDERR bit); the addressed data comes out on the 9th through 24th clocks.

Note 1: The Data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00, and 8-bit = D07:D00.

The unimplemented bits are output as ‘0’ and data are right justified for easy Host Controller operation (no data manipulation after reading the register value).

2: If an Error Condition occurs (CMDERR = ‘0’), all the following SDO bits will be output as ‘0’ until the CMDERR condition is cleared (the CS pin is forced to the Inactive state).

FIGURE 7-4: Read Single Memory Location Command - SDI and SDO States.
7.6.2 CONTINUOUS READS

Continuous reads allows the device’s memory to be read quickly. Continuous reads are possible to all memory locations. Read commands may only access volatile memory locations during an MTP Write Cycle.

Figure 7-5 shows the sequence for three continuous reads. The reads do not need to be to the same memory address.

**FIGURE 7-5:** Continuous Read Sequence.

<table>
<thead>
<tr>
<th>SDI</th>
<th>SDO</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD4 AD3 AD2 AD1 AD0  C  C  X  X  X</td>
<td>D11 D10 D09 D08 D07 D06 D05 D04 D03 D02 D01 D00</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Note 1:** The Data bits depend on the resolution of the device: 12-bit = D11:D00, 10-bit = D09:D00, and 8-bit = D07:D00. The unimplemented bits are output as ‘0’ and data are right justified for easy Host Controller operation (no data manipulation after reading the register value).

2: If an Error Condition occurs (CMDERR = ‘0’), all the following SDO bits will be output as ‘0’ until the CMDERR condition is cleared (the CS pin is forced to the Inactive state).

3: This CMDERR bit will be forced to ‘0’, regardless if this Address + Command combination is valid. This command will not be completed and requires the CS pin to return to VIH to clear the CMDERR condition.
8.0 TYPICAL APPLICATIONS

The MCP48CXBXX devices are general purpose, single/dual-channel voltage output DACs for various applications where a precision operation with low power is needed.

Applications generally suited for the devices are:
- Set Point or Offset Trimming
- Sensor Calibration
- Portable Instrumentation (Battery-Powered)
- Motor Control

8.1 Design Considerations

In the design of a system with the MCP48CXBXX devices, the following considerations should be taken into account:

- Power Supply Considerations
- Layout Considerations

8.1.1 POWER SUPPLY CONSIDERATIONS

The power source supplying these devices must be as clean as possible. If the application circuit has separate digital and analog power supplies, VDD and VSS may reside on the analog plane.

The power supply to the device is also used for the DAC voltage reference internally if the internal VDD is selected as the resistor ladder’s reference voltage.

The typical application requires a bypass capacitor in order to filter high-frequency noise, which can be induced onto the power supply's traces. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity.

Any noise induced on the VDD line can affect the DAC performance. Typical applications require a bypass capacitor in order to filter out high-frequency noise on the VDD line. The noise can be induced onto the power supply’s traces or as a result of changes on the DAC output. The bypass capacitor helps to minimize the effect of these noise sources on signal integrity. Figure 8-1 shows an example of using two bypass capacitors (a 10 µF tantalum capacitor and a 0.1 µF ceramic capacitor) in parallel on the VDD line. These capacitors should be placed as close to the VDD pin as possible (within 4 mm). If the application circuit has separate digital and analog power supplies, the VDD and VSS pins of the device should reside on the analog plane.

![Example Circuit](image_url)

**FIGURE 8-1:** Example Circuit.
8.1.2 LAYOUT CONSIDERATIONS

Several layout considerations may be applicable to your application. These may include:

- **Noise**
- **PCB Area Requirements**

8.1.2.1 Noise

Inductively-coupled AC transients and digital switching noise can degrade the input and output signal integrity, potentially masking the MCP48CXBXX’s performance. Careful board layout minimizes these effects and increases the Signal-to-Noise Ratio (SNR). Multilayer boards utilizing a low-inductance ground plane, isolated inputs, isolated outputs and proper decoupling are critical to achieving the performance that the silicon is capable of providing. Particularly harsh environments may require shielding of critical signals. Separate digital and analog ground planes are recommended. In this case, the $V_{SS}$ pin and the ground pins of the $V_{DD}$ capacitors must be terminated to the analog ground plane.

**Note:** Breadboards and wire-wrapped boards are not recommended.

8.1.2.2 PCB Area Requirements

In some applications, PCB area is a criteria for device selection. Table 8-1 shows the typical package dimensions and area for the different package options.

<table>
<thead>
<tr>
<th>Pins</th>
<th>Package</th>
<th>Package Footprint</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Dimensions (mm)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Length</td>
</tr>
<tr>
<td>10</td>
<td>MSOP</td>
<td>UN</td>
</tr>
<tr>
<td>10</td>
<td>DFN</td>
<td>MF</td>
</tr>
<tr>
<td>16</td>
<td>QFN</td>
<td>MG</td>
</tr>
</tbody>
</table>

**Note 1:** Does not include recommended land pattern dimensions. Dimensions are typical values.
8.2 Application Examples

The MCP48CXBXX devices are rail-to-rail output DACs designed to operate with a $V_{DD}$ range of 2.7V to 5.5V. The internal output amplifier is robust enough to drive common, small-signal loads directly, thus eliminating the cost and size of the external buffers for most applications. The user can select the gain of 1 or 2 of the output op amp by setting the Configuration register bits. The internal $V_{DD}$ or an external reference can be used. Various user options and easy-to-use features that make the devices suitable for various modern DAC applications.

Application examples include:

- Decreasing Output Step Size
- Building a "Window" DAC
- Bipolar Operation
- Selectable Gain and Offset Bipolar Voltage Output
- Designing a Double-Precision DAC
- Building Programmable Current Source
- Serial Interface Communication Times
- Development Support
- Power Supply Considerations
- Layout Considerations

8.2.1 DC SET POINT OR CALIBRATION

A common application for the devices is a digitally-controlled set point and/or calibration of variable parameters, such as sensor offset or slope. For example, the MCP48CVB2X provides 4096 output steps. If voltage reference is 4.096V (where $G_X = '0'\), the LSB size is 1 mV. If a smaller output step size is desired, a lower external voltage reference is needed.

8.2.1.1 Decreasing Output Step Size

If the application calibrates the bias voltage of a diode or transistor, a bias voltage range of 0.8V may be desired with about 200 µV resolution per step. Two common methods to achieve small step size are to use a lower $V_{REF}$ pin voltage or a voltage divider on the DAC's output.

Using an external voltage reference ($V_{REF}$) is an option if the external reference is available with the desired output voltage range. However, when using a low-voltage reference voltage, occasionally the noise floor causes an SNR error that is intolerable. Using a voltage divider method is another option, and provides some advantages when the external voltage reference needs to be very low, or when the desired output voltage is not available. In this case, a larger value reference voltage is used, while two resistors scale the output range down to the precise desired level.

Figure 8-2 illustrates this concept. A bypass capacitor on the output of the voltage divider plays a critical function in attenuating the output noise of the DAC and the induced noise from the environment.

**FIGURE 8-2: Example Circuit Of Set Point or Threshold Calibration.**

**EQUATION 8-1: $V_{OUT}$ AND $V_{TRIP}$ CALCULATIONS**

$$V_{OUT} = V_{REF} \cdot G \cdot \frac{DAC \ Register \ Value}{2^N}$$

$$V_{trip} = \frac{V_{OUT} \left( \frac{R_2}{R_1 + R_2} \right)}{R_{SENSE}}$$
8.2.1.2 Building a “Window” DAC

When calibrating a set point or threshold of a sensor, typically only a small portion of the DAC output range is utilized. If the LSb size is adequate enough to meet the application’s accuracy needs, the unused range is sacrificed without consequences. If greater accuracy is needed, then the output range will need to be reduced to increase the resolution around the desired threshold.

If the threshold is not near VREF, 2 • VREF, or VSS, then creating a “window” around the threshold has several advantages. One simple method to create this “window” is to use a voltage divider network with a pull-up and pull-down resistor. Figure 8-3 and Figure 8-5 illustrate this concept.

**FIGURE 8-3:** Single-Supply “Window” DAC.

**EQUATION 8-2:** \[ V_{OUT} \text{ AND } V_{TRIP} \]

\[ V_{OUT} = V_{REF} \cdot G \cdot \frac{\text{DAC Register Value}}{2^N} \]

\[ V_{TRIP} = \frac{V_{OUT} \cdot R_{23} + V_{23} \cdot R_1}{R_1 + R_{23}} \]

Thevenin Equivalent

\[ R_{23} = \frac{R_2 \cdot R_1}{R_2 + R_1} \]

\[ V_{23} = \frac{(V_{CC} \cdot R_2) + (V_{CC} \cdot R_3)}{R_2 + R_3} \]

\[ V_{OUT} = V_{TRIP} \]

\[ V_{23} = V_{TRIP} \]

**FIGURE 8-4:** Digitally-Controlled Bipolar Voltage Source Example Circuit.

**EQUATION 8-3:** \[ V_{OUT}, V_{OA+}, \text{ AND } V_O \]

\[ V_{OUT} = V_{REF} \cdot G \cdot \frac{\text{DAC Register Value}}{2^N} \]

\[ V_{OA+} = \frac{V_{OUT} \cdot R_4}{R_3 + R_4} \]

\[ V_O = V_{OA+} \cdot (1 + \frac{R_2}{R_1}) \cdot V_{DD} \cdot (\frac{R_2}{R_1}) \]

8.3 Bipolar Operation

Bipolar operation is achievable by utilizing an external operational amplifier. This configuration is desirable due to the wide variety and availability of op amps. This allows a general purpose DAC, with its cost and availability advantages, to meet almost any desired output voltage range, power and noise performance.

Figure 8-4 illustrates a simple bipolar voltage source configuration. R1 and R2 allow the gain to be selected, while R3 and R4 shift the DAC’s output to a selected offset. Note that R4 can be tied to VDD instead of VSS if a higher offset is desired.
8.4 Selectable Gain and Offset Bipolar Voltage Output

In some applications, precision digital control of the output range is desirable. Figure 8-5 illustrates how to use the DAC devices to achieve this in a bipolar or single-supply application.

This circuit is typically used for linearizing a sensor whose slope and offset varies.

The equation to design a bipolar “window” DAC would be utilized if $R_3$, $R_4$, and $R_5$ are populated.

8.4.1 BIPOLAR DAC EXAMPLE

An output step size of 1 mV, with an output range of ±2.05V, is desired for a particular application.

Step 1: Calculate the range: $+2.05V - (-2.05V) = 4.1V$

Step 2: Calculate the resolution needed:

$$4.1V / 1mV = 4100$$

Since $2^{12} = 4096$, 12-bit resolution is desired.

Step 3: The amplifier gain $(R_2/R_1)$, multiplied by full-scale $V_{OUT}$ (4.096V), must be equal to the desired minimum output to achieve bipolar operation. Since any gain can be realized by choosing resistor values $(R_1 + R_2)$, the $V_{REF}$ value must be selected first. If a $V_{REF}$ of 4.096V is used, solve for the amplifier’s gain by setting the DAC to 0, knowing that the output needs to be -2.05V.

The equation can be simplified to:

**EQUATION 8-4:**

$$- \frac{R_2}{R_1} = \frac{-2.05}{4.096V} \quad \frac{R_2}{R_1} = \frac{1}{2}$$

If $R_1 = 20 \, k\Omega$ and $R_2 = 10 \, k\Omega$, the gain will be 0.5.

Step 4: Next, solve for $R_3$ and $R_4$ by setting the DAC to 4096, knowing that the output needs to be ±2.05V.

**EQUATION 8-5:**

$$\frac{R_2}{(R_3 + R_4)} = \frac{2.05V + (0.5 \cdot 4.096V)}{1.5 \cdot 4.096V} = \frac{2}{3}$$

If $R_4 = 20 \, k\Omega$, then $R_3 = 10 \, k\Omega$
8.5 Designing a Double-Precision DAC

Figure 8-6 shows an example design of a single-supply voltage output capable of up to 24-bit resolution. This requires two 12-bit DACs. This design is simply a voltage divider with a buffered output.

As an example, if a similar application to the one developed in Section 8.4.1 “Bipolar DAC Example” required a resolution of 1 µV instead of 1 mV, and a range of 0V to 4.1V, then a 12-bit resolution would not be adequate.

**Step 1:** Calculate the resolution needed:

\[
4.1V/1 \mu V = 4.1 \times 10^6
\]

Since \(2^{22} = 4.2 \times 10^6\), a 22-bit resolution is desired. Since DNL = ±1.0 LSb, this design can be attempted with the 12-bit DAC.

**Step 2:** Since DAC1’s \(V_{OUT}\) has a resolution of 1 mV, its output only needs to be “pulled” 1/1000 to meet the 1 µV target. Dividing \(V_{OUT}\) by 1000 would allow the application to compensate for DAC1’s DNL error.

**Step 3:** If \(R_2\) is 100Ω, then \(R_1\) needs to be 100 kΩ.

**Step 4:** The resulting transfer function is shown in Equation 8-8.

\[
V_{OUT} = \frac{V_{OUT0} \cdot R_2 + V_{OUT1} \cdot R_1}{R_1 + R_2}
\]

Where:

\[
V_{OUT0} = (V_{REF} \cdot G \cdot DAC0 \text{ register value})/4096
\]

\[
V_{OUT1} = (V_{REF} \cdot G \cdot DAC1 \text{ register value})/4096
\]

**GX** = Selected Op Amp Gain

8.6 Building Programmable Current Source

Figure 8-7 shows an example of building a programmable current source using a voltage follower. The current sensor resistor is used to convert the DAC voltage output into a digitally-selectable current source.

The smaller \(R_{SENSE}\) is, the less power is dissipated across it. However, this also reduces the resolution that the current can be controlled at.

![Digitally-Controlled Current Source](image)

**FIGURE 8-7:** Digitally-Controlled Current Source.

8.7 Serial Interface Communication Times

Table 7-2 shows the time/frequency of the supported operations of the SPI Serial Interface for the different serial interface operational frequencies. This, along with the \(V_{OUT}\) output performance (such as slew rate), would be used to determine your application’s volatile DAC register update rate.
9.0 DEVELOPMENT SUPPORT

Development support can be classified into two groups:

• Development Tools
• Technical Documentation

9.1 Development Tools

Several development tools are available to assist in the design and evaluation of the MCP48CXBXX devices. The currently available tools are shown in Table 9-1.

Figure 9-1 shows how the ADM00309 bond-out PCB can be populated to easily evaluate the MCP48CXBXX devices. Device evaluation can use the PICkit™ Serial Analyzer to control the DAC output registers and state of the Configuration, Control and Status register.

The ADM00309 boards may be purchased directly from the Microchip web site at www.microchip.com.

9.2 Technical Documentation

Several additional technical documents for design and development are available. These technical documents include Application Notes, Technical Briefs, and Design Guides. Table 9-2 lists some of these documents.

<table>
<thead>
<tr>
<th>BOARD NAME</th>
<th>PART #</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSOP-8 and MSOP-10 Evaluation Board</td>
<td>ADM00309</td>
<td>The MSOP-10 and MSOP-8 Evaluation Board is a bond-out board that allows the system designer to quickly evaluate the operation of Microchip Technology’s devices in any of the following packages: • MSOP (8/10-pin) • DIP (10-pin)</td>
</tr>
</tbody>
</table>

Note 1: Supports the PICkit™ Serial Analyzer. See the User’s Guide for additional information and requirements.

<table>
<thead>
<tr>
<th>APPLICATION NOTE NUMBER</th>
<th>TITLE</th>
<th>LITERATURE #</th>
</tr>
</thead>
<tbody>
<tr>
<td>AN1326</td>
<td>Using the MCP4728 12-Bit DAC for LDMOS Amplifier Bias Control Applications</td>
<td>DS01326</td>
</tr>
<tr>
<td>—</td>
<td>Signal Chain Design Guide</td>
<td>DS21825</td>
</tr>
<tr>
<td>—</td>
<td>Analog Solutions for Automotive Applications Design Guide</td>
<td>DS01005</td>
</tr>
</tbody>
</table>
FIGURE 9-1: MCP48CXBXX Evaluation Board Circuit Using ADM00309.
10.0 PACKAGING INFORMATION

10.1 Package Marking Information

10-Lead MSOP

Legend:

XX...X Customer-specific information
Y Year code (last digit of calendar year)
YY Year code (last 2 digits of calendar year)
WWW Week code (week of January 1 is week ‘01’)
NNN Alphanumeric traceability code
Pb-free JEDEC designator for Matte Tin (Sn)
*
This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Example

Part Number | Code
------------|------
MCP48CVB01-E/MF | BAKH
MCP48CVB11-E/MF | BAKL
MCP48CVB21-E/MF | BAKN
MCP48CVB02-E/MF | BAKJ
MCP48CVB12-E/MF | BAKM
MCP48CVB22-E/MF | BAKP
MCP48CMB01-E/MF | BAKB
MCP48CMB11-E/MF | BAKD
MCP48CMB21-E/MF | BAKF
MCP48CMB02-E/MF | BAKC
MCP48CMB12-E/MF | BAKE
MCP48CMB22-E/MF | BAKG

Example

48CV01
908256

BAKH
1908
256
### MCP48CXBXX

16-Lead 3 x 3 mm QFN

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP48CVB01-E/MG</td>
<td>ANN</td>
</tr>
<tr>
<td>MCP48CVB11-E/MG</td>
<td>APP</td>
</tr>
<tr>
<td>MCP48CVB21-E/MG</td>
<td>ARR</td>
</tr>
<tr>
<td>MCP48CVB02-E/MG</td>
<td>AAK</td>
</tr>
<tr>
<td>MCP48CVB12-E/MG</td>
<td>AAL</td>
</tr>
<tr>
<td>MCP48CVB22-E/MG</td>
<td>AAM</td>
</tr>
<tr>
<td>MCP48CMB01-E/MG</td>
<td>AKK</td>
</tr>
<tr>
<td>MCP48CMB11-E/MG</td>
<td>ALL</td>
</tr>
<tr>
<td>MCP48CMB21-E/MG</td>
<td>AMM</td>
</tr>
<tr>
<td>MCP48CMB02-E/MG</td>
<td>AAG</td>
</tr>
<tr>
<td>MCP48CMB12-E/MG</td>
<td>AAH</td>
</tr>
<tr>
<td>MCP48CMB22-E/MG</td>
<td>AAJ</td>
</tr>
</tbody>
</table>
10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

![Package Diagram](image)

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>( \varphi )</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
</tbody>
</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.
10-Lead Plastic Micro Small Outline Package (UN) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

**RECOMMENDED LAND PATTERN**

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td></td>
</tr>
<tr>
<td>MIN</td>
<td>NOM</td>
</tr>
<tr>
<td>Contact Pitch (E)</td>
<td>0.50 BSC</td>
</tr>
<tr>
<td>Contact Pad Spacing (C)</td>
<td>4.40</td>
</tr>
<tr>
<td>Overall Width (Z)</td>
<td>5.80</td>
</tr>
<tr>
<td>Contact Pad Width (X10) (X1)</td>
<td>0.30</td>
</tr>
<tr>
<td>Contact Pad Length (X10) (Y1)</td>
<td>1.40</td>
</tr>
<tr>
<td>Distance Between Pads (G1)</td>
<td>3.00</td>
</tr>
<tr>
<td>Distance Between Pads (GX)</td>
<td>0.20</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
2. BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2021A
10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
MCP48CXBXX

10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
<th>Dimension Limits</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Pins</td>
<td>N</td>
<td></td>
<td></td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
<td></td>
<td>0.50 BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
<td></td>
<td>0.80</td>
<td>0.90</td>
<td>1.00</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
<td></td>
<td>0.00</td>
<td>0.02</td>
<td>0.05</td>
</tr>
<tr>
<td>Contact Thickness</td>
<td>A3</td>
<td></td>
<td>0.20 REF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
<td></td>
<td>3.00 BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
<td></td>
<td>2.15</td>
<td>2.35</td>
<td>2.45</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
<td></td>
<td>3.00 BSC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
<td></td>
<td>1.40</td>
<td>1.50</td>
<td>1.75</td>
</tr>
<tr>
<td>Contact Width</td>
<td>b</td>
<td></td>
<td>0.18</td>
<td>0.25</td>
<td>0.30</td>
</tr>
<tr>
<td>Contact Length</td>
<td>L</td>
<td></td>
<td>0.30</td>
<td>0.40</td>
<td>0.50</td>
</tr>
<tr>
<td>Contact-to-Exposed Pad</td>
<td>K</td>
<td></td>
<td>0.20</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-063C Sheet 2 of 2
MCP48CXBXX

10-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Optional Center Pad Width</td>
<td>W2</td>
</tr>
<tr>
<td>Optional Center Pad Length</td>
<td>T2</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
</tr>
<tr>
<td>Contact Pad Width (X10)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X10)</td>
<td>Y1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2063B
16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
</tr>
<tr>
<td>Contact Thickness</td>
<td>A3</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>E2</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>D2</td>
</tr>
<tr>
<td>Contact Width</td>
<td>b</td>
</tr>
<tr>
<td>Contact Length</td>
<td>L</td>
</tr>
<tr>
<td>Contact-to-Exposed Pad</td>
<td>K</td>
</tr>
</tbody>
</table>

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
   - **BSC:** Basic Dimension. Theoretically exact value shown without tolerances.
   - **REF:** Reference Dimension, usually without tolerance, for information purposes only.
16-Lead Plastic Quad Flat, No Lead Package (MG) – 3x3x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

**Recommended Land Pattern**

---

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Optional Center Pad Width</td>
<td>W2</td>
</tr>
<tr>
<td>Optional Center Pad Length</td>
<td>T2</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C2</td>
</tr>
<tr>
<td>Contact Pad Width (X16)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X16)</td>
<td>Y1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
</tbody>
</table>

**Notes:**
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2142A
APPENDIX A: REVISION HISTORY

Revision A (February 2019)

• Original release of this document.
APPENDIX B: TERMINOLOGY

B.1 Resolution

The resolution is the number of DAC output states that divide the full-scale range. For the 12-bit DAC, the resolution is $2^{12}$, meaning the DAC code ranges from 0 to 4095.

Note: When there are $2^N$ resistors in the resistor ladder and $2^N$ tap points, the full-scale DAC register code is the resistor element (1 LSB) from the source reference voltage ($V_{DD}$ or $V_{REF}$).

B.2 Least Significant Bit (LSb)

This is the voltage difference between two successive codes. For a given output voltage range, it is divided by the resolution of the device. The range may be $V_{DD}$ or $V_{REF}$ to $V_{SS}$ (ideal), the DAC register codes across the linear range of the output driver (Measured 1), or full-scale to zero-scale (Measured 2).

EQUATION B-1: LSb VOLTAGE CALCULATION

Ideal:

$$V_{LSb(Ideal)} = \frac{V_{DD}}{2^N} \text{ or } \frac{V_{REF}}{2^N}$$

Measured 1 (12-bit device):

$$V_{LSb(Measured)} = \frac{V_{OUT(@4032)} - V_{OUT(@64)}}{(4032 - 64)}$$

Measured 2:

$$V_{LSb} = \frac{V_{OUT(@FS)} - V_{OUT(@ZS)}}{2^N - 1}$$

$2^N = 4096$ (MCP48CXB2X)

$= 1024$ (MCP48CXB1X)

$= 256$ (MCP48CXB0X)

B.3 Monotonic Operation

The monotonic operation means that the device’s output voltage ($V_{OUT}$) increases with every 1 code step (LSb) increment (from $V_{SS}$ to the DAC’s reference voltage ($V_{DD}$ or $V_{REF}$)).

FIGURE B-1: $V_{W} (V_{OUT})$.  

B.4 Full-Scale Error ($E_{FS}$)

The Full-Scale Error (see Figure B-3) is the error on the $V_{OUT}$ pin relative to the expected $V_{OUT}$ voltage (theoretical) for the maximum device DAC register code (code FFFh for 12-bit, code 3FFh for 10-bit, and code FFh for 8-bit) (see Equation B-2). The error is dependent on the resistive load on the $V_{OUT}$ pin (and where that load is tied to, such as $V_{SS}$ or $V_{DD}$). For loads (to $V_{SS}$) greater than specified, the full-scale error will be greater.

The error in bits is determined by the theoretical voltage step size to give an error in LSb.

EQUATION B-2: FULL-SCALE ERROR

$$E_{FS} = \frac{V_{OUT(@FS)} - V_{IDEAL(@FS)}}{V_{LSb(Ideal)}}$$

Where:

$E_{FS}$ is expressed in LSb

$V_{OUT(@FS)}$ is the $V_{OUT}$ voltage when the DAC register code is at full-scale.

$V_{IDEAL(@FS)}$ is the ideal output voltage when the DAC register code is at full-scale.

$V_{LSb(Ideal)}$ is the theoretical voltage step size.
B.5 Zero-Scale Error ($E_{ZS}$)

The Zero-Scale Error (see Figure B-2) is the difference between the ideal and measured $V_{OUT}$ voltage with the DAC register code equal to 000h (Equation B-3). The error is dependent on the resistive load on the $V_{OUT}$ pin and where that load is tied to, such as $V_{SS}$ or $V_{DD}$. For loads (to $V_{DD}$) greater than specified, the Zero-Scale Error is greater.

The error in bits is determined by the theoretical voltage step size to give an error in LSb.

**EQUATION B-3: ZERO SCALE ERROR**

$$E_{ZS} = \frac{V_{OUT(@ZS)}}{V_{LSb(Ideal)}}$$

Where:
- $E_{FS}$ is expressed in LSb.
- $V_{OUT(@ZS)}$ is the $V_{OUT}$ voltage when the DAC register code is at Zero-Scale.
- $V_{LSb(Ideal)}$ is the theoretical voltage step size.

B.6 Total Unadjusted Error ($E_T$)

The Total Unadjusted Error ($E_T$) is the difference between the ideal and measured $V_{OUT}$ voltage. Typically, calibration of the output voltage is implemented to improve the system’s performance.

The error in bits is determined by the theoretical voltage step size to give an error in LSb. **Equation B-4** shows the Total Unadjusted Error calculation.

**EQUATION B-4: TOTAL UNADJUSTED ERROR CALCULATION**

$$E_T = \frac{(V_{OUT\_Actual(@code)} - V_{OUT\_Ideal(@code)})}{V_{LSb(Ideal)}}$$

Where:
- $E_T$ is expressed in LSb.
- $V_{OUT\_Actual(@code)}$ = The measured DAC output voltage at the specified code
- $V_{OUT\_Ideal(@code)}$ = The calculated DAC output voltage at the specified code
- $V_{LSb(Ideal)}$ = $V_{REF}/#\text{Steps}$
  - 12-bit = $V_{REF}/4096$
  - 10-bit = $V_{REF}/1024$
  - 8-bit = $V_{REF}/256$

B.7 Offset Error ($E_{OS}$)

The Offset Error is the delta voltage of the $V_{OUT}$ voltage from the ideal output voltage at the specified code. This code is specified where the output amplifier is in the linear operating range; for the MCP48CXBXX we specify code 64 (decimal). Offset Error does not include gain error, which is illustrated in Figure B-2.

This error is expressed in mV. Offset Error can be negative or positive. The error can be calibrated by software in application circuits.

**FIGURE B-2: OFFSET ERROR (ZERO GAIN ERROR).**

B.8 Offset Error Drift ($E_{OSD}$)

The Offset Error Drift is the variation in Offset Error due to a change in ambient temperature. The Offset Error Drift is typically expressed in ppm/°C or µV/°C.

B.9 Gain Error ($E_{G}$)

Gain Error is a calculation based on the ideal slope using the voltage boundaries for the linear range of the output driver (e.g., code 64 and code 4032) (see Figure B-3). The Gain Error calculation nullifies the device’s Offset Error.

The Gain Error indicates how well the slope of the actual transfer function matches the slope of the ideal transfer function. The Gain Error is usually expressed as a percentage of full-scale range (% of FSR) or in LSb. FSR is the ideal full-scale voltage of the DAC (see Equation B-5).
B.10 Gain Error Drift (E_{GD})

The Gain Error Drift is the variation in Gain Error due to a change in ambient temperature. The Gain Error Drift is typically expressed in ppm/°C (of FSR).

B.11 Integral Nonlinearity (INL)

The Integral Nonlinearity (INL) Error is the maximum deviation of an actual transfer function from an ideal transfer function (straight line) passing through the defined end-points of the DAC transfer function (after Offset and Gain Errors have been removed).

For the MCP48CXBXX, INL is calculated using the defined end-points, DAC code 64 and code 4032. INL can be expressed as a percentage of FSR or in LSb. INL is also called relative accuracy. Equation B-6 shows how to calculate the INL error in LSb and Figure B-4 shows an example of INL accuracy.

Positive INL means a V_{OUT} voltage higher than the ideal one. Negative INL means a V_{OUT} voltage lower than the ideal one.

**EQUATION B-6: INL ERROR**

\[
E_{INL} = \left( \frac{V_{OUT} - V_{Calc\_Ideal}}{V_{LSb(Measured)}} \right) \times 100
\]

Where:

- INL is expressed in LSb.
- \( V_{Calc\_Ideal} = \text{Code} \times V_{LSb(Measured)} + V_{OS} \)
- \( V_{OUT}\text{\_{(Code = n)}} = \text{The measured DAC output voltage with a given DAC register code} \)
- \( V_{LSb(Measured)} = \text{For Measured:} \frac{(V_{OUT(4032)} - V_{OUT(64)})}{3968} \)
- \( V_{OS} = \text{Measured offset voltage} \)
B.12 Differential Nonlinearity (DNL)

The Differential Nonlinearity (DNL) Error (see Figure B-5) is the measure of step size between codes in actual transfer function. The ideal step size between codes is 1 LSb. A DNL Error of zero would imply that every code is exactly 1 LSb wide. If the DNL Error is less than 1 LSb, the DAC guarantees monotonic output and no missing codes. Equation B-7 shows how to calculate the DNL Error between any two adjacent codes in LSb.

EQUATION B-7: DNL ERROR

\[
E_{\text{DNL}} = \frac{V_{\text{OUT}(\text{code} = n+1)} - V_{\text{OUT}(\text{code} = n)}}{V_{\text{LSb(Measured)}}} - 1
\]

Where:

- DNL is expressed in LSb.
- \( V_{\text{OUT}(\text{Code} = n)} \) = The measured DAC output voltage with a given DAC register code
- \( V_{\text{LSb(Measured)}} \) = For Measured: \( \frac{(V_{\text{OUT}(4032)} - V_{\text{OUT}(64)})}{3968} \)

![DNL Accuracy Diagram](image)

**FIGURE B-5: DNL ACCURACY.**

B.13 Settling Time

The Settling time is the time delay required for the \( V_{\text{OUT}} \) voltage to settle into its new output value. This time is measured from the start of code transition to when the \( V_{\text{OUT}} \) voltage is within the specified accuracy.

For the MCP48CXBXX, the settling time is a measure of the time delay until the \( V_{\text{OUT}} \) voltage reaches within 0.5 LSb of its final value, when the volatile DAC register changes from 1/4 to 3/4 of the FSR (12-bit device: 400h to C00h).

B.14 Major-Code Transition Glitch

Major-Code transition glitch is the impulse energy injected into the DAC analog output when the code in the DAC register changes the state. It is normally specified as the area of the glitch in nV-Sec and is measured when the digital code is changed by 1 LSb at the major carry transition (Example: 011...111 to 100...000, or 100...000 to 011...111).

B.15 Digital Feed-Through

The digital feed-through is the glitch that appears at the analog output caused by coupling from the digital input pins of the device. The area of the glitch is expressed in nV-Sec and is measured with a full-scale change (Example: all 0s to all 1s and vice versa) on the digital input pins. The digital feed-through is measured when the DAC is not being written to the output register.

B.16 -3 dB Bandwidth

This is the frequency of the signal at the \( V_{\text{REF}} \) pin that causes the voltage at the \( V_{\text{OUT}} \) pin to fall to -3 dB from a static value on the \( V_{\text{REF}} \) pin. The output decreases due to the RC characteristics of the resistor ladder and the characteristics of the output buffer.

B.17 Power-Supply Sensitivity (PSS)

PSS indicates how the output of the DAC is affected by changes in the supply voltage. PSS is the ratio of the change in \( V_{\text{OUT}} \) to a change in \( V_{\text{DD}} \) for mid-scale output of the DAC. The \( V_{\text{OUT}} \) is measured while the \( V_{\text{DD}} \) is varied from 5.5V to 2.7V as a step (\( V_{\text{REF}} \) voltage held constant) and expressed in %/%, which is the % change of the DAC output voltage with respect to the % change of the \( V_{\text{DD}} \) voltage.

EQUATION B-8: PSS CALCULATION

\[
PSS = \frac{(V_{\text{OUT}(@5.5V)} - V_{\text{OUT}(@2.7V)})}{V_{\text{OUT}(@5.5V)}}
\]

Where:

- PSS is expressed in %/%.
- \( V_{\text{OUT}(@5.5V)} \) = The measured DAC output voltage with \( V_{\text{DD}} = 5.5V \)
- \( V_{\text{OUT}(@2.7V)} \) = The measured DAC output voltage with \( V_{\text{DD}} = 2.7V \)
B.18  Power-Supply Rejection Ratio (PSRR)

PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in $V_{OUT}$ to a change in $V_{DD}$ for full-scale output of the DAC. The $V_{OUT}$ is measured while the $V_{DD}$ is varied $\pm 10\%$ ($V_{REF}$ voltage held constant) and expressed in dB or $\mu$V/V.

B.19  $V_{OUT}$ Temperature Coefficient

The $V_{OUT}$ temperature coefficient quantifies the error in the resistor ladder’s resistance ratio (DAC register code value) and Output Buffer due to temperature drift.

B.20  Absolute Temperature Coefficient

The absolute temperature coefficient quantifies the error in the end-to-end output voltage (Nominal output voltage $V_{OUT}$) due to temperature drift. For a DAC, this error is typically not an issue due to the ratiometric aspect of the output.

B.21  Noise Spectral Density

The noise spectral density is a measurement of the device’s internally generated random noise, and is characterized as a spectral density (voltage per $\sqrt{\text{Hz}}$). It is measured by loading the DAC to the mid-scale value and measuring the noise at the $V_{OUT}$ pin. It is measured in nV/$\sqrt{\text{Hz}}$. 
**PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>Device</th>
<th>X (1)</th>
<th>Tape and Reel</th>
<th>X</th>
<th>Temperature Range</th>
<th>/XX</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MCP48CXBXX: 1 LSb INL Voltage Output Digital-to-Analog Converters, with SPI Interface, 8/10/12-bit Resolution, Single/Dual Outputs and Volatile/MTP Memory</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Tape and Reel:</td>
<td>T = Tape and Reel</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Range:</td>
<td>E = -40°C to +125°C (Extended)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package:</td>
<td>MF = Plastic Dual Flat, No Lead Package (DFN), 3 x 3 x 0.9 mm, 10-Lead</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>MG = Plastic Quad Flat, No Lead Package (QFN), 3 x 3 x 0.9 mm, 16-Lead</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>UN = Plastic Micro Small Outline Package (MSOP), 10-Lead</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Examples:**

- a) MCP48CVB01-E/MF: 1 LSb INL Voltage Output Digital-to-Analog Converter, 8-bit Resolution, Extended Temperature, 10LD DFN, with volatile memory.
- b) MCP48CVB01T-E/MF: 1 LSb INL Voltage Output Digital-to-Analog Converter, 8-bit Resolution, Tape and Reel, Extended Temperature, 10LD DFN, with volatile memory.
- a) MCP48CVB12-E/MG: 1 LSb INL Voltage Output Digital-to-Analog Converter, 10-bit Resolution, Extended Temperature, 16LD QFN, with volatile memory.
- b) MCP48CVB12T-E/MG: 1 LSb INL Voltage Output Digital-to-Analog Converter, 10-bit Resolution, Tape and Reel, Extended Temperature, 16LD QFN, with volatile memory.
- a) MCP48CMB21-E/UN: 1 LSb INL Voltage Output Digital-to-Analog Converter, 12-bit Resolution, Extended Temperature, 10LD MSOP, with nonvolatile memory.
- b) MCP48CMB21T-E/UN: 1 LSb INL Voltage Output Digital-to-Analog Converter, 12-bit Resolution, Tape and Reel, Extended Temperature, 10LD MSOP, with nonvolatile memory.

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Heldo, JuiceBlox, KeeLoq, Kleer, LANCheck, LINK MD, maXStylus, maTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntellIMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A. Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AynIn, AynOut, BodyCom, CodeGuard, CryptoAuthentication, CryptoAutomotive, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, INICnet, Inter-Chip Connectivity, JitterBlocker, KleerNet, KleerNet logo, memBrain, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, PowerSmart, PureSilicon, QMatrix, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2019, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-4219-6
Worldwide Sales and Service

AMERICAS
Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support: http://www.microchip.com/support
Web Address: www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453
Tel: 317-536-2380

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608
Tel: 951-273-7800

Raleigh, NC
Tel: 919-844-7510

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110
Tel: 408-436-4270

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC
Australia - Sydney
Tel: 61-2-9886-6733
China - Beijing
Tel: 86-10-8569-7000
China - Chengdu
Tel: 86-28-8665-5511
China - Chongqing
Tel: 86-23-8980-9588
China - Dongguan
Tel: 86-769-8702-9880
China - Guangzhou
Tel: 86-20-8755-8029
China - Hangzhou
Tel: 86-571-8792-8115
China - Hong Kong SAR
Tel: 852-2943-5100
China - Nanjing
Tel: 86-25-8473-2460
China - Qingdao
Tel: 86-532-8502-7355
China - Shanghai
Tel: 86-21-3326-8000
China - Shenyang
Tel: 86-24-2334-2829
China - Shenzhen
Tel: 86-755-8864-2200
China - Suzhou
Tel: 86-186-6233-1526
China - Wuhan
Tel: 86-27-5980-5300
China - Xian
Tel: 86-29-8833-7252
China - Xiamen
Tel: 86-592-2386138
China - Zuhai
Tel: 86-756-3210040

ASIA/PACIFIC
India - Bangalore
Tel: 91-80-3090-4444
India - New Delhi
Tel: 91-11-4160-8631
India - Pune
Tel: 91-20-4121-0141
Japan - Osaka
Tel: 81-6-6152-7160
Japan - Tokyo
Tel: 81-3-6880-3770
Korea - Daegu
Tel: 82-53-744-4301
Korea - Seoul
Tel: 82-2-554-7200
Malaysia - Kuala Lumpur
Tel: 60-3-7651-7906
Malaysia - Penang
Tel: 60-4-227-8870
Philippines - Manila
Tel: 63-2-634-99065
Singapore
Tel: 65-6334-8870
Taiwan - Hsin Chu
Tel: 886-3-577-8366
Taiwan - Kaohsiung
Tel: 886-7-213-7830
Taiwan - Taipei
Tel: 886-2-2508-8600
Thailand - Bangkok
Tel: 66-2-694-1351
Vietnam - Ho Chi Minh
Tel: 84-28-5448-2100

ASIA/PACIFIC

EUROPE
Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

Finland - Espoo
Tel: 358-9-4520-820

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Garching
Tel: 49-8931-9700

Germany - Haan
Tel: 49-2129-3766400

Germany - Heilbronn
Tel: 49-7131-67-3636

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Germany - Rosenheim
Tel: 49-8031-354-560

Israel - Ra'anan
Tel: 972-9-744-7705

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Padova
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Norway - Trondheim
Tel: 47-7288-4388

Poland - Warsaw
Tel: 48-22-3325737

Romania - Bucharest
Tel: 40-21-407-87-50

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Gothenburg
Tel: 46-31-704-60-40

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820