<table>
<thead>
<tr>
<th>REV</th>
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<tr>
<td>A</td>
<td>Release</td>
<td></td>
<td>6-12-08</td>
</tr>
<tr>
<td>B</td>
<td>Removed POR Reference and Updated VDD_CORE Bulk Cap Value</td>
<td></td>
<td>6-16-08</td>
</tr>
<tr>
<td>C</td>
<td>Added VDDVARIO Decoupling Capacitors</td>
<td></td>
<td>6-19-08</td>
</tr>
<tr>
<td>D</td>
<td>Changed EEDIO Feedback Resistor to 10K Ω</td>
<td></td>
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DOCUMENT DESCRIPTION

Schematic Checklist for the LAN9221I, 56-pin QFN Package

SMSC
80 Arkay Drive
Hauppauge, New York 11788

<table>
<thead>
<tr>
<th>Document Number</th>
<th>Revision</th>
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<td>SC471222</td>
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LAN9221I QFN Phy Interface:

1. **TPO+ (pin 45)**; This pin is the transmit twisted pair output positive connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

2. **TPO- (pin 44)**; This pin is the transmit twisted pair output negative connection from the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the transmit channel of the magnetics.

3. For Transmit Channel connection and termination details, refer to Figure 1.

4. **TPI+ (pin 48)**; This pin is the receive twisted pair input positive connection to the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the receive channel of the magnetics.

5. **TPI- (pin 47)**; This pin is the receive twisted pair input negative connection to the internal phy. It requires a 49.9Ω, 1.0% pull-up resistor to VDD33A (created from +3.3V). This pin also connects to the receive channel of the magnetics.

6. For Receive Channel connection and termination details, refer to Figure 2.
Figure 1 – Transmit Channel Connections and Terminations

Figure 2 - Receive Channel Connections and Terminations
LAN9221I QFN Magnetics:

1. The center tap connection on the LAN9221I side for the transmit channel must be connected to VDD33A (created from +3.3V) through a 10.0Ω series resistor. This resistor must have a tolerance of 1.0%. The transmit channel center tap of the magnetics also connects to the receive channel center tap of the magnetics.

2. The center tap connection on the LAN9221I side for the receive channel is connected to the transmit channel center tap on the magnetics. In addition, a 0.022 μF capacitor is required from the receive channel center tap of the magnetics to digital ground.

3. The center tap connection on the cable side (RJ45 side) for the transmit channel should be terminated with a 75Ω resistor through a 1000 pF, 2KV capacitor (Cmagterm) to chassis ground.

4. The center tap connection on the cable side (RJ45 side) for the receive channel should be terminated with a 75Ω resistor through a 1000 pF, 2KV capacitor (Cmagterm) to chassis ground.

5. Only one 1000 pF, 2KV capacitor (Cmagterm) to chassis ground is required. It is shared by both TX & RX center taps.

6. Assuming the design of an end-point device (NIC), pin 1 of the RJ45 is TX+ and should trace through the magnetics to TPO+ (pin 45) of the LAN9221I QFN.

7. Assuming the design of an end-point device (NIC), pin 2 of the RJ45 is TX- and should trace through the magnetics to TPO- (pin 44) of the LAN9221I QFN.

8. Assuming the design of an end-point device (NIC), pin 3 of the RJ45 is RX+ and should trace through the magnetics to TPI+ (pin 48) of the LAN9221I QFN.

9. Assuming the design of an end-point device (NIC), pin 6 of the RJ45 is RX- and should trace through the magnetics to TPI- (pin 47) of the LAN9221I QFN.

10. When using the SMSC LAN922x Family of parts in the HP Auto MDIX mode of operation, the use of an Auto MDIX style magnetics module is required. Please refer to the SMSC Applications Note 8.13 “Suggested Magnetics” for proper magnetics.

11. In order to guarantee IEEE compliance over the entire temperature range of operation, the magnetics used in conjunction with the LAN9221I must be rated for Industrial Temperature use.
**RJ45 Connector:**

1. Pins 4 & 5 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2KV capacitor ($C_{rjterm}$). There are two methods of accomplishing this:
   
a) Pins 4 & 5 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 pF, 2KV capacitor ($C_{rjterm}$).

   b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2KV capacitor ($C_{rjterm}$) to chassis ground, creates an equivalent circuit.

2. Pins 7 & 8 of the RJ45 connector connect to one pair of unused wires in CAT-5 type cables. These should be terminated to chassis ground through a 1000 pF, 2KV capacitor ($C_{rjterm}$). There are two methods of accomplishing this:
   
a) Pins 7 & 8 can be connected together with two 49.9Ω resistors. The common connection of these resistors should be connected through a third 49.9Ω to the 1000 pF, 2KV capacitor ($C_{rjterm}$).

   b) For a lower component count, the resistors can be combined. The two 49.9Ω resistors in parallel look like a 25Ω resistor. The 25Ω resistor in series with the 49.9Ω makes the whole circuit look like a 75Ω resistor. So, by shorting pins 4 & 5 together on the RJ45 and terminating them with a 75Ω resistor in series with the 1000 pF, 2KV capacitor ($C_{rjterm}$) to chassis ground, creates an equivalent circuit.

3. The RJ45 shield should be attached directly to chassis ground.
+3.3V Power Supply Connections:

1. The internal regulator supply (VDD33REG) input on the LAN9221I QFN is pin 1. This pin requires a connection to +3.3V.

2. The VDD33REG power pin should have one .01 μF (or smaller) capacitor to decouple the LAN9221I. The capacitor size should be SMD_0603 or smaller.

3. The analog supply (VDD33A) pins on the LAN9221I QFN are 46, 49 & 51. They require a connection to +3.3V through a ferrite bead. Be sure to place bulk capacitance on each side of the ferrite bead.

4. Each VDD33A pin should have one .01 μF (or smaller) capacitor to decouple the LAN9221I. The capacitor size should be SMD_0603 or smaller.

+1.8V to +3.3V Variable I/O Power Supply Connections:

1. The variable I/O supply (VDDVARIO) pins on the LAN9221I QFN are 18, 24, 30, & 56. They require an externally supplied voltage supply between +1.8V and +3.3V.

Caution: In the case of a +1.8V I/O application, the VDDVARIO pins cannot be supplied from the VDD18CORE regulator of the LAN9221I. The VDDVARIO pins must be supplied from an on-board, external +1.8V regulator.

2. Each VDDVARIO pin should have one .01 μF (or smaller) capacitor to decouple the LAN9221I. The capacitor size should be SMD_0603 or smaller.

VDD18CORE:

1. VDD18CORE (pins 2 & 37), these two pins are used to provide bypassing for the +1.8V core regulator. Each pin requires a 0.01 μF decoupling capacitor. Each capacitor should be located as close as possible to its pin without using vias. In addition, pin 2 requires a bulk capacitor placed as close as possible to pin 2. The bulk capacitor must have a value of at least 4.7 μF, and have an ESR (equivalent series resistance) of no more than 2.0 Ω. SMSC recommends a very low ESR ceramic capacitor for design stability. Other values, tolerances & characteristics are not recommended.

Caution: This +1.8V supply is for internal logic only. Do Not power other external circuits or devices with this supply.

VDD18A:

1. VDD18A (pin 53), this pin is used to provide an external +1.8V supply to the internal Phy PLL. A 0.01 μF decoupling capacitor must be attached to this pin. The capacitor should be located as close as possible to pin 53, and must be attached without using vias. This pin can be connected directly to pins 2 & 37 (VDD18CORE) of the LAN9221I to provide the +1.8V supply.

Caution: This +1.8V supply is for internal logic only. Do Not power other circuits or devices with this supply.
External Power Supply Ranging from +1.8V to +3.3V

Connect to RX & TX terminations

Connect 53 & 2 together on PCB with mini-plane

Two Caps on Pin 2

Connect 2 & 37 together on PCB with mini-plane

0.1 uF

4.7 uF Low ESR

Figure 3 - LAN9221I Power Connections
**Ground Connections:**

1. All grounds, the digital ground pins (GND), the core ground pins (GND_CORE) and the analog ground pins (VSS_A) on the LAN9221I QFN, are all connected internally to the exposed die paddle ground (VSS). The EDP Ground pad on the underside of the LAN9221I must be connected directly to a solid, contiguous digital ground plane.

2. On the PCB, we recommend one Digital Ground. We do not recommend running separate ground planes for any of our LAN products.

**Crystal Connections:**

1. A 25.000 MHz crystal must be used with the LAN9221I QFN. For exact specifications and tolerances refer to the latest revision LAN9221I data sheet.

2. XTAL1 (pin 55) on the LAN9221I QFN is the clock circuit input. This pin requires a $15 - 33 \ \mu F$ capacitor to digital ground. One side of the crystal connects to this pin.

3. XTAL2 (pin 54) on the LAN9221I QFN is the clock circuit output. This pin requires a matching $15 - 33 \ \mu F$ capacitor to ground and the other side of the crystal.

4. Since every system design is unique, the value for the capacitor is system dependant. The PCB design, the crystal selected, the layout and the type of caps selected all contribute to the characteristics of this circuit. Once the board is complete and operational, it is up to the system engineer to analyze this circuit in a lab environment. The system engineer should verify the frequency, the stability and the voltage level of the circuit to guarantee that the circuit meets all design criteria as put forth in the data sheet.

5. For proper operation, an additional $1.0M \ \Omega$ resistor needs to be added to the crystal circuit. This resistor needs to be placed in parallel with the crystal.

6. In order to guarantee IEEE compliancy over the entire temperature range of operation, the crystal used in conjunction with the LAN9221I must be rated for Industrial Temperature use.
EEPROM Interface:

1. EECS (pin 39) on the LAN9221I QFN connects to the external EEPROM’s CS pin.

2. EECLK (pin 40) on the LAN9221I QFN connects to the external EEPROM’s serial clock pin. This pin has an internal pull-up. See section “Internal Pull-up / Pull-down Augmentation” for details when operating the LAN9221I at VDDVARIO levels below +3.0V.

Caution: To ensure normal device operation, the EECLK pin must be high during any power-up and/or hardware reset event. Do not add any type of external pull-down or grounding connection to this pin as this will result in configuring the device disabled.

3. EEDIO (pin 38) on the LAN9221I QFN connects to the external EEPROM’s Data In pin. This pin on the LAN9221I is a bi-directional pin and it also connects to the EEPROM’s Data Out pin through a 10K Ω resistor.

4. Be sure to select a 3-wire style 1K EEPROM that is organized for 128 x 8-bit or the ability to be strapped for 128 x 8-bit operation. Recommended EEPROMs can be found in our LAN9118 Designing with the LAN9118 - Getting Started design guide, application note AN 12.5.

5. When operating at lower VDDVARIO levels, the designer should select an appropriate EEPROM that also operates at the same lower supply voltage.

EXRES Resistor:

1. EXRES (pin 50) on the LAN9221I QFN should connect to digital ground through a 12.4K Ω resistor with a tolerance of 1.0%. This pin is used to set-up critical bias currents for the embedded 10/100 Ethernet Physical device.
**Required External Pull-ups/Pull-downs:**

1. IRQ (pin 43) may require an external pull-up resistor if this output is programmed as an Open Drain type. This pull-up resistor should be referenced to the VDDVARIO supply.

2. PME (pin 41) may require an external pull-up resistor if this output is programmed as an Open Drain type. This pull-up resistor should be referenced to the VDDVARIO supply.

3. GPIO0/nLED1 (pin 3) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed for LED functionality, this pin indicates what speed (10/100) the Ethernet phy is currently set for. A pull-up resistor would also be required if this pin is programmed as an Open Drain Output. This pull-up resistor should be referenced to the VDDVARIO supply.

4. GPIO1/nLED2 (pin 4) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed for LED functionality, this pin indicates Link & Activity status of the Ethernet phy. A pull-up resistor would also be required if this pin is programmed as an Open Drain Output. This pull-up resistor should be referenced to the VDDVARIO supply.

5. GPIO2/nLED3 (pin 5) may require an external pull-up resistor if this pin is programmed in one of two ways. An external pull-up resistor would be required if this pin is programmed for the LED functionality. When programmed for LED functionality, this pin indicates what duplex mode (half/full) the Ethernet phy is currently set for. A pull-up resistor would also be required if this pin is programmed as an Open Drain Output. This pull-up resistor should be referenced to the VDDVARIO supply.

**CPU Interface:**

1. A1 – A7 Address Bus: Please refer to the latest revision of the LAN9221I Application Note for exact implementation of the CPU interface selected.

2. D0 – D15 Data Bus: Please refer to the latest revision of the LAN9221I Application Note for exact implementation of the CPU interface selected.

3. Control Signals: Please refer to the latest revision of the LAN9221I Application Note for exact implementation of the CPU interface selected.

4. The LAN9221I is a Little Endian LAN device. It is the designers’ responsibility to ensure that the selected CPU has compatible Endianess, as this may affect Data Bus connections to the LAN9221I. For example, if a Big Endian processor is used in conjunction with the LAN9221I, it may be necessary to swap data bus byte lanes in order to ensure proper system operation. Please refer to the latest LAN9221I data sheet and design guides to determine compatibility.
Internal Pull-up / Pull-down Augmentation:

1. There are four pins on the LAN9221I that rely on internal pull-ups or pull-downs to ensure that the device is initialized properly on power-up, reset and/or POR events. When using the LAN9221I at reduced VDDVARIO voltages (less than +3.0V), these four pins require external resistors to ensure the proper pull-up / pull-down configuration.

2. When operating the LAN9221I at VDDVARIO voltage levels higher than +3.0V, the designer should simply rely on the internal pull-ups / pull-downs of these four pins and not add any external compensation.

3. The EECLK (pin 40) requires an external pull-up resistor when using the LAN9221I with reduced VDDVARIO voltage levels. This pull-up resistor should be referenced to the VDDVARIO supply. For the proper resistor value, reference the table below.

4. The nRESET (pin 42) requires an external pull-up resistor when using the LAN9221I with reduced VDDVARIO voltage levels. This pull-up resistor should be referenced to the VDDVARIO supply. For the proper resistor value, reference the table below.

5. The AMDIX_EN (pin 52) requires an external pull-up resistor when using the LAN9221I with reduced VDDVARIO voltage levels. This pull-up resistor should be referenced to the VDDVARIO supply. For the proper resistor value, reference the table below.

6. The TEST (pin 14) requires an external 56.2 Ω pull-down resistor or ground connection when using the LAN9221I with reduced VDDVARIO voltage levels.

<table>
<thead>
<tr>
<th>I/O Voltage</th>
<th>Pull-up Resistor</th>
</tr>
</thead>
<tbody>
<tr>
<td>+3.3V ± 300 mV</td>
<td>10K Ω</td>
</tr>
<tr>
<td>+2.5V ± 10%</td>
<td>7.5K Ω</td>
</tr>
<tr>
<td>+1.8V ± 10%</td>
<td>4.7K Ω</td>
</tr>
</tbody>
</table>
Miscellaneous:

1. **TEST** (pin 14), for VDDVARIO operation above +3.0V, this pin must be left as a no-connect. See the section "Internal Pull-up / Pull-down Augmentation" for details when operating the LAN9221I at VDDVARIO levels below +3.0V.

2. **FIFO_SEL** (pin 13), when driven high, all accesses to the LAN9221I are to the RX or TX Data FIFOs. In this mode, the address input is ignored. Typical use will involve connecting an upper address line (A11 is recommended) to this pin to determine functionality. For normal operation (FIFO_SEL disabled), a 1.0K Ω external pull-down resistor must be attached to this pin.

3. **nRESET** (pin 42), this pin is an active-low reset input. This signal resets all logic and registers within the LAN9221I. This signal is pulled high with a weak internal pull-up resistor. The nRESET input cannot be left unconnected; the nRESET pin must be driven low after the +3.3V power supply is stable. See latest data sheet for timing details. See the section "Internal Pull-up / Pull-down Augmentation" for details when operating the LAN9221I at VDDVARIO levels below +3.0V.

4. **AMDX_EN** (pin 52), this pin enables the HP Auto MDIX feature of the LAN9221I. This pin has a weak internal pull-up, so this pin should be left as a no-connection in order to enable the Auto MDIX feature (default mode of operation). In order to disable the HP Auto MDIX feature, a 1.0K Ω pull-down resistor must be attached to this pin. See the section "Internal Pull-up / Pull-down Augmentation" for details when operating the LAN9221I at VDDVARIO levels below +3.0V.

5. Incorporate a large SMD resistor (SMD_1210) to connect the chassis ground to the digital ground. This will allow some flexibility at EMI testing for different grounding options. Leave the resistor out, the two grounds are separate. Short them together with a zero ohm resistor. Short them together with a cap or a ferrite bead for best performance.

6. Be sure to incorporate enough bulk capacitors (4.7 - 22μF caps) for each power plane.

7. In order to guarantee IEEE compliancy over the entire temperature range of operation, all components used in the customer's application must be rated for Industrial Temperature use. Processors, crystals, oscillators, magnetics and all integrated circuits must be rated properly to avoid operational inconsistencies.
**LAN9221I QFN QuickCheck Pinout Table:**

Use the following table to check the LAN9221I QFN shape in your schematic.

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Pin Name</th>
<th>Pin No.</th>
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<tr>
<td>1</td>
<td>VDD33REG</td>
<td>15</td>
<td>nRD</td>
<td>29</td>
<td>D6</td>
<td>43</td>
<td>IRQ</td>
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<td>2</td>
<td>VDD18CORE</td>
<td>16</td>
<td>nWR</td>
<td>30</td>
<td>VDDVARIO</td>
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<td>TPO-</td>
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<td>3</td>
<td>nLED1</td>
<td>17</td>
<td>nCS</td>
<td>31</td>
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<td>45</td>
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<td>48</td>
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<td>D13</td>
<td>35</td>
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<tr>
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<td>D7</td>
<td>42</td>
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<td>56</td>
<td>VDDVARIO</td>
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**Notes:**

- EDP Ground Connection
- Exposed Die Paddle Ground
- Pad on Bottom of Package
Reference Material:

1. SMSC LAN9221I Data Sheet; check web site for latest revision.

2. SMSC LAN9221I EVB Schematic, Assembly No. 6527; check web site for latest revision.

3. SMSC LAN9221I EVB PCB, Assembly No. 6527; order PCB from web site.

4. SMSC LAN9221I EVB PCB Bill of Materials, Assembly No. 6527; check web site for latest revision.

5. SMSC LAN9118 Design Guide, Designing with the LAN9118I – Getting Started, Application Note AN 12.5; check web site for latest revision.


7. SMSC Suggested Magnetics Application Note 8-13; check web site for latest revision.