## Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Revision Summary</th>
<th>Author</th>
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<tbody>
<tr>
<td>01A</td>
<td>21 07 14</td>
<td>Initial Version</td>
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<tr>
<td>02A</td>
<td>05 08 14</td>
<td>Review Comments updated</td>
<td>Manikandan.TB</td>
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<tr>
<td>A</td>
<td>14 08 14</td>
<td>Released for FAB</td>
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<tr>
<td>B</td>
<td>19 09 14</td>
<td>Released for FAB(Refer : /depot_hw_jutland/Validation/Post-Silicon/ EVB Design/EVB patch work details/Jutland EVB patch work details.xlsx)</td>
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<td>01C</td>
<td>13 11 15</td>
<td>Refer : /depot_hw_jutland/Validation/Post-Silicon/EVB Design/SCH+PCB+GBR+BOM files/EVB2-9252-HB&amp;SPI+GPIO/REV-C/EVB-LAN9252-HBI-REV-C_Requirement_list.xlsx</td>
<td>Senthil M</td>
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<td>C</td>
<td>28 DEC 15</td>
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<tr>
<td>D</td>
<td>12 FEB 15</td>
<td>U10 pin 4 &amp; 5 changed, U9 footprint updated</td>
<td>Manikandan.TB</td>
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<td></td>
<td></td>
<td>PIM SPI changed to SPI2, PIM TX,RX changed to Pin 51 &amp;52, RES R147,R148,R150 &amp; R151 deleted and RN1,RN2,RN3 &amp; RN4 added</td>
<td></td>
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<tr>
<td></td>
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<td>Released for FAB</td>
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### Page No. | Schematic Page
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1 | Title
2 | Block Diagram
3 | Power Supply & RST
4 | LAN9252(Part1)
5 | Copper Mode Interface
6 | SFP Interface
7 | STRAP,GPIO,I2C & FXLOS
8 | LAN9252(Part2)
9 | ON-Board-PIC32MX
10 | GPIO
11 | UART, ADC & DAC
12 | PIM
**POWER SUPPLY**

3 V REGULATOR, 3A  
(3V fixed when Rb=50kΩ)

**RESET Options**

Note:
1. POR -> Reset to ASIC & SOC (Default)
2. RESET O/P from ASIC -> Reset to EX-PHY (PORT2) & SOC : Only Ethercat sku
3. RESET from SOC (GPIO/RST-O/P) -> Reset to ASIC
4. RESET from Push Button -> Reset to ASIC & SOC

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**Reset Generator**

**TPS3125**  
SS03-5  
Threshold = 2.64V  
Delay = 180ms

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**SW2**  
sw_pb_2P

**U1**  
3_Amp

**U2**  
TPS3125

**U3**  
74LVC1G14

**D1**  
GRN

**R1**  
0R

**C1**  
4.7uF  
DNP

**R2**  
1K

**R4**  
470R  
1%

**R5**  
4.75K  
1%

**R6**  
10k  
1%

**R7**  
100Ω  
1%

**R8**  
1K

**C2**  
10uF  
25V  

**C3**  
0.1uF

**C4**  
2.2uF  

**C5**  
0.1uF

**C6**  
0.1uF  

**SW1**  
Switch SPDT, Slide  
PN: 160160325082

---

**TP1**  
RED

**TP2**  
ORANGE

**TP3**  
BLACK

**TP4**  
BLACK
Note: 
OSCVSS need to connect to Chip gnd.
Note: Capacitors C10 through C13 are optional for EMI purposes and are not populated on the LAN8740/41 evaluation board. These capacitors are required for operation in an EMI constrained environment.
### GPIO [0-2] & LED_POL_Strap

The diagram illustrates the connections for GPIOs [0-2] and LED_POL_Strap. The GPIOs are connected to LED conditions as follows:

- **GPIO0 = LED0, LEDPOL0, MNGT0**
- **GPIO1 = LED1, LEDPOL1, MNGT1**
- **GPIO2 = LED2, LEDPOL2, E2PSIZE**

#### Management/LED Polarity Strap

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Logic</th>
<th>Connector</th>
<th>LED Polarity Strap</th>
</tr>
</thead>
<tbody>
<tr>
<td>MNGT0</td>
<td>0</td>
<td>J48,J51 (1&amp;2)</td>
<td>The LED is set as active high.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>J48,J51 (1&amp;2)</td>
<td>The LED is set as active low.</td>
</tr>
<tr>
<td>MNGT1</td>
<td>0</td>
<td>J50,J53 (1&amp;2)</td>
<td>The LED is set as active high.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>J50,J53 (1&amp;2)</td>
<td>The LED is set as active low.</td>
</tr>
<tr>
<td>E2PSIZE</td>
<td>0</td>
<td>J49,J52 (1&amp;2)</td>
<td>The LED is set as active high. LEDPOL Strap: (9K-8) through 18K (2KX8)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>J49,J52 (1&amp;2)</td>
<td>The LED is set as active low. LEDPOL Strap: (9K-8) through 18K (2KX8) or 48K (512KX8) (LAN9052 only)</td>
</tr>
</tbody>
</table>

**Note:** To use GPIOs as LED

* Short 2-3 of both jumpers (ex. for GPIO0 short 2-3 of J48 & J51)

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### I2C EEPROM

- **I2C EEPROM Lower size:** Below 16K(2K x 8)
- **I2C EEPROM Higher size:** Above 16K(2K x 8)

**Signal Name** | **Connector** | **Logic** |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C2_SDA</td>
<td>J49,J52 (1&amp;2)</td>
<td>1</td>
</tr>
<tr>
<td>I2C2_SCL</td>
<td>J49,J52 (2&amp;3)</td>
<td>1</td>
</tr>
<tr>
<td>J50,J53 (1&amp;2)</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>J50,J53 (2&amp;3)</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Default:**
- **Copper mode:**
  - R77=1.2K & R78=1K
  - Level of 1.5 V selects FX-LOS for port A and FX-SD/Copper twisted pair for port B further determined by FXSDENB

---

### FX_Log_Strap_1 & 2

- **Default:**
  - Copper mode:
    - R77-12K & R78=Assemble
  - I2C EEPROM
  - Below 16K(2K x 8): R77=1.2K & R78=1K
  - Above 16K(2K x 8): R77=Assemble & R78=DNP

**FX_Log_Strap_1 & 2**

- **Default:**
  - Copper mode:
    - R77=1.2K & R78=1K
  - FX-LOS for port A and FX-SD/Copper twisted pair for port B further determined by FXSDENB

**FX_Mode_Strap_1 & 2**

- **Default:**
  - Copper mode:
    - R77=1.2K & R78=1K
  - Fiber Mode
    - R77=Assemble & R78=DNP

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### Microchip

Microchip Technology Inc.
### Digital INPUTS

Input = one (Default); Input = Zero (change the Switch position)

<table>
<thead>
<tr>
<th>GPIO</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>GP0</td>
<td>GP00</td>
</tr>
<tr>
<td>GP1</td>
<td>GP01</td>
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<tr>
<td>GP2</td>
<td>GP02</td>
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<tr>
<td>GP3</td>
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<td>GP14</td>
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<tr>
<td>GP15</td>
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### Digital OUTPUTS

<table>
<thead>
<tr>
<th>GPIO</th>
<th>Configuration</th>
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<tbody>
<tr>
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<td>GP00</td>
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<td>GP1</td>
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<td>GP14</td>
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<tr>
<td>GP15</td>
<td>GP15</td>
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</tbody>
</table>

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**Note:**
- **Digital INPUTS**
- **Digital OUTPUTS**
- Switche positions can be adjusted to change the input state.
**POT (Analog Input)**

Default Short

**Temp sensor**

**DAC (Analog output)**

Default Open

J26 Pin 2 = External Vref

Short J26 1-2 for Vref = 3V3

C87 & C88 = Default DNP

Assemble only when Vref is used

**RS-232 I/F**

Default Open

Short only when DAC need to be connect to onboard MX.
PIM unused GPIOs with GND probing option
PIM TXD & RXD can't be used in HBI mode. 
In other modes, TXD & RXD can be externally connected to UART.