Crystal-less™ Clock Generator
for
Baseboard Management Controller (BMC)
Overview

• Introduction to Discera’s Fully Integrated Crystal-less™ Timing Solution for Baseboard Management Controller (BMC)

  • DSC591-03
  • DSC592-03
Brief Definition of BMC

- Baseboard Management Controller (BMC) Functions
  - Processor that monitors server mainboard condition
  - Communicates status to IT through dedicated LAN
  - Allows IT to remotely address system issues
Current BMC Clocking Solution

- Oscillator generates 50MHz LVCMOS clock
- Additional clock fanout buffer
BMC Crystal-less™ Clock Generator

- Single device reduces BOM and saves space
  - Generates two synchronous low skew 50MHz outputs
  - Drives a total of 4 loads with synchronous outputs
  - Pin selects provide 8 independent drive options per output
  - Benefits of MEMS
BMC Clock Generator Solutions

• DSC591-03
  - 14 pin QFN Solution
    • Selectable output drive

• DSC591-02
  - 6 pin TDFN Solution
DSC591-03; 14 QFN

- **Features**
  - Crystal-less™, fully integrated clock generator
  - Two 50MHz LVCMOS outputs:
    - Selectable 50M/25MHz on CLK1
  - Eight output drive strength options
  - Wide temperature range: up to -55°C - 125°C
  - Wide supply voltage range: 2.25V to 3.6 V
    - Separate power supply on CLK1 and CLK0 for mixed voltage requirements

- **Benefits**
  - BOM and space savings
  - Simplifies clock trace layouts and tuning
  - Tunable EMI and signal integrity
  - Excellent ppm stability over temperature
  - PureSilicion™ MEMS
    - Excellent Immunity to Shock and Vibration; 1.2 FIT rate - 20x better than quartz
  - Eliminates the output divider network in mixed voltage supply applications (slide 12)
DSC591-02; 6 TDFN

• Features
  – Crystal-less™, fully integrated clock generator
  – Two 50MHz LVCMOS outputs:
  – Wide temperature range: up to -55°C - 125°C
  – Wide supply voltage range: 2.25V to 3.6 V
  – Small form factor and low profile 6 TDFN package

• Benefits
  – BOM and space savings
  – Simplifies clock trace layouts and tuning
  – Excellent ppm stability over temperature
  – PureSilicion™ MEMS
    • Excellent Immunity to Shock and Vibration;
    • 1.2 FIT rate - 20x better than quartz
Schematics Diagrams

- Place 0.1 µF capacitor as close as possible to VDD pins
- Damping resistors ‘R’ are optional on DSC591-03
  - Output drive may be programmed to eliminate ‘R’ on short traces (DSC591-03 only)
  - It is recommended that ‘R’ be placed on the PCB and populated with a 0 ohms resistor in the event where a damping resistor is not required
- Damping resistors R1 and R2 are required for traces longer than 2 inches
- OE pin has an internal pull-up, it maybe connected to a jumper or to an external signal to disable/enable the device dynamically.
C0S(0:2) = 101; CLK0 drive level at 11.5mA (IOH)
- Example shows CLK0 output is split at the source
- Drives BMC and LAN with minimized skew
C1S(0:2) = 100; CLK1 drive level at 10.1mA (IOH)
- Example shows CLK1 is split at the load
- Drives two LAN components in the same vicinity
LVCMOS Clock Tr/Tf Controls

- Eight (8) Rise and Fall time settings
- Controlled through pin strapping
  - Accommodate different trace length/load
  - Minimize overshoot and undershoot
  - Assist in controlling emission

<p>| VDD= 3.3V  | Output Drive Strength, Tr/Tf Select Bits |
| CL = 15pF  | [S2, S1, S0] - Default [111]             |</p>
<table>
<thead>
<tr>
<th>20%-80%</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>001</td>
</tr>
<tr>
<td>Tr (ns)</td>
<td>2.1</td>
</tr>
<tr>
<td>Tf (ns)</td>
<td>2.5</td>
</tr>
</tbody>
</table>
Mixed Supply on DSC591-03

• Applicable when outputs are driving loads in different power planes
  – VDD is main voltage supply to the device, controls CLK1
  – VDDO supplies CLK0 output buffer
  – VDDO ≤ VDD

• Eliminates external resistive divider network
  – Improves signal quality
  – Reduces power consumption
  – Reduces component count
  – Saves PCB space
Placement Recommendations

- Place DSC591/2-03 at even distance between the BMC and the dedicated LAN/PHY
  - Allows for minimizing trace snaking
  - Allows for equalizing trace length for lowest skew
- Route the 50MHz with the shortest possible trace
  - Trace from 22Ω to BMC = Trace from 22Ω to LAN
Trace Layout Consideration

- Avoid using vias on clock signal as they change the trace impedance, consequently causing reflection.
  - Attempt to layout clock traces on the same layer as the components
- If a bend is necessary make it with two 45° corners or by using round bend
- Avoid routing clock signals close to the board edge
- Reduce cross talk by routing the split clocks at a min distance of $A = 4 \times W$
  - $W$ is the width of the trace
## Competitive Advantages

<table>
<thead>
<tr>
<th></th>
<th>DSC591-03</th>
<th>XO + Buffer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Components</td>
<td>1</td>
<td>2-4</td>
</tr>
<tr>
<td>Drive Options per output</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>Frequency flexibility</td>
<td>50MHz or 25MHz</td>
<td>Require additional components</td>
</tr>
<tr>
<td>Temp Performance</td>
<td>-55°C to 125°C</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td>Shock Resistance</td>
<td>50,000G</td>
<td>100G</td>
</tr>
<tr>
<td>Vibration Resistance</td>
<td>70G</td>
<td>15G</td>
</tr>
<tr>
<td>Production Lead Time</td>
<td>2 Weeks</td>
<td>12-16 Weeks</td>
</tr>
</tbody>
</table>
Benefits of MEMS over Quartz

MEMS oscillators drop into standard oscillator footprints and offer advantages in performance, reliability, pricing, and time-to-market.

Performance: Stability & Jitter
- Up to 10ppm stability across full temperature range
- Temperature grades up to 125°C (vs. 85°C)
- Less than 0.5 ps phase noise jitter

Higher reliability
- Full AEC-Q100, JEDEC qualification
- 1.2 FIT reliability rates vs. 20 FIT for crystal
- 50,000 G shock and 70 G vibration tolerance (vs 200 G shock, 10 G vibration)

Cost Effective
- Semiconductor supply chain, without mechanical handling steps of crystal
- On CMOS pricing trend, scaling with chip geometry in Global, TSMC processes

Faster Time to Market
- 2 weeks production lead time vs. 8-16 weeks for crystal
- Engineering prototypes programmable in 1 sec with full production performance
## Best in Class Reliability

<table>
<thead>
<tr>
<th>MECHANICAL SHOCK</th>
<th>Discera MEMS Oscillators</th>
<th>Quartz Oscillators</th>
<th>Improvement over Quartz</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>50,000G</td>
<td>100G</td>
<td>500 x</td>
<td>MIL-STD-883; Method 2002</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VIBRATION</th>
<th>Discera MEMS Oscillators</th>
<th>Quartz Oscillators</th>
<th>Improvement over Quartz</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>70G</td>
<td>15G</td>
<td>4.6 x</td>
<td>MIL-STD-883; Method 2007</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>FIT (Failure in Time)</th>
<th>Discera MEMS Oscillators</th>
<th>Quartz Oscillators</th>
<th>Improvement over Quartz</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2</td>
<td>29</td>
<td>24 x</td>
<td>Confidence level = 90%</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DPPM</th>
<th>Discera MEMS Oscillators</th>
<th>Quartz Oscillators</th>
<th>Improvement over Quartz</th>
<th>Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 10</td>
<td>100</td>
<td>10 x</td>
<td>Over Production Lifetime</td>
<td></td>
</tr>
</tbody>
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MEMS stability over wider temp range

- Discera’s products maintain very low PPM over wider range of temperature
- Quartz based products drift exponentially beyond 70°C