**Introduction**

Atmel® | SMART SAM L21 is a series of Ultra low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor at max. 48MHz (2.46 CoreMark®/MHz) and up to 256KB Flash and 40KB of SRAM in a 32, 48, and 64 pin package. The sophisticated power management technologies, such as power domain gating, SleepWalking, Ultra low-power peripherals and more, allow for very low current consumptions. The highly configurable peripherals include a touch controller supporting capacitive interfaces with proximity sensing.

**Features**

- **Processor**
  - ARM Cortex-M0+ CPU running at up to 48MHz
  - Single-cycle hardware multiplier
  - Micro Trace Buffer

- **Memories**
  - 32/64/128/256KB in-system self-programmable Flash
  - 1/2/4/8KB Flash Read-While-Write section
  - 4/8/16/32KB SRAM Main Memory
  - 2/4/8/8KB SRAM Low power Memory

- **System**
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options
  - External Interrupt Controller (EIC)
  - 16 external interrupts
  - One non-maskable interrupt
  - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface

- **Low Power**
  - Idle, Standby, Backup, and Off sleep modes
  - SleepWalking peripherals
- Static and Dynamic Power Gating Architecture
- Battery backup support
- Two Performance Levels
- Embedded Buck/LDO regulator supporting on-the-fly selection

- Peripherals
  - 16-channel Direct Memory Access Controller (DMAC)
  - 12-channel Event System
  - Up to five 16-bit Timer/Counters (TC) including one low-power TC, each configurable as:
    • 16-bit TC with two compare/capture channels
    • 8-bit TC with two compare/capture channels
    • 32-bit TC with two compare/capture channels, by using two TCs
  - Two 24-bit and one 16-bit Timer/Counters for Control (TCC), with extended functions:
    • Up to four compare channels with optional complementary output
    • Generation of synchronized pulse width modulation (PWM) pattern across port pins
    • Deterministic fault protection, fast decay and configurable dead-time between complementary output
    • Dithering that increase resolution with up to 5 bit and reduce quantization error
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 interface
    • Embedded host and device function
    • Eight endpoints
  - Up to six Serial Communication Interfaces (SERCOM) including one low-power SERCOM, each configurable to operate as either:
    • USART with full-duplex and single-wire half-duplex configuration
    • I²C up to 3.4MHz
    • SPI
    • LIN slave
  - One AES encryption engine
  - One True Random Generator (TRNG)
  - One Configurable Custom Logic (CCL)
  - One 12-bit, 1MSPS Analog-to-Digital Converter (ADC) with up to 20 channels
    • Differential and single-ended input
    • Automatic offset and gain error compensation
    • Oversampling and decimation in hardware to support 13-, 14-, 15-, or 16-bit resolution
  - Two 12-bit, 1MSPS Dual Output Digital-to-Analog Converter (DAC)
  - Two Analog Comparators (AC) with window compare function
  - Three Operational Amplifiers (OPAMP)
  - Peripheral Touch Controller (PTC)
    • 169-Channel capacitive touch and proximity sensing
    • Wake-up on touch in standby mode

- Oscillators
  - 32.768kHz crystal oscillator (XOSC32K)
– 0.4-32MHz crystal oscillator (XOSC)
– 32.768kHz internal oscillator (OSC32K)
– 32.768kHz ultra-low-power internal oscillator (OSCLUDP32K)
– 16/12/8/4MHz high-accuracy internal oscillator (OSC16M)
– 48MHz Digital Frequency Locked Loop (DFLL48M)
– 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)

• I/O
  – Up to 51 programmable I/O pins

• Easy migration from SAM D family

• Packages
  – 64-pin TQFP, QFN, WLCSP
  – 48-pin TQFP, QFN
  – 32-pin TQFP, QFN

• Operating Voltage
  – 1.62V – 3.63V
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1. **Description**

Atmel® | SMART SAM L21 is a series of Ultra low-power microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, and ranging from 32- to 64-pins with up to 256KB Flash and 40KB of SRAM. The SAM L21 devices operate at a maximum frequency of 48MHz and reach 2.46 CoreMark®/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, Atmel Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The Atmel SAM L21 devices provide the following features: In-system programmable Flash, 16-channel direct memory access (DMA) controller, 12-channel Event System, programmable interrupt controller, up to 51 programmable I/O pins, 32-bit real-time clock and calendar, up to five 16-bit Timer/Counters (TC) and three Timer/Counters for Control (TCC) where each TC/TCC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and three timer/counters have extended functions optimized for motor, lighting and other control applications. Two TCC can operate in 24-bit mode, the third TCC can operate in 16-bit mode. The series provide one full-speed USB 2.0 embedded host and device interface; up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, I²C up to 3.4MHz, SMBus, PMBus, and LIN slave; up to twenty channel 1MSPS 12-bit ADC with programmable gain and optional oversampling and decimation supporting up to 16-bit resolution, two 12-bit 1MSPS DACs, two analog comparators with window mode, three independent cascadable OPAMPs supporting internal connection with others analog features, Peripheral Touch Controller supporting up to 192 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM L21 devices have four software-selectable sleep modes, idle, standby, backup and off. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped except those selected to continue running. In this mode all RAMs and logic contents are retained. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows some internal operation like DMA transfer and/or the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The SAM L21 devices have two software-selectable performance levels (PL0 and PL2) allowing the user to scale the lowest core voltage level that will support the operating frequency. To further minimize consumption, specifically leakage dissipation, the SAM L21 devices utilizes power domain gating technique with retention to turn off some logic area while keeping its logic state. This technique is fully handled by hardware.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for nonintrusive on-chip debugging of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.
The Atmel SAM L21 devices are supported with a full suite of programs and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.
## Configuration Summary

<table>
<thead>
<tr>
<th>Feature</th>
<th>SAM L21J</th>
<th>SAM L21G</th>
<th>SAM L21E</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pins</td>
<td>64</td>
<td>48</td>
<td>32</td>
</tr>
<tr>
<td>General Purpose I/O-pins (GPIOs)</td>
<td>51</td>
<td>37</td>
<td>25</td>
</tr>
<tr>
<td>Flash</td>
<td>256/128/64KB</td>
<td>256/128/64KB</td>
<td>256/128/64/32KB</td>
</tr>
<tr>
<td>Flash RWW section</td>
<td>8/4/2KB</td>
<td>8/4/2KB</td>
<td>8/4/2/1KB</td>
</tr>
<tr>
<td>System SRAM</td>
<td>32/16/8KB</td>
<td>32/16/8KB</td>
<td>32/16/8/4KB</td>
</tr>
<tr>
<td>Low Power SRAM</td>
<td>8/8/4KB</td>
<td>8/8/4KB</td>
<td>8/8/4/2KB</td>
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<tr>
<td>Timer Counter (TC) instances</td>
<td>5</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Waveform output channels per TC instance</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Timer Counter for Control (TCC) instances</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Waveform output channels per TCC</td>
<td>8/4/2</td>
<td>8/4/2</td>
<td>6/4/2</td>
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<tr>
<td>DMA channels</td>
<td>16</td>
<td>16</td>
<td>16</td>
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<tr>
<td>USB interface</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>AES engine</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>Configurable Custom Logic (CCL) (LUTs)</td>
<td>4</td>
<td>4</td>
<td>4</td>
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<tr>
<td>True Random Generator (TRNG)</td>
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<td>1</td>
<td>1</td>
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<tr>
<td>Serial Communication Interface (SERCOM) instances</td>
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<td>6</td>
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<tr>
<td>Analog-to-Digital Converter (ADC) channels</td>
<td>20</td>
<td>14</td>
<td>10</td>
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<tr>
<td>Analog Comparators (AC)</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Digital-to-Analog Converter (DAC) channels</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Operational Amplifier (OPAMP)</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>Feature</td>
<td>SAM L21J</td>
<td>SAM L21G</td>
<td>SAM L21E</td>
</tr>
<tr>
<td>---------------------------------------------</td>
<td>----------</td>
<td>----------</td>
<td>----------</td>
</tr>
<tr>
<td>Real-Time Counter (RTC)</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>RTC alarms</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>RTC compare values</td>
<td>One 32-bit value or two 16-bit values</td>
<td>One 32-bit value or two 16-bit values</td>
<td>One 32-bit value or two 16-bit values</td>
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<tr>
<td>External Interrupt lines</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>Peripheral Touch Controller (PTC) channels (X- x Y-Lines) for mutual capacitance (2)</td>
<td>169 (13x13)</td>
<td>81 (9x9)</td>
<td>42 (7x6)</td>
</tr>
<tr>
<td>Peripheral Touch Controller (PTC) channels for self capacitance (Y-Lines only) (3)</td>
<td>16</td>
<td>10</td>
<td>7</td>
</tr>
<tr>
<td>Maximum CPU frequency</td>
<td>48MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Packages</td>
<td>QFN</td>
<td>QFN</td>
<td>QFN</td>
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<tr>
<td></td>
<td>TQFP</td>
<td>TQFP</td>
<td>TQFP</td>
</tr>
<tr>
<td></td>
<td>WLCSP(4)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Oscillators</td>
<td>32.768kHz crystal oscillator (XOSC32K)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0.4-32MHz crystal oscillator (XOSC)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>32.768kHz internal oscillator (OSC32K)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>32KHz ultra-low-power internal oscillator (OSCULP32K)</td>
<td>96MHz Fractional Digital Phased Locked Loop (FDPLL96M)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>16/12/8/4MHz high-accuracy internal oscillator (OSC16M)</td>
<td>48MHz Digital Frequency Locked Loop (DFLL48M)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>48MHz Digital Frequency Locked Loop (DFLL48M)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Event System channels</td>
<td>12</td>
<td>12</td>
<td>12</td>
</tr>
<tr>
<td>SW Debug Interface</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Watchdog Timer (WDT)</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

**Note:**
1. For SAM L21E and SAM L21G, only TC0, TC1 and TC4 are available.
2. The number of X- and Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. Refer to *Multiplexed Signals* for details. The number in the Configuration Summary is the maximum number of channels that can be obtained.
3. The number of Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. The number given here is the maximum number of Y-lines that can be obtained.

4. WLCSP parts are programmed with a specific SPI bootloader. Refer to Application Note AT09002 for details.
3. Ordering Information

- **Product Family**
  - SAML = Low Power ULP Microcontroller

- **Product Series**
  - 21 = Cortex M0 + CPU, Advanced Feature Set + DMA + USB

- **Pin Count**
  - E = 32 Pins
  - G = 48 Pins
  - J = 64 Pins

- **Flash Memory Density**
  - 18 = 256KB
  - 17 = 128KB
  - 16 = 64KB
  - 15 = 32KB

- **Device Variant**
  - A = Engineering Samples Only
  - B = Released to Production

**Note:** The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

### 3.1. SAM L21J

#### Table 3-1. SAM L21J Ordering Codes

<table>
<thead>
<tr>
<th>Ordering Code</th>
<th>FLASH (bytes)</th>
<th>SRAM (bytes)</th>
<th>Package</th>
<th>Carrier Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATSAML21J16B-AUT</td>
<td>64K</td>
<td>8K</td>
<td>TQFP64</td>
<td>Tape &amp; Reel</td>
</tr>
<tr>
<td>ATSAML21J16B-MUT</td>
<td></td>
<td></td>
<td>QFN64</td>
<td></td>
</tr>
<tr>
<td>ATSAML21J17B-AUT</td>
<td>128K</td>
<td>16K</td>
<td>TQFP64</td>
<td>Tape &amp; Reel</td>
</tr>
<tr>
<td>ATSAML21J17B-MUT</td>
<td></td>
<td></td>
<td>QFN64</td>
<td></td>
</tr>
<tr>
<td>ATSAML21J17B-UUT</td>
<td></td>
<td></td>
<td>WLCSP64</td>
<td></td>
</tr>
<tr>
<td>ATSAML21J18B-AUT</td>
<td>256K</td>
<td>32K</td>
<td>TQFP64</td>
<td>Tape &amp; Reel</td>
</tr>
<tr>
<td>ATSAML21J18B-MUT</td>
<td></td>
<td></td>
<td>QFN64</td>
<td></td>
</tr>
<tr>
<td>ATSAML21J18B-UUT</td>
<td></td>
<td></td>
<td>WLCSP64</td>
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</tr>
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</table>
## 3.2. SAM L21G

### Table 3-2. SAM L21G Ordering Codes

<table>
<thead>
<tr>
<th>Ordering Code</th>
<th>FLASH (bytes)</th>
<th>SRAM (bytes)</th>
<th>Package</th>
<th>Carrier Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATSAML21G16B-AUT</td>
<td>64K</td>
<td>8K</td>
<td>TQFP48</td>
<td>Tape &amp; Reel</td>
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<tr>
<td>ATSAML21G16B-MUT</td>
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<td></td>
<td>QFN48</td>
<td></td>
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<tr>
<td>ATSAML21G17B-AUT</td>
<td>128K</td>
<td>16K</td>
<td>TQFP48</td>
<td>Tape &amp; Reel</td>
</tr>
<tr>
<td>ATSAML21G17B-MUT</td>
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<td>QFN48</td>
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<td>ATSAML21G18B-AUT</td>
<td>256K</td>
<td>32K</td>
<td>TQFP48</td>
<td>Tape &amp; Reel</td>
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<td>ATSAML21G18B-MUT</td>
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<td>QFN48</td>
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</table>

## 3.3. SAM L21E

### Table 3-3. SAM L21E

<table>
<thead>
<tr>
<th>Ordering Code</th>
<th>FLASH (bytes)</th>
<th>SRAM (bytes)</th>
<th>Package</th>
<th>Carrier Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATSAML21E15B-AUT</td>
<td>32K</td>
<td>4K</td>
<td>TQFP32</td>
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<td>ATSAML21E15B-MUT</td>
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<td>QFN32</td>
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<tr>
<td>ATSAML21E16B-AUT</td>
<td>64K</td>
<td>8K</td>
<td>TQFP32</td>
<td>Tape &amp; Reel</td>
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<tr>
<td>ATSAML21E16B-MUT</td>
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<td>QFN32</td>
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<tr>
<td>ATSAML21E17B-AUT</td>
<td>128K</td>
<td>16K</td>
<td>TQFP32</td>
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<td>ATSAML21E17B-MUT</td>
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<tr>
<td>ATSAML21E18B-AUT</td>
<td>256K</td>
<td>32K</td>
<td>TQFP32</td>
<td>Tape &amp; Reel</td>
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<td>ATSAML21E18B-MUT</td>
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<td></td>
<td>QFN32</td>
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</tbody>
</table>

## 3.4. Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM L21 variants have a reset value of DID=0x1081drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

### Table 3-4. SAM L21 Device Identification Values

<table>
<thead>
<tr>
<th>DEVSEL (DID[7:0])</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>SAML21J18A</td>
</tr>
<tr>
<td>0x01</td>
<td>SAML21J17A</td>
</tr>
<tr>
<td>0x02</td>
<td>SAML21J16A</td>
</tr>
<tr>
<td>0x03-0x04</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x05</td>
<td>SAML21G18A</td>
</tr>
<tr>
<td>DEVSEL (DID[7:0])</td>
<td>Device</td>
</tr>
<tr>
<td>-------------------</td>
<td>----------</td>
</tr>
<tr>
<td>0x06</td>
<td>SAML21G17A</td>
</tr>
<tr>
<td>0x07</td>
<td>SAML21G16A</td>
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<td>0x08-0x09</td>
<td>Reserved</td>
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<tr>
<td>0x0A</td>
<td>SAML21E18A</td>
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<tr>
<td>0x0B</td>
<td>SAML21E17A</td>
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<tr>
<td>0x0C</td>
<td>SAML21E16A</td>
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<td>0x0D</td>
<td>SAML21E15A</td>
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<td>SAML21E17B</td>
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<td>SAML21E16B</td>
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<td>0x1C</td>
<td>SAML21E15B</td>
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<tr>
<td>0x1D-0xFF</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Note:** The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.
4. Block Diagram

Note:
1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals.
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines.
5. Pinout

5.1. SAM L21J
5.2. SAM L21J WLCSP64

![SAM L21J WLCSP64 Diagram]

- **Digital Pin**
- **Analog Pin**
- **Oscillator**
- **Ground**
- **Input Supply**
- **Regulated Input/Output Supply**
- **Reset Pin**
5.3. SAM L21G
5.4. SAM L21E
6. Product Mapping

Figure 6-1. Atmel SAM L21 Product Mapping

Global Memory Space

- **Reserved**
- **System**
- **AHB-APB Bridge A**
- **AHB-APB Bridge B**
- **AHB-APB Bridge C**
- **AHB-APB Bridge D**
- **AHB-APB Bridge E**

**Code**

- **Internal Flash**
- **Reserved**

**SRAM**

- **Internal SRAM**
- **SRAM Low Power**

** peripherals**

**AHB-APB**

- **USB**
- **DSU**
- **NVMCTRL**
- **MTB**
- **PAC**
- **DMAC**
- **Reserved**

**AHB-APB Bridge A**

- **PM**
- **MCLK**
- **RSTC**
- **OSCCCTRL**
- **OSC32KCTRL**

**AHB-APB Bridge B**

- **SERCOM0**
- **SERCOM1**
- **SERCOM2**
- **SERCOM3**
- **SERCOM4**

**AHB-APB Bridge C**

- **TCC0**
- **TCC1**
- **TCC2**
- **TC0**
- **TC1**
- **TC2**
- **TC3**
- **DAC**
- **AES**
- **TRNG**

**AHB-APB Bridge D**

- **EVSYS**
- **SERCOM5**
- **TC4**
- **ADC**
- **AC**
- **PTC**
- **OPAMP**
- **CCL**

**AHB-APB Bridge E**

- **Reserved**

**System**

- **Reserved**
- **SCS**
- **ROMTable**
- **Reserved**
7. Processor and Architecture

7.1. Cortex M0+ Processor
The Atmel SAM L21 implements the ARM® Cortex™-M0+ processor, based on the ARMv6 Architecture and Thumb®-2 ISA. The Cortex M0+ is 100% instruction set compatible with its predecessor, the Cortex-M0 core, and upward compatible to Cortex-M3 and M4 cores. The implemented ARM Cortex-M0+ is revision r0p1. For more information refer to http://www.arm.com

7.1.1. Cortex M0+ Configuration

Table 7-1. Cortex M0+ Configuration in Atmel SAM L21

<table>
<thead>
<tr>
<th>Features</th>
<th>Cortex M0+ options</th>
<th>Atmel SAM L21 configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interrupts</td>
<td>External interrupts 0-32</td>
<td>29</td>
</tr>
<tr>
<td>Data endianness</td>
<td>Little-endian or big-endian</td>
<td>Little-endian</td>
</tr>
<tr>
<td>SysTick timer</td>
<td>Present or absent</td>
<td>Present</td>
</tr>
<tr>
<td>Number of watchpoint</td>
<td>0, 1, 2</td>
<td>2</td>
</tr>
<tr>
<td>comparators</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Number of breakpoint</td>
<td>0, 1, 2, 3, 4</td>
<td>4</td>
</tr>
<tr>
<td>comparators</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Halting debug support</td>
<td>Present or absent</td>
<td>Present</td>
</tr>
<tr>
<td>Multiplier</td>
<td>Fast or small</td>
<td>Fast (single cycle)</td>
</tr>
<tr>
<td>Single-cycle I/O port</td>
<td>Present or absent</td>
<td>Present</td>
</tr>
<tr>
<td>Wake-up interrupt controller</td>
<td>Supported or not supported</td>
<td>Not supported</td>
</tr>
<tr>
<td>Vector Table Offset Register</td>
<td>Present or absent</td>
<td>Present</td>
</tr>
<tr>
<td>Unprivileged/Privileged support</td>
<td>Present or absent</td>
<td>Absent - All software run in privileged mode only</td>
</tr>
<tr>
<td>Memory Protection Unit</td>
<td>Not present or 8-region</td>
<td>Not present</td>
</tr>
<tr>
<td>Reset all registers</td>
<td>Present or absent</td>
<td>Absent</td>
</tr>
<tr>
<td>Instruction fetch width</td>
<td>16-bit only or mostly 32-bit</td>
<td>32-bit</td>
</tr>
</tbody>
</table>

The ARM Cortex-M0+ core has two bus interfaces:

- Single 32-bit AMBA-3 AHB-Lite system interface that provides connections to peripherals and all system memory including Flash memory and RAM
- Single 32-bit I/O port bus interfacing to the PORT with 1-cycle loads and stores

7.1.1.1. Cortex M0+ Peripherals

- System Control Space (SCS)
  - The processor provides debug through registers in the SCS. Refer to the Cortex-M0+
- Nested Vectored Interrupt Controller (NVIC)
– External interrupt signals connect to the NVIC, and the NVIC prioritizes the interrupts. Software can set the priority of each interrupt. The NVIC and the Cortex-M0+ processor core are closely coupled, providing low latency interrupt processing and efficient processing of late arriving interrupts. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com).

**Note:** When the CPU frequency is much higher than the APB frequency it is recommended to insert a memory read barrier after each CPU write to registers mapped on the APB. Failing to do so in such conditions may lead to unexpected behavior such as e.g. re-entering a peripheral interrupt handler just after leaving it.

- **System Timer (SysTick)**
  - The System Timer is a 24-bit timer clocked by CLK_CPU that extends the functionality of both the processor and the NVIC. Refer to the Cortex-M0+ Technical Reference Manual for details (http://www.arm.com).

- **System Control Block (SCB)**
  - The System Control Block provides system implementation information, and system control. This includes configuration, control, and reporting of the system exceptions. Refer to the Cortex-M0+ Devices Generic User Guide for details (http://www.arm.com)

- **Micro Trace Buffer (MTB)**
  - The CoreSight MTB-M0+ (MTB) provides a simple execution trace capability to the Cortex-M0+ processor. Refer to section MTB-Micro Trace Buffer and the CoreSight MTB-M0+ Technical Reference Manual for details (http://www.arm.com).

**Related Links**

*Nested Vector Interrupt Controller* on page 21

### 7.1.1.2. Cortex M0+ Address Map

**Table 7-2. Cortex-M0+ Address Map**

<table>
<thead>
<tr>
<th>Address</th>
<th>Peripheral</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE000E000</td>
<td>System Control Space (SCS)</td>
</tr>
<tr>
<td>0xE000E010</td>
<td>System Timer (SysTick)</td>
</tr>
<tr>
<td>0xE000E100</td>
<td>Nested Vectored Interrupt Controller (NVIC)</td>
</tr>
<tr>
<td>0xE000ED00</td>
<td>System Control Block (SCB)</td>
</tr>
<tr>
<td>0x41006000</td>
<td>Micro Trace Buffer (MTB)</td>
</tr>
</tbody>
</table>

### 7.1.1.3. I/O Interface

The device allows direct access to PORT registers. Accesses to the AMBA® AHB-Lite™ and the single cycle I/O interface can be made concurrently, so the Cortex M0+ processor can fetch the next instructions while accessing the I/Os. This enables single cycle I/O access to be sustained for as long as necessary.

### 7.2. Nested Vector Interrupt Controller

#### 7.2.1. Overview

The Nested Vectored Interrupt Controller (NVIC) in the SAM L21 supports 32 interrupt lines with four different priority levels. For more details, refer to the Cortex-M0+ Technical Reference Manual (http://www.arm.com).
### 7.2.2. Interrupt Line Mapping

Each of the 28 interrupt lines is connected to one peripheral instance, as shown in the table below. Each peripheral can have one or more interrupt flags, located in the peripheral’s Interrupt Flag Status and Clear (INTFLAG) register.

An interrupt flag is set when the interrupt condition occurs. Each interrupt in the peripheral can be individually enabled by writing a 1 to the corresponding bit in the peripheral’s Interrupt Enable Set (INTENSET) register, and disabled by writing 1 to the corresponding bit in the peripheral’s Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated from the peripheral when the interrupt flag is set and the corresponding interrupt is enabled.

The interrupt requests for one peripheral are ORed together on system level, generating one interrupt request for each peripheral. An interrupt request will set the corresponding interrupt pending bit in the NVIC interrupt pending registers (SETPEND/CLRPEND bits in ISPR/ICPR).

For the NVIC to activate the interrupt, it must be enabled in the NVIC interrupt enable register (SETENA/CLRENA bits in ISER/ICER). The NVIC interrupt priority registers IPR0-IPR7 provide a priority field for each interrupt.

<table>
<thead>
<tr>
<th>Peripheral source</th>
<th>NVIC line</th>
</tr>
</thead>
<tbody>
<tr>
<td>EIC NMI – External Interrupt Controller</td>
<td>NMI</td>
</tr>
<tr>
<td>PM – Power Manager</td>
<td>0</td>
</tr>
<tr>
<td>MCLK - Main Clock</td>
<td></td>
</tr>
<tr>
<td>OSCCTRL - Oscillators Controller</td>
<td></td>
</tr>
<tr>
<td>OSC32KCTRL - 32KHz Oscillators Controller</td>
<td></td>
</tr>
<tr>
<td>SUPC - Supply Controller</td>
<td></td>
</tr>
<tr>
<td>PAC - Protecion Access Controller</td>
<td></td>
</tr>
<tr>
<td>WDT – Watchdog Timer</td>
<td>1</td>
</tr>
<tr>
<td>RTC – Real Time Counter</td>
<td>2</td>
</tr>
<tr>
<td>EIC – External Interrupt Controller</td>
<td>3</td>
</tr>
<tr>
<td>NVMCTRL – Non-Volatile Memory Controller</td>
<td>4</td>
</tr>
<tr>
<td>DMAC - Direct Memory Access Controller</td>
<td>5</td>
</tr>
<tr>
<td>USB - Universal Serial Bus</td>
<td>6</td>
</tr>
<tr>
<td>EVSYS – Event System</td>
<td>7</td>
</tr>
<tr>
<td>SERCOM0 – Serial Communication Interface</td>
<td>8</td>
</tr>
<tr>
<td>SERCOM1 – Serial Communication Interface</td>
<td>9</td>
</tr>
<tr>
<td>SERCOM2 – Serial Communication Interface</td>
<td>10</td>
</tr>
<tr>
<td>SERCOM3 – Serial Communication Interface</td>
<td>11</td>
</tr>
<tr>
<td>SERCOM4 – Serial Communication Interface</td>
<td>12</td>
</tr>
</tbody>
</table>
7.3. **Micro Trace Buffer**

7.3.1. **Features**

- Program flow tracing for the Cortex-M0+ processor
- MTB SRAM can be used for both trace and general purpose storage by the processor
- The position and size of the trace buffer in SRAM is configurable by software
- CoreSight compliant

7.3.2. **Overview**

When enabled, the MTB records the changes in program flow that are reported by the Cortex-M0+ processor over the execution trace interface. This interface is shared between the Cortex-M0+ processor and the CoreSight MTB-M0+. The information is stored by the MTB in the SRAM as trace packets. An off-chip debugger can extract the trace information using the Debug Access Port to read the trace information from the SRAM. The debugger can then reconstruct the program flow from this information.

The MTB stores trace information into the SRAM and gives the processor access to the SRAM simultaneously. The MTB ensures that trace write accesses have priority over processor accesses.

An execution trace packet consists of a pair of 32-bit words that the MTB generates when it detects a non-sequential change of the program pointer (PC) value. A non-sequential PC change can occur during branch instructions or during exception entry. See the CoreSight MTB-M0+ Technical Reference Manual for more details on the MTB execution trace packet format.

Tracing is enabled when the MASTER.EN bit in the Master Trace Control Register is 1. There are various ways to set the bit to 1 to start tracing, or to 0 to stop tracing. See the CoreSight Cortex-M0+ Technical Reference Manual for more details on the Trace start and stop and for a detailed description of the MTB’s...
MASTER register. The MTB can be programmed to stop tracing automatically when the memory fills to a specified watermark level or to start or stop tracing by writing directly to the MASTER.EN bit. If the watermark mechanism is not being used and the trace buffer overflows, then the buffer wraps around overwriting previous trace packets.

The base address of the MTB registers is 0x41006000; this address is also written in the CoreSight ROM Table. The offset of each register from the base address is fixed and as defined by the CoreSight MTB-M0+ Technical Reference Manual. The MTB has four programmable registers to control the behavior of the trace features:

- **POSITION**: Contains the trace write pointer and the wrap bit
- **MASTER**: Contains the main trace enable bit and other trace control fields
- **FLOW**: Contains the WATERMARK address and the AUTOSTOP and AUTOHALT control bits
- **BASE**: Indicates where the SRAM is located in the processor memory map. This register is provided to enable auto discovery of the MTB SRAM location by a debug agent

See the CoreSight MTB-M0+ Technical Reference Manual for a detailed description of these registers.

### 7.4. High-Speed Bus System

#### 7.4.1. Features

High-Speed Bus Matrix has the following features:

- Symmetric crossbar bus switch implementation
- Allows concurrent accesses from different masters to different slaves
- 32-bit data bus
- Operation at a one-to-one clock frequency with the bus masters

H2LBRIDGE has the following features:

- LP clock division support
- Write: Posted-write FIFO of 3 words, no bus stall until it is full
- Write: 1 cycle bus stall when full when LP clock is not divided
- 2 stall cycles on read when LP clock is not divided
- Ultra low latency mode:
  - Suitable when the HS clock frequency is not above half the maximum device clock frequency
  - Removes all intrinsic bridge stall cycles (except those needed for LP clock ratio adaptation)
  - Enabled by writing a ’1’ in 0x41008120 using a 32-bit write access

L2HBRIDGE has the following features:

- LP clock division support
- Write: Posted-write FIFO of 1 word, no bus stall until it is full
- Write: 1 cycle bus stall when full when LP clock is not divided
- 2 stall cycles on read when LP clock is not divided
- ultra low latency mode:
  - Suitable when the HS clock frequency is not above half the maximum device clock frequency
  - Removes all intrinsic bridge stall cycles (except those needed for LP clock ratio adaptation)
  - Enabled by writing a ’1’ in 0x41008120 using a 32-bit write access
7.4.2. Configuration

Figure 7-2. Master-Slave Relations High-Speed Bus Matrix

Figure 7-3. Master-Slave Relations Low-Power Bus Matrix
### Table 7-4. High-Speed Bus Matrix Masters

<table>
<thead>
<tr>
<th>High-Speed Bus Matrix Masters</th>
<th>Master ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>CM0+ - Cortex M0+ Processor</td>
<td>0</td>
</tr>
<tr>
<td>DSU - Device Service Unit</td>
<td>1</td>
</tr>
<tr>
<td>L2HBRIDGEM - Low-Power to High-Speed bus matrix AHB to AHB bridge</td>
<td>2</td>
</tr>
</tbody>
</table>

### Table 7-5. High-Speed Bus Matrix Slaves

<table>
<thead>
<tr>
<th>High-Speed Bus Matrix Slaves</th>
<th>Slave ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal Flash Memory</td>
<td>0</td>
</tr>
<tr>
<td>HS SRAM Port 0 - CM0+ Access</td>
<td>1</td>
</tr>
<tr>
<td>HS SRAM Port 1 - DSU Access</td>
<td>2</td>
</tr>
<tr>
<td>AHB-APB Bridge B</td>
<td>3</td>
</tr>
<tr>
<td>H2LBRIDGES - High-Speed to Low-Power bus matrix AHB to AHB bridge</td>
<td>4</td>
</tr>
</tbody>
</table>

### Table 7-6. Low-Power Bus Matrix Masters

<table>
<thead>
<tr>
<th>Low-Power Bus Matrix Masters</th>
<th>Master ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>H2LBRIDGEM - High-Speed to Low-Power bus matrix AHB to AHB bridge</td>
<td>0</td>
</tr>
<tr>
<td>DMAC - Direct Memory Access Controller - Data Access</td>
<td>2</td>
</tr>
</tbody>
</table>

### Table 7-7. Low-Power Bus Matrix Slaves

<table>
<thead>
<tr>
<th>Low-Power Bus Matrix Slaves</th>
<th>Slave ID</th>
</tr>
</thead>
<tbody>
<tr>
<td>AHB-APB Bridge A</td>
<td>0</td>
</tr>
<tr>
<td>AHB-APB Bridge C</td>
<td>1</td>
</tr>
<tr>
<td>AHB-APB Bridge D</td>
<td>2</td>
</tr>
<tr>
<td>AHB-APB Bridge E</td>
<td>3</td>
</tr>
<tr>
<td>LP SRAM Port 2- H2LBRIDGEM access</td>
<td>5</td>
</tr>
<tr>
<td>LP SRAM Port 1- DMAC access</td>
<td>7</td>
</tr>
<tr>
<td>L2HBRIDGES - Low-Power to High-Speed bus matrix AHB to AHB bridge</td>
<td>8</td>
</tr>
<tr>
<td>HS SRAM Port 2- HMATRIXLP access</td>
<td>9</td>
</tr>
</tbody>
</table>

#### 7.4.3. SRAM Quality of Service

To ensure that masters with latency requirements get sufficient priority when accessing RAM, priority levels can be assigned to the masters for different types of access.
The Quality of Service (QoS) level is independently selected for each master accessing the RAM. For any access to the RAM, the RAM also receives the QoS level. The QoS levels and their corresponding bit values for the QoS level configuration are shown in the following table.

Table 7-8. Quality of Service

<table>
<thead>
<tr>
<th>Value</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>DISABLE</td>
<td>Background (no sensitive operation)</td>
</tr>
<tr>
<td>0x1</td>
<td>LOW</td>
<td>Sensitive Bandwidth</td>
</tr>
<tr>
<td>0x2</td>
<td>MEDIUM</td>
<td>Sensitive Latency</td>
</tr>
<tr>
<td>0x3</td>
<td>HIGH</td>
<td>Critical Latency</td>
</tr>
</tbody>
</table>

If a master is configured with QoS level DISABLE (0x0) or LOW (0x1) there will be a minimum latency of one cycle for the RAM access.

The priority order for concurrent accesses are decided by two factors. First, the QoS level for the master and second, a static priority given by the port ID. The lowest port ID has the highest static priority. See the tables below for details.

The MTB has a fixed QoS level HIGH (0x3).

The CPU QoS level can be written/read, using 32-bit access only, at address 0x41008114 bits [1:0]. Its reset value is 0x3.

Refer to different master QOSCTRL registers for configuring QoS for the other masters (USB, DMAC).

Table 7-9. HS SRAM Port Connections QoS

<table>
<thead>
<tr>
<th>HS SRAM Port Connection</th>
<th>Port ID</th>
<th>Connection Type</th>
<th>QoS</th>
<th>default QoS</th>
</tr>
</thead>
<tbody>
<tr>
<td>MTB - Micro Trace Buffer</td>
<td>4</td>
<td>Direct</td>
<td>STATIC-3</td>
<td>0x3</td>
</tr>
<tr>
<td>USB - Universal Serial Bus</td>
<td>3</td>
<td>Direct</td>
<td>IP-QOSCTRL</td>
<td>0x3</td>
</tr>
<tr>
<td>HMATRIXLP - Low-Power Bus Matrix</td>
<td>2</td>
<td>Bus Matrix</td>
<td>0x44000934(1), bits[1:0]</td>
<td>0x2</td>
</tr>
<tr>
<td>DSU - Device Service Unit</td>
<td>1</td>
<td>Bus Matrix</td>
<td>0x4100201C(1)</td>
<td>0x2</td>
</tr>
<tr>
<td>CM0+ - Cortex M0+ Processor</td>
<td>0</td>
<td>Bus Matrix</td>
<td>0x41008114(1), bits[1:0]</td>
<td>0x3</td>
</tr>
</tbody>
</table>

Note:
1. Using 32-bit access only.

Table 7-10. LP SRAM Port Connections QoS

<table>
<thead>
<tr>
<th>LP SRAM Port Connection</th>
<th>Port ID</th>
<th>Connection Type</th>
<th>QoS</th>
<th>default QoS</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMAC - Direct Memory Access Controller - Write-Back Access</td>
<td>5, 6</td>
<td>Direct</td>
<td>IP-QOSCTRL.WRBQOS</td>
<td>0x2</td>
</tr>
<tr>
<td>DMAC - Direct Memory Access Controller - Fetch Access</td>
<td>3, 4</td>
<td>Direct</td>
<td>IP-QOSCTRL.FQOS</td>
<td>0x2</td>
</tr>
<tr>
<td>LP SRAM Port Connection</td>
<td>Port ID</td>
<td>Connection Type</td>
<td>QoS</td>
<td>default QoS</td>
</tr>
<tr>
<td>-------------------------</td>
<td>--------</td>
<td>-----------------</td>
<td>-----</td>
<td>------------</td>
</tr>
<tr>
<td>H2LBRIDGEM - HS to LP bus matrix AHB to AHB bridge</td>
<td>2</td>
<td>Bus Matrix</td>
<td>0x44000924&lt;sup&gt;(1)&lt;/sup&gt;, bits[1:0]</td>
<td>0x2</td>
</tr>
<tr>
<td>DMAC - Direct Memory Access Controller - Data Access</td>
<td>1</td>
<td>Bus Matrix</td>
<td>IP-QOSCTRL.DQOS</td>
<td>0x2</td>
</tr>
</tbody>
</table>

**Note:**
1. Using 32-bit access only.
8. Packaging Information

8.1. Thermal Considerations

8.1.1. Thermal Resistance Data

The following table summarizes the thermal resistance data depending on the package.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>$\theta_{JA}$</th>
<th>$\theta_{JC}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>32-pin TQFP</td>
<td>68°C/W</td>
<td>25.8°C/W</td>
</tr>
<tr>
<td>48-pin TQFP</td>
<td>78.8°C/W</td>
<td>12.3°C/W</td>
</tr>
<tr>
<td>64-pin TQFP</td>
<td>66.7°C/W</td>
<td>11.9°C/W</td>
</tr>
<tr>
<td>32-pin QFN</td>
<td>37.2°C/W</td>
<td>3.1°C/W</td>
</tr>
<tr>
<td>48-pin QFN</td>
<td>31.6°C/W</td>
<td>10.3°C/W</td>
</tr>
<tr>
<td>64-pin QFN</td>
<td>32.2°C/W</td>
<td>10.1°C/W</td>
</tr>
<tr>
<td>64-pin WLCSP</td>
<td>36.8°C/W</td>
<td>5.0°C/W</td>
</tr>
</tbody>
</table>

Related Links
Junction Temperature on page 29

8.1.2. Junction Temperature

The average chip-junction temperature, $T_J$, in °C can be obtained from the following:

1. $T_J = T_A + (P_D \times \theta_{JA})$
2. $T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$

where:
- $\theta_{JA}$ = Package thermal resistance, Junction-to-ambient (°C/W), see Thermal Resistance Data
- $\theta_{JC}$ = Package thermal resistance, Junction-to-case thermal resistance (°C/W), see Thermal Resistance Data
- $\theta_{HEATSINK}$ = Thermal resistance (°C/W) specification of the external cooling device
- $P_D$ = Device power consumption (W)
- $T_A$ = Ambient temperature (°C)

From the first equation, the user can derive the estimated lifetime of the chip and decide if a cooling device is necessary or not. If a cooling device is to be fitted on the chip, the second equation should be used to compute the resulting average chip-junction temperature $T_J$ in °C.

Related Links
Thermal Resistance Data on page 29
8.2. Package Drawings

8.2.1. 64-Ball WLCSP

Table 8-2. Device and Package Maximum Weight

<table>
<thead>
<tr>
<th>Ball</th>
<th>X COORD</th>
<th>Y COORD</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>-1.212</td>
<td>-1.5</td>
</tr>
<tr>
<td>B1</td>
<td>0.979</td>
<td>1.3</td>
</tr>
<tr>
<td>A5</td>
<td>0.173</td>
<td>-1.5</td>
</tr>
<tr>
<td>B2</td>
<td>0.965</td>
<td>-1.3</td>
</tr>
<tr>
<td>B4</td>
<td>0.147</td>
<td>-1.3</td>
</tr>
<tr>
<td>B6</td>
<td>0.519</td>
<td>-1.2</td>
</tr>
<tr>
<td>BE</td>
<td>1.212</td>
<td>-1.3</td>
</tr>
<tr>
<td>C1</td>
<td>-1.212</td>
<td>-1.3</td>
</tr>
<tr>
<td>C3</td>
<td>-0.191</td>
<td>-1.3</td>
</tr>
<tr>
<td>D1</td>
<td>2.172</td>
<td>-1.3</td>
</tr>
<tr>
<td>D3</td>
<td>0.509</td>
<td>-0.9</td>
</tr>
<tr>
<td>D6</td>
<td>0.173</td>
<td>-0.9</td>
</tr>
<tr>
<td>D8</td>
<td>1.212</td>
<td>-0.9</td>
</tr>
<tr>
<td>E1</td>
<td>-1.212</td>
<td>-0.9</td>
</tr>
<tr>
<td>E3</td>
<td>0.173</td>
<td>-0.9</td>
</tr>
<tr>
<td>F1</td>
<td>0.866</td>
<td>-0.5</td>
</tr>
<tr>
<td>F2</td>
<td>-0.865</td>
<td>-0.5</td>
</tr>
<tr>
<td>F4</td>
<td>-0.174</td>
<td>-0.5</td>
</tr>
</tbody>
</table>

Notes:
1. Dimension "b" is measured at the maximum ball diameter in a plane to the seating plane.
2. Applied to whole wafer.

Table 8-3. Package Characteristics

| Moisture Sensitivity Level | MSL1 |
8.2.2. 64 pin TQFP

Table 8-4. Package Reference

<table>
<thead>
<tr>
<th>JEDEC Drawing Reference</th>
<th>N/A</th>
</tr>
</thead>
<tbody>
<tr>
<td>JESD97 Classification</td>
<td>E1</td>
</tr>
</tbody>
</table>

Table 8-5. Device and Package Maximum Weight

| 300 | mg |

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing M8-026, Variation ACD.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side.
3. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Lead coplanarity is 0.10mm maximum.

Atmel Package Drawing Contact: packagedrawings@atmel.com

05/03/2013
Table 8-6. Package Characteristics

| Moisture Sensitivity Level | MSL3 |

Table 8-7. Package Reference

<table>
<thead>
<tr>
<th>JEDEC Drawing Reference</th>
<th>MS-026</th>
</tr>
</thead>
<tbody>
<tr>
<td>JESD97 Classification</td>
<td>E3</td>
</tr>
</tbody>
</table>
8.2.3. 64 pin QFN

**Note:** The exposed die attach pad is not connected electrically inside the device.

**Table 8-8. Device and Package Maximum Weight**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>mg</td>
</tr>
</tbody>
</table>

**Table 8-9. Package Characteristics**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Moisture Sensitivity Level</td>
<td>MSL3</td>
</tr>
</tbody>
</table>
Table 8-10. Package Reference

<table>
<thead>
<tr>
<th>JEDEC Drawing Reference</th>
<th>MO-220</th>
</tr>
</thead>
<tbody>
<tr>
<td>JESD97 Classification</td>
<td>E3</td>
</tr>
</tbody>
</table>

8.2.4. 48 pin TQFP

Table 8-11. Device and Package Maximum Weight

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>140 mg</td>
</tr>
</tbody>
</table>

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MS-026, Variation ABC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side.
3. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
4. Lead coplanarity is 0.10mm maximum.

10/04/2011

Package Drawing Contact: packagedrawings@atmel.com
8.2.5. 48 pin QFN

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Viatelco VSKD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

Note: The exposed die attach pad is not connected electrically inside the device.
Table 8-14. Device and Package Maximum Weight

<table>
<thead>
<tr>
<th>Weight</th>
<th>mg</th>
</tr>
</thead>
<tbody>
<tr>
<td>140</td>
<td></td>
</tr>
</tbody>
</table>

Table 8-15. Package Characteristics

| Moisture Sensitivity Level | MSL3 |

Table 8-16. Package Reference

<table>
<thead>
<tr>
<th>JEDEC Drawing Reference</th>
<th>MO-220</th>
</tr>
</thead>
<tbody>
<tr>
<td>JESD97 Classification</td>
<td>E3</td>
</tr>
</tbody>
</table>
8.2.6. 32 pin TQFP

Table 8-17. Device and Package Maximum Weight

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>mg</td>
</tr>
</tbody>
</table>

Table 8-18. Package Characteristics

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Moisture Sensitivity Level</td>
<td>MSL3</td>
</tr>
</tbody>
</table>
8.2.7. 32 pin QFN

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VHDD-5, for proper dimensions, tolerances, etc.

2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.

   If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

---

Atmel

Packing Drawing Contact:
pkgdrawing@atmel.com

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Table 8-20. Device and Package Maximum Weight

| mg |
Table 8-21. Package Characteristics

| Moisture Sensitivity Level | MSL3 |

Table 8-22. Package Reference

| JEDEC Drawing Reference   | MO-220 |
| JESD97 Classification     | E3     |

8.3. Soldering Profile

The following table gives the recommended soldering profile from J-STD-20.

Table 8-23.

<table>
<thead>
<tr>
<th>Profile Feature</th>
<th>Green Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Ramp-up Rate (217°C to peak)</td>
<td>3°C/s max.</td>
</tr>
<tr>
<td>Preheat Temperature 175°C ±25°C</td>
<td>150-200°C</td>
</tr>
<tr>
<td>Time Maintained Above 217°C</td>
<td>60-150s</td>
</tr>
<tr>
<td>Time within 5°C of Actual Peak Temperature</td>
<td>30s</td>
</tr>
<tr>
<td>Peak Temperature Range</td>
<td>260°C</td>
</tr>
<tr>
<td>Ramp-down Rate</td>
<td>6°C/s max.</td>
</tr>
<tr>
<td>Time 25°C to Peak Temperature</td>
<td>8 minutes max.</td>
</tr>
</tbody>
</table>

A maximum of three reflow passes is allowed per component.