Features

- 4 Mbits On-Chip Flash Array
- Memory Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)
- In-System Programming (ISP) via Two Wire Interface (TWI)
- Simple Interface to SRAM FPGAs
- Compatible with Atmel FPGA devices
- Cascadable Read-Back to Support Additional Configurations or Higher-Density Arrays
- Memory Write Protection
- Programmable Reset Polarity
- Low-power Rad-Hard non volatile 0.15µm CMOS process
- Operating range:
  - Voltage: 3V to 3.6V
  - Temperature: -55°C to +125°C
- Operating power consumption: 72 mW max
- High-Reliability:
  - Endurance: 50,000 write cycles (in page mode)
  - Data retention: 10 Years @ 125°C
- Radiation Tolerance (test report available on request):
  - No Single Event Latch-up below a LET Threshold of 95 MeV/mg/cm² @125°C
    - No corruption of the memory cells during the SEU test
  - Total Dose according to MIL-STD-883 Method 1019:
    - biased (read mode): tested up to 20 krad (Si)
    - unbiased: tested up to 60 krad (Si)
- Quality Grades:
  - QML-V or Q
- Package: 305 Milis FP18
- Mass: 1 g
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1. **Description**

The AT69170F FPGA configuration memory (configurator) is an electrically erasable and re-programmable RadHard memory organized as 4Mx1bit. It is an easy-to-use and cost-effective configuration memory for space Field Programmable Grid Array (FPGA). It is manufactured with ATMEL low power non volatile CMOS RadHard process.

It is packaged in the 18-pin 305 Mils wide Flat Pack package. AT69170F uses a simple serial-access procedure to configure one or more FPGA devices. A two wire interface (TWI) is available for memory programmanation.

The user can select the polarity of the reset function by programming a dedicated sequence. These devices also support a write-protection mechanism within its programming mode.

Preliminary analysis shows there is a risk of SEGR in write mode above a LET threshold of 67.7 MeV/mg/cm² and above a temperature of 85°C. Without a complete characterization of the SEGR phenomena, ATMEL recommends to activate the write protection (see Section 8.5.3.1, “Data Protection” on page 22) in space flights configurations to prevent writing operations. Atmel shall not be liable for eventual damages if these conditions are not met.

2. **Block Diagram**
3. Pin Configuration

3.1 Package Description

The AT69170F is packaged in a 18-pins flat pack package.

![Figure 3-1.- Pin assignment](image)

Note: The package lid is connected to GND
### 3.2 Pin Description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Name and Function</th>
<th>Type</th>
</tr>
</thead>
</table>
| **VCC** | Power Supply input  
The VCC pin is used to supply the source voltage to the device. Operations at invalid VCC voltages may produce spurious results and should not be attempted. It is recommended to implement a decoupling capacitor on each pair of VCC/GND. | Power |
| **GND** | Ground pin  
The ground reference for the power supply. GND should be connected to the system ground. | Power |
| **RESET** | Reset input (operates only in Dump Mode)  
The polarity of this input is programmable. For Atmel FPGA’s, the RESET pin should be programmed active low and connected to the FPGA’s INIT pin (see Figure 9-3 on page 25). When the RESET pin is active, both address and bit counters are reset. This pin does not reset the device in the Two-Wire serial programming mode (SER_EN low). | Input |
| **CLK** | Clock input  
The clock input is used to increment the internal address and bit counters for reading and programming. In Two-Wire serial programming mode (SER_EN Low), the CLK pin must be compliant with the TWI frame description provided in Section 8. “TWI mode” on page 8. In Dump Mode, the serial data will be provided on the CLK's falling edge (see Figure 10-5 on page 33). | Input |
| **CE** | Chip Enable input (active low, operates only in Dump Mode)  
Low : address counter is incremented by CLK.  
High : address and bit counters are disabled.  
This pin has no effect on the device in the Two-Wire serial programming mode (SER_EN Low). | Input |
### Table 3-1. Pin Description

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Name and Function</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A2/CEO</strong></td>
<td><strong>A2 : device selection input (operates only in TWI mode)</strong>&lt;br&gt;Device selection input is used to configure the device address for multiple device configuration. A2 enables to attach two AT69170F devices on the same bus (SER_EN low). A2 pin configured to a logic “0” or “1” level. It is recommended to connect it to GND or VCC through a 10 kΩ pull-up resistor.&lt;br&gt;<strong>CEO : Chip Enable Output (operates only in DUMP mode)</strong>&lt;br&gt;CCEO is an active low output which goes low when the address counter of the memory has reached the end of the memory plan. In a daisy chain mode including multiple AT69170F devices, the CEO pin of a device is connected to the CE input of the following device in the chain. (see Figure 10. on page 29).</td>
<td>Input / Output</td>
</tr>
<tr>
<td><strong>SER_EN</strong></td>
<td><strong>Serial Mode Enable input (active low)</strong>&lt;br&gt;Low : Two-Wire serial programming mode&lt;br&gt;High : Dump Mode.&lt;br&gt;For applications not using the TWI serial mode, SER_EN should be tied to VCC.</td>
<td>Input</td>
</tr>
<tr>
<td><strong>DATA</strong></td>
<td><strong>DATA I/O</strong>&lt;br&gt;It is an open-drain bi-directional pin in TWI mode (SER_EN Low).&lt;br&gt;It is an output in Dump Mode (SER_EN high)</td>
<td>Input/Output</td>
</tr>
<tr>
<td><strong>READY</strong></td>
<td><strong>Open-drain reset state output</strong>&lt;br&gt;It is an open-drain output. The READY is driven low during Power-On Reset. It is recommended to use a 4.7 kΩ pull-up resistor.&lt;br&gt;The device does not operate while this signal remains low.</td>
<td>Output</td>
</tr>
<tr>
<td><strong>Reserved</strong></td>
<td>Those pins are bonded internally for the manufacturing tests. <strong>DO NOT CONNECT.</strong></td>
<td></td>
</tr>
</tbody>
</table>
4. **Device Modes Summary**

Table 4-1. Device Modes Summary

<table>
<thead>
<tr>
<th>INPUT</th>
<th>I/O</th>
<th>OUTPUT</th>
<th>DEVICE MODES</th>
</tr>
</thead>
<tbody>
<tr>
<td>SER_EN</td>
<td>RESET</td>
<td>CE</td>
<td>CLK</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>A</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>I</td>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>H</td>
<td>I</td>
<td>L</td>
<td>Running</td>
</tr>
<tr>
<td>H</td>
<td>I</td>
<td>L</td>
<td>Running</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
<td>Running</td>
</tr>
</tbody>
</table>

X: means don't care between H or L
A: means Active State
I: means Inactive State
HZ: means High Impedance

The active level of the RESET pin depends on the reset polarity configuration.

5. **Factory Settings**

The following table lists the parameters that can be changed by the user and their respective factory settings. Those parameters can be changed by means of special functions described in Section 8.5.3 on page 22.

Table 5-1. Factory Settings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Factory Setting</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Protection</td>
<td>Disabled</td>
<td>The changing procedure is described in Section 8.5.3.1 on page 22</td>
</tr>
<tr>
<td>RESET pin</td>
<td>Active low</td>
<td>The changing procedure is described in Section 8.5.3.2 on page 23</td>
</tr>
</tbody>
</table>

6. **Power-On initialisation**

The AT69170F provides a READY output pin to indicate that the memory power-on sequence is completed and ready for use.

7. **Standby Mode**

The AT69170F enters in a standby mode whenever CE input pin is asserted high in FPGA loading mode. In standby mode, the data output pin remains in high impedance.
8. TWI mode

8.1 Definitions

MASTER: any TWI device controlling the transfer of data, such as a microprocessor.
SLAVE: device being controlled. EEPROMs are always considered as slaves.
TRANSMITTER: device currently sending data on the bus. May be either a master or a slave.
RECEIVER: device currently receiving data on the bus. May be either a master or a slave.
WORD: 32 bit of data, formatted as a 4-byte packet.
PAGE: 128 sequential word locations starting at 3-byte address boundary, that may be programmed during a "page write" programming cycle.

8.2 TWI Bus Description

The internal memory of the AT69170F is accessed through a TWI bus which is enabled when SER_EN pin is driven Low.

The TWI is a bi-directional 2-wire bus which supports a serial synchronous data transmission protocol. A device that sends data onto the bus (DATA wire) is defined as transmitter and a device receiving data as receiver. The bus works in Master/Slave mode. Several slave and master devices can be attached to the bus but only one master and one slave can communicate at a time. The bus is always controlled by the master device which generates the serial clock (CLK wire), controls the bus access and generates the START and STOP conditions. Both master and slaves can operate as transmitter and receiver but the master determines which mode is activated. The slave devices are identified by a unique address on the bus and only one slave can be selected at a time by the master. The data sent onto the bus by the transmitter are acknowledged by the receiver.

The AT69170F is a Slave Transmitter / Receiver.

8.3 TWI Bus Characteristics

The following bus conditions have been defined.

8.3.1 Bus Ready

The bus is ready when both data and clock lines remain high. A data transfer may be initiated only when the bus is ready.

8.3.2 Start and Stop Conditions

A high to low transition of the DATA line while the clock (CLK) is high determines a START condition.
A low to high transition of the DATA line while the clock (CLK) is high determines a STOP condition.
All data transfers must be preceded by a START condition and terminated by a STOP condition.

Figure 8-1.- Typical System Configuration
8.3.3 Clock and Data Transitions

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the high period of the clock signal. The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of the data bytes transferred between the START and the STOP conditions is determined by the maximum page size (see Section 8.4). Changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

8.3.4 Acknowledge

Each receiver, when addressed, must generate an acknowledge after the reception of each byte. The master must generate an extra clock pulse which is associated with this acknowledge bit.

Note: the AT69170F does not generate any acknowledge bit if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the DATA line during the acknowledge clock pulse in such a way that the DATA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out by the slave. In this case, the slave must leave the data line high to enable the master to generate the STOP condition.
8.3.5 Device Addressing

The first byte sent by the master after the START condition is the control byte. It enables the master to select a unique slave on the bus and indicate if the access is a read or a write operation.

The control byte is composed of three fields:

- **Device Class Identifier**: the TWI bus is designed to support a variety of devices such as RAMs, EPROMs etc., along with EEPROMs. Hence to properly identify various devices on the TWI bus, a 4-bit “Device Class” identifier string is used. For EEPROMs, the string is 1010.

- **Device Address**: When multiple devices of the same type (e.g., multiple EEPROMs) are present on the TWI bus, the Device Address is used to properly identify the device in the Class.
  
  The device Address of the AT69170F is “A2 1 1”. A2 is the value of A2 pin. This address allows as many as two AT69170F on the same bus.

- **Read/Write bit**: the last bit of the control byte indicates if the access is Read or Write. If the bit is “1”, then the access is Read, whereas if the bit is “0”, then the access is Write.

![Control Byte Format Diagram](image-url)

The most significant bit (MSB) of the control byte is transmitted first on the TWI bus.

The TWI addresses of the memory device are supplied in the table below.

<table>
<thead>
<tr>
<th>Device Class Identifier</th>
<th>Device Address</th>
<th>Read / Write bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0 1 0</td>
<td>A2 1 1</td>
<td>R/W</td>
</tr>
</tbody>
</table>

Figure 8-5.- Control Byte Format
8.3.6 Internal Memory Addressing

The internal memory of the AT69170F is based on a 32-bit architecture interface and is accessed by pages of 128 words. A word is 32 bit wide. The AT69170F has a size of 1024 pages.

Therefore a word address is composed of 17 bits which means that 3 bytes are necessary to define a word address. The word address is encoded in a TWI frame as described herafter:

![Figure 8-6.- Internal Memory Access](image)

![Figure 8-7.- TWI Word Address Format](image)
The word address must be shift left by two bits when encoded in a TWI frame. The unused bits must be cleared. The most significant byte of the word address is transmitted first and the most significant bit of a byte is transmitted first. Each byte of a word address must be acknowledged by the receiver device.

8.3.7 Data Packets

The data packets are composed of an integer number of words and are encoded in a TWI frame in the following manner:

![TWI Data Packets format](image)

The data packets encoded in TWI frames must be multiples of a data word. The most significant word of a data packet and the most significant byte of a data word are transmitted first while the least significant bit of a byte is transmitted first.
8.4 TWI Operations

8.4.1 Write Operations

8.4.1.1 Page Write Sequence

In programming mode, the internal memory of AT69170F is organized as 1024 pages of 128 words. This organization involves that it’s not possible to program an amount of data lower than a page during a write operation. A page is written through an internal FIFO buffer of 128 words. The buffer is filled by a unique TWI sequence called Page Write Sequence.

The Stop Condition of a Page Write Sequence generates an internal write cycle whose maximum duration is $T_{WR}$ (see Table 10-5 on page 33). During this time, the AT69170F ignores the DATA and CLK signals and does not acknowledge any bytes that a transmitter could send.

A power loss during the reception of a Page Write Sequence does not damage the memory contents while a STOP condition is not received. However, the data packet is lost and must be resent by the master.

A Page Write Sequence frame is composed of the following fields:

- Control Byte
- Word Address
- Data Packet

The figure below describes a Page Write Sequence.
The Data Packet field contains all the words that will be written to the buffer during a Page Write Sequence. Only an integer number of words is allowed.

The Word Address field contains only the address of the first word of the Data Packet field. This address is shifted left by two bits and the two least significant bits of the Word Address field are cleared. The Data Word Address is copied by the device into an internal Address Counter. The rest of data word addresses are internally generated by an automatic incrementation of the Address Counter. This involves that the buffer must be written by a packet of contiguous data words locations. The number of data words can range from 1 to 128. In case, the buffer is not entirely filled, the unwritten words are set to “FF FF FF FF” by default.
The Word Address field is composed of two sections:
- the Device Memory Page
- the Buffer Address

The Device Memory Page ranges from 0 to 1023 while the Buffer Address ranges from 0 to 127.

A Page Write Sequence operation can be initiated to begin at any location within the buffer, but then the entire buffer only is written to the memory page during a Write Cycle.

To modify a byte within a memory page, it is therefore necessary to read the entire page, modify the byte within the page and perform a Page Write Sequence operation.

When the Buffer Address reaches the buffer boundary and additional locations are continued to be accessed, the address “rolls over” from the last word to the first word of the buffer and previous data words are overwritten.

### 8.4.1.2 Page Write Header

The programming of the entire device memory or part of, must be always performed by means of Page Write sequences preceded by a Page Write Header.

The Page Write Header is composed of the following TWI sequences:
- write “AA AA AA AA” at address “05 55 55”
- write “55 55 55 55” at address “02 AA AA”
- write “00 00 00 F4” at address “05 55 55”
- write “AA AA AA AA” at address “05 55 55”
- write “55 55 55 55” at address “02 AA AA”
- write “00 00 00 00” at address “05 55 55”

See figure below for a complete description of the page Write Header.
The figure below describes the complete writing process of the device memory.

![Writing process of the device memory](image)

**Figure 8-12.** Writing process of the device memory

### 8.4.1.3 Acknowledge Polling

Since the AT69170F does not acknowledge during a write cycle, this can be used to determine when the cycle is complete. This feature can be used to maximize bus throughput. Once the stop condition for a Page Write has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/W=0). If the AT69170F is still busy with the write cycle, then no ACK is returned. If the write cycle is complete, then the AT69170F returns the ACK and the master can then proceed with the next write or read operation. See figure below for the flow chart.

An alternative way to the acknowledge polling would be to wait for a $t_{WR}$ time before initiating the next write or read operation.
8.4.2 Read Operations

For read operations, the internal memory of AT69170F is directly accessed by the TWI bus in 32-bit mode. Internally the AT69170F contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or a write) is done to address N, the next read operation will access data word from address N+1.

When address N reaches the device memory boundary, the address counter is incremented by one and the word address “rolls-over” from the last to the first location of the memory.

Read operations are initiated in the same manner as write operations. There are two basic read operations:

- random read
- sequential read

8.4.2.1 Random Read

A random read requires a word address write sequence to load in the address counter. Once the control byte and the word address are clocked in and acknowledged by the AT69170F, the master must generate another start condition. Then, the master initiates a read sequence by sending a control byte with the R/W bit set to “1”. The AT69170F acknowledges the control byte and serially clocks out the data word. The master acknowledges all the bytes except the last one and then generates a stop condition to discontinue the transmission.
Sequential reads must be initiated as random read access. The first word is clocked out by AT69170F in the same manner as the random read mode. However, the master now responds with an acknowledge indicating it requires additional data. As long as the AT69170F receives an acknowledge, it continues to increment the word address and serially clock out sequential data words. The read operation is terminated by the master which does not acknowledge the reception of the last byte but does generate the stop condition.

The data output is sequential, with the word from address N followed by the word from address N+1. The address counter for read operations increments all the byte addresses of a data word, allowing the entire memory contents to be serially read during one operation. When the memory address limit is reached, the word address will “roll-over” from the last to the first location of the memory and the AT69170F continues to output data for each acknowledge received.
8.5 Special Functions

The AT69170F supports special functions that are accessible by commands sent through the TWI bus.

A Special Function command is obtained by the concatenation of special basic commands.

A special basic command frame is composed of the following fields:

- Control Byte
- Special Word Address
- Special Word Data

See figure below for a complete description of a special basic command frame.
A special basic command is differentiated from a normal read/write operation by means of the address field. The address word of read/write operations is shift left by two bits while the address word for special basic commands is not. The two least significant bits of the word address field are always cleared for read/write operations while they cannot be simultaneously equal to zero (A1A0 <> 0) for special basic commands.

The **least significant byte of a data word** and the **least significant bit of a byte** are transmitted first.

Special Functions commands allow to read or write configurations which are saved by means of internal fuse bits.

**8.5.1 Configuration Write Function**

The Configuration Write Function is built by the concatenation of the following special basic commands:

- write “AA AA AA AA” at address “05 55 55”
- write “55 55 55 55” at address “02 AA AA”
- write “Word Code” at address “05 55 55”
- write “AA AA AA AA” at address “05 55 55”
- write “55 55 55 55” at address “02 AA AA”
- write “00 00 00 00” at address “05 55 55”

See figure below for a complete description of the Configuration Write Function
The Configuration Write Functions are listed hereafter:

- Data Protection
- Chip Reset Polarity
- Full Chip Erase

8.5.2 Configuration Read Function

The Configuration Read Function is built by the concatenation of the following special basic commands:

- write “AA AA AA AA” at address “05 55 55”
- write “55 55 55 55” at address “02 AA AA”
- write “Code Word” at address “05 55 55”
- read “Data Word” from address “00 00 01”
- write “AA AA AA AA” at address “05 55 55”
- write “55 55 55 55” at address “02 AA AA”
- write “00 00 00 00” at address “05 55 55”

See figure below for a complete description of the Configuration Read Function.
8.5.3 Special Functions

8.5.3.1 Data Protection

The AT69170F has a “Write Protection” feature that disables data write capability to the memory. When the lock is activated, the data uploaded into the buffer is not written to the memory which preserves its content.

The write protection is managed by an internal fuse bit only as the AT69170F does not provide any write protect pin.

Table 8-2. Data Protection Commands

<table>
<thead>
<tr>
<th>Special Function Name</th>
<th>Description</th>
<th>Operation</th>
<th>Code Word</th>
<th>Data Word</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable Data Protection</td>
<td>Memory data protection is activated</td>
<td>Write</td>
<td>00 00 00 A0</td>
<td></td>
</tr>
<tr>
<td>Disable Data Protection</td>
<td>Memory data protection is deactivated</td>
<td>Write</td>
<td>00 00 00 20</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Read</td>
<td>00 00 00 F2</td>
<td>00 XX XX XX : Memory is not write protected</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>FF XX XX XX : Memory is write protected</td>
</tr>
</tbody>
</table>
The “Enable Data Protection” command must be followed by one and only one page write command for the memory device to be correctly programmed and write protected. This means that the “Enable Data Protection” command must be received by the memory device before the last page write command during a memory programming operation. If this condition is not fulfilled, the memory device is not correctly programmed.

When the memory device is write protected, the only way to deactivate the memory protection is to apply the “Disable Data Protection” command. It’s not possible to perform a Full Chip Erase operation when the memory device is write protected.

By default, the device is supplied with memory data protection deactivated.

**Important Note**: read Section 1., “Description” on page 3.

### 8.5.3.2 Chip Reset Polarity

The AT69170F allows the user to configure the polarity of the RESET pin as either active low or active high. This feature allows the memory device to work with various FPGA families. The device is supplied with the RESET pin active low.

The RESET polarity change is effective immediately. The written value can be verified by reading the Reset Polarity fuse bit.

**Table 8-3. Chip Reset Polarity Commands**

<table>
<thead>
<tr>
<th>Special Function Name</th>
<th>Description</th>
<th>Operation</th>
<th>Code Word</th>
<th>Data Word</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reset Active Low</td>
<td>Chip Reset is active low</td>
<td>Write</td>
<td>00 00 00 FF</td>
<td></td>
</tr>
<tr>
<td>Reset Active High</td>
<td>Chip Reset is active high</td>
<td>Write</td>
<td>00 00 FF FF</td>
<td></td>
</tr>
<tr>
<td>Chip Reset Status</td>
<td>Returns the state of the Reset Polarity fuse bit</td>
<td>Read</td>
<td>00 00 00 F2</td>
<td>XX [B2] XX XX B2 = 0XXX XXXX : RESET Active Low B2 = 1XXX XXXX : RESET Active High</td>
</tr>
</tbody>
</table>

### 8.5.3.3 Full Chip Erase

This command enables to erase the entire memory with a simple command. This command does not operate when the memory is write protected. The AT69170F does not acknowledge the TWI protocol during the memory erase cycle.

**Table 8-4. Full Chip Erase Command**

<table>
<thead>
<tr>
<th>Special Function Name</th>
<th>Description</th>
<th>Operation</th>
<th>Code Word</th>
<th>Data Word</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full Chip Erase</td>
<td>Erase the entire memory</td>
<td>Write</td>
<td>00 00 00 B0</td>
<td></td>
</tr>
</tbody>
</table>

### 9. FPGA Dump Mode

#### 9.1 Operating Mode overview

The I/O and logic functions of any SRAM-based FPGA device are configured with a bitstream supplied by an external memory device. The FPGA’s mode pins enable to select the way the bitstream is loaded into the FPGA. The bitstream can be supplied by a remote device or downloaded by the FPGA itself at power-on. In Master Serial Mode (Mode 0), the ATMEL’s AT40K FPGA serie automatically downloads the bitstream from an external memory device without the need of an external smart controller. The AT69170F has been designed to support the Master Serial Mode of AT40K FPGA serie.

#### 9.2 Single Device Configuration

The interface between FPGA and AT69170F device is composed of signals READY, RESET, CE, CLK and DATA.
When the power is up, the AT69170F’s internal address counter is reset and the READY pin is driven high, enabling the FPGA to leave its reset state and start the download process.

The RESET and CE pins of the AT69170F device control the tri-state buffer of the DATA output pin and the internal address counter. When the RESET pin is driven low, regardless to the level of the CE pin, the AT69170F resets its address counter and the DATA pin is set in tri-state mode.

If the CE pin is hold high when RESET pin is released (driven high), the address counter is disabled and the DATA output pin is set in tri-state mode.

If the CE pin is hold low when the RESET pin is released, the address counter and the DATA pin outputs the first data bit which is sampled by the FPGA on the first rising edge of the clock.

The AT69170F is clocked by the FPGA. The internal address counter is incremented on each clock’s period. The data bits are output by the AT69170F on the falling edges of the clock so that they can be sampled by the FPGA on the rising edges of the clock.

Once the bitstream’s download is complete, the CON pin is released by the FPGA.
An exemple of application schematic is provided on figure below.

The SER_EN pin enables to configure the AT69170F in TWI or DUMP mode. This pin is pulled up to Vcc to select the dump mode by default. A diode between READY and SER_EN enables to set automatically the FPGA in the reset state when the TWI mode is selected in order to avoid signal contentions.

Pull-up resistors are mandatory on DATA and CLK pins in TWI mode and on READY signal in DUMP mode.

It’s recommended to add an RC circuit between READY and RESETn signals in order to guaranty that the memory device is ready when the FPGA starts downloading.

---

**Figure 9-3.- Single Device Configuration Schematic**

---
9.3 Daisy Chain Configuration

The interface between FPGA and AT69170F devices is composed of signals READY, RESET, CE, CLK, DATA and CEO.

For multiple FPGAs configured in a daisy-chain, or for FPGAs requiring larger configuration memory, it is possible to cascade several AT69170F devices.

Once the last bit from the first AT69170F is read, the device drives its CEO pin low and disables its DATA pin to avoid signal contention with another AT69170F. The second AT69170F recognizes the Low level on its CE pin and enables its DATA pin. The same scenario repeats for the following AT69170F devices.

![Diagram of Daisy Chain Configuration](image-url)
An example of application schematic implementing four memory devices is provided on Figure 9-6 on page 28. In TWI mode, it is not possible to select more than two AT69170F devices at a time. Therefore, two chip selects CS1 and CS2 must be defined, each one selecting two devices, in order to program the all the devices two by two.

Pull-up resistors are mandatory on DATA and CLK pins in TWI mode and on READY signal in DUMP mode.

Figure 9-5.- Dump Mode (Daisy Chain Configuration)
Figure 9-6. Daisy Chain Configuration Schematic
10. Electrical Specifications

10.1 Absolute Maximum Ratings*

Supply voltage to ground .................. -0.5V to 4.6V
All input voltages (including NC pins) with respect to ground ................... <0.5V to +4.6V
All output voltages with respect to ground ............................................. <0.5V to VCC+ 0.5V
Storage temperature ..................... 65°C to +150°C
ESD Voltage (MIL STD 883D Method 3015.3) .............. > 4000V

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Exposure between recommended DC operating and absolute maximum rating conditions for extended periods may affect device reliability.

10.2 Recommended DC Operating Conditions

Table 10-1. Recommended DC Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc</td>
<td>Supply Voltage</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Temp</td>
<td>Operating Temperature (Case)</td>
<td>-55</td>
<td>25</td>
<td>125</td>
<td>°C</td>
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</table>

10.3 Capacitance

Table 10-2. Capacitance

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{IN}^{(1)}$</td>
<td>Input Capacitance</td>
<td>7</td>
<td>10</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{OUT}^{(1)}$</td>
<td>Output Capacitance</td>
<td>7</td>
<td>10</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: 1. Guaranteed but not tested
10.4 DC Characteristics

Table 10-3. DC Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IL}$, $I_{IH}$</td>
<td>Low Level Input Current</td>
<td>$V_{IN} = 0$ to $3.6$V $V_{CC} = 3.6$V</td>
<td>-1</td>
<td>1</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{CSL}$, $I_{CSH}$</td>
<td>Cold Sparing Leakage Current</td>
<td>$V_{IN} = 0$ to $3.6$V $V_{CC} = 0$V</td>
<td>-1</td>
<td>1</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{CSB}$</td>
<td>Static consumption in TWI mode</td>
<td>$SER_{EN} = 0$V $CE &gt;= VCC - 0.3$V $f_{CLK} = 0$ MHz $VCC = 3.6$V</td>
<td>15</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CCOP_READ}$</td>
<td>Read Operating Current</td>
<td>$f_{CLK} = 15$ MHz $I_{OUT} = 0$ mA</td>
<td>20</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{CCOP_WRITE}$</td>
<td>Write Operating Current</td>
<td>$f_{CLK} = 1/t_{WR}$</td>
<td>30</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>$V_{CC} = 3.0$V</td>
<td>GND - 0.3</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>$VCC = 3.6$V</td>
<td>2.2</td>
<td>VCC + 0.3</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage</td>
<td>$I_{OL} = 8$ mA $VCC = 3.0$ to $3.6$V</td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>$I_{OH} = -8$ mA $VCC = 3.0$ to $3.6$V</td>
<td></td>
<td>VCC - 0.4</td>
<td>V</td>
</tr>
</tbody>
</table>
10.5 AC Characteristics

Temperature Range: -55°C to +125°C
Supply Voltage: 3.3 ±0.3V
Input and Output Timing Reference Levels: 1.5V

10.5.1 Test Loads and Waveforms

![Output Test Load Diagram](image)

![Waveform Diagram](image)

Figure 10-1.- Output Test Load

Figure 10-2.- Waveform
### 10.5.2 TWI Mode Characteristics

![TWI Data Transfer Waveforms](image)

#### Table 10-4. TWI Data Transfer Timings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>$F_{CLOCK}$</td>
<td>Clock Frequency</td>
<td></td>
<td>400</td>
<td>KHz</td>
</tr>
<tr>
<td>$T_{LOW}$</td>
<td>Clock Low Pulse Width</td>
<td>1.2</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$T_{HIGH}$</td>
<td>Clock High Pulse Width</td>
<td>1.2</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$T_{AA}$</td>
<td>Clock Low to Data Out Valid</td>
<td>0.9</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$T_{BUF}$</td>
<td>Time the bus must be free before a new transmission can start</td>
<td>1.2</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$T_{HD-STA}$</td>
<td>Start Hold Time from CLOCK</td>
<td>0.6</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$T_{SU-STA}$</td>
<td>Start Setup Time from CLOCK</td>
<td>0.6</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$T_{HD-DAT}$</td>
<td>Data In Hold Time</td>
<td>0.1</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$T_{SU-DAT}$</td>
<td>Data In Setup Time</td>
<td>0.1</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$T_{R}$</td>
<td>Inputs Rise Time</td>
<td>0.3</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$T_{F}$</td>
<td>Inputs Fall Time</td>
<td>0.3</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$T_{SU-STO}$</td>
<td>Stop Setup Time</td>
<td>0.6</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>$T_{DH}$</td>
<td>Data Out Hold Time</td>
<td>0</td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>
### 10.5.3 Dump Mode Characteristics

![Diagram of Dump Mode Waveforms](image-url)

**Figure 10-5.- Dump Mode Waveforms**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
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<tr>
<td>tWR</td>
<td>Write Cycle Time</td>
<td>34</td>
<td>68</td>
<td>ms</td>
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**Table 10-5. Write Cycle Time**
Figure 10-6. Cascade Mode Waveforms

Table 10-6. Dump Mode Timings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>T_{OE}</td>
<td>Data Output Delay from RESET</td>
<td>35</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>T_{CE}</td>
<td>Data Output Delay from CE</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>T_{CAC}</td>
<td>Data Output Delay from CLK</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>T_{OH}</td>
<td>Data Hold from CE, RESET, or CLK</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>T_{DF}</td>
<td>Data Float Output Delay from CE or RESET</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>T_{CDF}</td>
<td>Data Float Output Delay from CLK</td>
<td>30</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>T_{CKE}</td>
<td>CEO Output Delay from CLK</td>
<td>35</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>T_{CKE}</td>
<td>CEO Output Delay from CE</td>
<td>25</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>T_{OE}</td>
<td>CEO Output Delay from RESET</td>
<td>25</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>T_{LC}</td>
<td>CLK Low Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>T_{HC}</td>
<td>CLK High Time</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>T_{SCE}</td>
<td>CE Setup Time to CLK (to guarantee proper counting)</td>
<td>20</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>T_{HCE}</td>
<td>CE Hold Time from CLK (to guarantee proper counting)</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>T_{HOE}</td>
<td>RESET pulse width that guarantees the counter is reset</td>
<td>60</td>
<td></td>
<td>ns</td>
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<tr>
<td>F_{MAX}</td>
<td>Maximum Clock Frequency</td>
<td>15</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>T_{RDY}</td>
<td>RESET hold Delay after READY</td>
<td>0</td>
<td></td>
<td>ns</td>
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11. Ordering Information

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<td>Engineering Samples</td>
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<td>AT69170F-DT-MQ(^{(1)}(2))</td>
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Note:  
1. Contact Atmel for availability  
2. Will be replaced by SMD part number when available
12. Packaging Information

Note: The package lid is connected to GND

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<th>Max</th>
<th>Min</th>
<th>Max</th>
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<td>A</td>
<td>1.14</td>
<td>2.92</td>
<td>.045</td>
<td>.115</td>
</tr>
<tr>
<td>b</td>
<td>0.38</td>
<td>0.48</td>
<td>.015</td>
<td>.019</td>
</tr>
<tr>
<td>c</td>
<td>0.08</td>
<td>0.15</td>
<td>.003</td>
<td>.006</td>
</tr>
<tr>
<td>D</td>
<td>---</td>
<td>12.45</td>
<td>---</td>
<td>.490</td>
</tr>
<tr>
<td>E</td>
<td>6.22</td>
<td>8.00</td>
<td>.245</td>
<td>.315</td>
</tr>
<tr>
<td>E2</td>
<td>3.30</td>
<td>---</td>
<td>.130</td>
<td>---</td>
</tr>
<tr>
<td>E3</td>
<td>0.76</td>
<td>---</td>
<td>.030</td>
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<td>k</td>
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<td>0.39</td>
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<td>0.63</td>
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<td>.025</td>
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<td>e</td>
<td>1.27</td>
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<td>L</td>
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<td>S</td>
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<td>1.14</td>
<td>---</td>
<td>.045</td>
</tr>
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<td>S1</td>
<td>0.13</td>
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<tr>
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Note: The package lid is connected to GND
### 13. Revision History

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<td>- Update: Section 1, “Features” on page 1</td>
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<td>- Update: Section 1., “Description” on page 3</td>
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<td>- Update: Section 8.5.3.1, “Data Protection” on page 22</td>
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<td>- Update: $T_{HOE}$ parameter in Table 10-6, “Dump Mode Timings,” on page 34</td>
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<td>- Change: document footers renaming to be in compliance with new corporate specifications</td>
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