The ATtiny212/214/412/414 Automotive devices you have received conform functionally to the current device data sheet (www.microchip.com/DS40002229), except for the anomalies described in this document. The erratas described in this document will likely be addressed in future revisions of the ATtiny212/214/412/414 Automotive devices.

Notes:
- This document summarizes all the silicon errata issues from all revisions of silicon, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002229) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance
1. **Silicon Issue Summary**

**Legend**
- Erratum is not applicable.
- X Erratum is applicable.
- * This silicon revision was never released to production.

<table>
<thead>
<tr>
<th>Peripheral</th>
<th>Short Description</th>
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</tr>
</tbody>
</table>
2. Silicon Errata Issues

2.1 Errata Details
- Erratum is not applicable.
X Erratum is applicable.
* This silicon revision was never released to production.

2.2 Device

2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to ‘1’ Prevents Automatic Loading of Calibration Values
Writing the OSCLOCK fuse in FUSE.OSCCFG to ‘1’ prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

Work around
Do not use OSCLOCK for locking the oscillator calibration value. The oscillator calibration value can be locked by writing LOCK in CLKCTRL.OSC20MCALIBB to ‘1’.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>Rev. A</th>
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2.2.2 The Temperature Sensor is Not Calibrated on Parts with Date Code 727, 728 and 1728 (Year 2017, Week 27/28)
The temperature sensor is not calibrated on parts with date code 727/728 (used on QFN packages) and 1728 (used on SOIC packages).

Work around
If temperature sensor calibration data is required, devices with the affected date code may be returned through the Microchip RMA service. Devices with this date code are no longer shipped by Microchip.

Affected Silicon Revisions

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2.3 ADC - Analog-to-Digital Converter

2.3.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode
The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work around
Write ADCn.CTRLA.ENABLE to ‘0’ to stop the Free-Running mode immediately.
2.3.2 ADC Functionality Cannot be Ensured with $\text{CLK}_{\text{ADC}}$ Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if $\text{CLK}_{\text{ADC}} > 1.5$ MHz with $\text{ADCn.CALIB.DUTYCYC}$ set to ‘1’.

**Work around**

If ADC is operated with $\text{CLK}_{\text{ADC}} > 1.5$ MHz, $\text{ADCn.CALIB.DUTYCYC}$ must be set to ‘0’ (50% duty cycle).

### Affected Silicon Revisions

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</table>

2.4 CCL - Configurable Custom Logic

2.4.1 Connecting LUTs in Linked Mode Requires OUTEN Set to ‘1’

Connecting the LUTs in linked mode requires $\text{LUTnCTRLA.OUTEN}$ set to ‘1’ for the LUT providing the input source.

**Work around**

Use an event channel to link the LUTs or do not use the corresponding I/O pin for other purposes.

### Affected Silicon Revisions

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<thead>
<tr>
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2.4.2 D-latch is Not Functional

The CCL D-latch is not functional.

**Work around**

None.

### Affected Silicon Revisions

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2.5 PORTMUX - Port Multiplexer

2.5.1 Selecting Alternative Output Pin for TCA0 Waveform Output 0-2 also Changes Waveform Output 3-5

Selecting the alternative output pin for TCA0 in $\text{PORTMUX.CTRLC}$ does not work as described when TCA0 operates in split mode.

- Writing $\text{PORTMUX.CTRLC}$ bit 0 to ‘1’ will shift the pin position for both WO0 and WO3
• Writing PORTMUX.CTRLC bit 1 to ‘1’ will shift the pin position for both WO1 and WO4
• Writing PORTMUX.CTRLC bit 2 to ‘1’ will shift the pin position for both WO2 and WO5

PORTMUX.CTRLC[5:3] are non-functional.

Work around
None.

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Note: Not applicable to 8-pin devices.

2.6 RTC - Real-Time Counter

2.6.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler
Any write to the RTC.CTRLA register resets the RTC and PIT prescaler.

Work around
None.

Affected Silicon Revisions

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2.6.2 Disabling the RTC Stops the PIT
Writing RTC.CTRLA.RTCEN to ‘0’ will stop the PIT.
Writing RTC.PITCTRLA.PITEN to ‘0’ will stop the RTC.

Work around
Do not disable the RTC or the PIT if any of the modules are used.

Affected Silicon Revisions

<table>
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<tr>
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2.7 TCB - Timer/Counter B

2.7.1 Minimum Event Duration Must Exceed the Selected Clock Period
Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) Time-Out Check and Input Capture Frequency and Pulse-Width Measurement mode.

Work around
Ensure that the high/low period of input events is equal to or longer than the period of the selected clock source (CLKSEL in TCBn.CTRLA).
### 2.7.2 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force a restart of the TCB when TCB is running in SYNCUPD mode. TCB is only restarted after a TCA OVF.

**Work around**

None.

### 2.8 USART - Universal Synchronous and Asynchronous Receiver and Transmitter

#### 2.8.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:
- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to ‘0’ while the USART receiver is disabled (RXEN in USART.CTRLB is ‘0’)
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to ‘0’

**Work around**

There are two possible workarounds:
- Make sure the receiver is enabled (RXEN in USART.CTRLB is ‘1’) while disabling the transmitter (writing TXEN in USART.CTRLB to ‘0’)
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

### 2.8.2 Full Range Duty Cycle Not Supported When Validating LIN Sync Field

For the LIN sync field, the USART is validating each bit to be within ±15% instead of the time between falling edges as described in the LIN specification. This allows a minimum duty cycle of 43.5% and a maximum duty cycle of 57.5%.

**Work around**

None.
2.8.3 Frame Error on a Previous Message May Cause False Start Bit Detection
A false start bit detection will trigger if receiving a frame with RXDATAH.FERR set and reading the RXDATAL before the RxD line goes high.

Work around
Wait for the RXD pin to go high before reading RXDATA, for instance, by polling the bit in PORTn.IN where the RXD pin is located.

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2.8.4 Open-Drain Mode Does Not Work When TXD is Configured as Output
When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work around
Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to ‘0’ when using Open-Drain mode.

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3. **Data Sheet Clarifications**
   The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (www.microchip.com/DS40002229).

   **Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

3.1 **None**
There are no known data sheet clarifications as of this publication date.
4. Document Revision History

Note: The data sheet clarification document revision is independent of the die revision and the device variant (last letter of the ordering number).

4.1 Revision History

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<tr>
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<tr>
<td>A</td>
<td>05/2020</td>
<td>Initial document release</td>
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