Description

The ATWILC1000-MR110xB module is a low-power consumption IEEE 802.11 b/g/n IoT (Internet of Things) module, which is specifically optimized for low-power IoT applications. The ATWILC1000-MR110xB modules feature small form factor (21.7mm x 14.7mm x 2.1mm) while fully integrating Power Amplifier (PA), Low Noise Amplifier (LNA), Transmit/Receive (T/R), switch, and power management. The ATWILC1000-MR110PB includes a PCB antenna while the ATWILC1000-MR110UB module includes a u.FL connector to use with an external antenna. With advanced security, it is interoperable with various vendors using IEEE 802.11b/g/n Access Points in wireless LAN. The module provides Serial Peripheral Interface (SPI) and Secure Digital Input Output (SDIO) to interface with the host controller.

Note that all references to the ATWILC1000-MR110xB module include all the module devices listed below unless otherwise noted:

- ATWILC1000-MR110PB
- ATWILC1000-MR110UB

Features

- Compliant with IEEE 802.11 b/g/n 20 MHz (1x1) Solution
- Supports Single Spatial Stream in 2.4 GHz ISM Band
- Integrated Power Amplifier (PA) and Transmit/Receive (T/R) Switch
- Superior Sensitivity and Range through Advanced PHY Signal Processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization
- Wi-Fi Direct® and Soft-AP Support
- Supports IEEE 802.11 WEP, WPA, WPA2 and WPA2-Enterprise Security
- Superior Medium Access Control (MAC) Throughput through Hardware Accelerated Two-Level A-MSDU/A-MPDU Frame Aggregation and Block Acknowledgement
- On-Chip Memory Management Engine to Reduce the Host Load
- SPI and SDIO Host Interfaces
- Operating Temperature Ranges from -40°C to +85°C
- Input/Output Operating Voltage of 2.7V to 3.6V
- Built-In 26 MHz Crystal
- Power-Save Modes:
  - <1µA Power-Down mode typical at 3.3V I/O
  - 380µA Doze mode with chip settings preserved (used for beacon monitoring)
  - On-chip low-power Sleep oscillator
  - Fast host wake-up from Doze mode by a pin or the host I/O transaction
• Wi-Fi Alliance® certified for connectivity and optimizations
  – ID: WFA65340
# Table of Contents

Description ....................................................................................................................... 1

Features .......................................................................................................................... 1

1. Ordering Information and Module Marking............................................................... 5

2. Functional Overview .............................................................................................. 6

3. Pinout and Package Information ............................................................................ 7

4. Electrical Specifications ........................................................................................ 11
   4.1. Absolute Ratings ............................................................................................... 11
   4.2. Recommended Operating Conditions ............................................................... 11
   4.3. Receiver Performance ..................................................................................... 11
   4.4. Transmitter Performance ................................................................................. 13
   4.5. Timing Characteristics ...................................................................................... 14

5. Power Management ................................................................................................ 19
   5.1. Current Consumption in Various Device States .................................................. 19
   5.2. Restrictions for Power States ............................................................................ 20
   5.3. Power-Up/Down Sequence .............................................................................. 20
   5.4. Digital I/O Pin Behavior During Power-Up Sequences ....................................... 21

6. CPU and Memory Subsystems .............................................................................. 22
   6.1. Processor ......................................................................................................... 22
   6.2. Memory Subsystem ........................................................................................ 22
   6.3. Nonvolatile Memory (eFuse) ........................................................................... 22

7. WLAN Subsystem .................................................................................................. 24
   7.1. MAC ................................................................................................................ 24
   7.2. PHY ............................................................................................................... 25
   7.3. Radio .............................................................................................................. 26

8. External Interfaces ................................................................................................... 27
   8.1. Interfacing with the Host Microcontroller ......................................................... 27
   8.2. SPI Slave Interface ........................................................................................ 28
   8.3. SDIO Slave Interface ...................................................................................... 29
   8.4. UART Debug Interface .................................................................................. 30
   8.5. I²C Slave Interface ......................................................................................... 31

9. Notes on Interfacing with the ATWILC1000-MR110xB .......................................... 32

10. Application Reference Design ............................................................................. 33

11. Module Outline Drawings .................................................................................... 35

12. Design Consideration .......................................................................................... 38
12.1. ATWILC1000-MR110PB Placement and Routing Guidelines .................................................... 38
12.2. Printed PCB Antenna Performance of ATWILC1000-MR110PB ................................................ 39
12.3. ATWILC1000-MR110UB Placement and Routing Guidelines .................................................... 42

13. Reflow Profile Information ........................................................................................................ 44
   13.1. Storage Condition .............................................................................................................. 44
   13.2. Baking Conditions ............................................................................................................. 44
   13.3. Reflow Oven ..................................................................................................................... 44

14. Module Assembly Considerations ......................................................................................... 45

15. Regulatory Approval ................................................................................................................. 46
   15.1. United States ...................................................................................................................... 46
   15.2. Canada ............................................................................................................................. 49
   15.3. Europe ............................................................................................................................. 50
   15.4. Japan ............................................................................................................................... 53
   15.5. Korea .............................................................................................................................. 53
   15.6. Taiwan ............................................................................................................................ 54
   15.7. China ............................................................................................................................... 55
   15.8. Other Regulatory Information .......................................................................................... 55

16. Reference Documentation ........................................................................................................ 56

17. Document Revision History .................................................................................................... 57

The Microchip Web Site ................................................................................................................. 59

Customer Change Notification Service ....................................................................................... 59

Customer Support ....................................................................................................................... 59

Microchip Devices Code Protection Feature ............................................................................... 59

Legal Notice .................................................................................................................................. 60

Trademarks .................................................................................................................................... 60

Quality Management System Certified by DNV .......................................................................... 61

Worldwide Sales and Service ....................................................................................................... 62
1. Ordering Information and Module Marking

The following table provides the ordering information of the ATWILC1000-MR110xB module.

Table 1-1. Ordering Information

<table>
<thead>
<tr>
<th>Model Number</th>
<th>Ordering Code</th>
<th>Package</th>
<th>No. of Pins</th>
<th>Description</th>
<th>Regulatory Certification</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATWILC1000-MR110PB</td>
<td>ATWILC1000-MR110PB</td>
<td>21.7x14.7x2.1 mm</td>
<td>28</td>
<td>Certified module with ATWILC1000B-MU chip and PCB antenna</td>
<td>FCC, ISED, CE, MIC, KCC, NCC, SRRC</td>
</tr>
<tr>
<td>ATWILC1000-MR110UB</td>
<td>ATWILC1000-MR110UB</td>
<td>21.7x14.7x2.1 mm</td>
<td>28</td>
<td>Certified module with ATWILC1000B-MU chip and uFL connector</td>
<td>FCC, ISED, CE</td>
</tr>
</tbody>
</table>

The following figure provides the marking information of the ATWILC1000-MR110xB module.

Figure 1-1. Marking Information

![Marking Information Diagram]
2. Functional Overview

The ATWILC1000-MR110xB module block diagram is shown in the following figure.

Figure 2-1. ATWILC1000-MR110xB Module Block Diagram
3. Pinout and Package Information

The ATWILC1000-MR110xB package has an exposed paddle that must be connected to the system board ground. The module pin assignment is shown in the following figure.

**Figure 3-1. Pin Assignment**

![Pin Assignment Diagram]

**Note:** This pin assignment is applicable for both ATWILC1000-MR110PB and ATWILC1000-MR110UB modules.

The following table describes the pin description of this module.

**Table 3-1. Pin Details**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
<th>Programmable Pull up Resistor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GPIO_6(^1)</td>
<td>I/O</td>
<td>General purpose I/O.</td>
<td>-</td>
</tr>
<tr>
<td>Pin No.</td>
<td>Name</td>
<td>Type</td>
<td>Description</td>
<td>Programmable Pull up Resistor</td>
</tr>
<tr>
<td>--------</td>
<td>---------------</td>
<td>------</td>
<td>-----------------------------------------------------------------------------</td>
<td>------------------------------</td>
</tr>
<tr>
<td>2</td>
<td>I²C_SCL</td>
<td>I/O</td>
<td>I²C slave clock. Used only for development debug purposes. It is recommended to add test point for this pin.</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>I²C_SDA</td>
<td>I/O</td>
<td>I²C slave data. Used only for development debug purposes. It is recommended to add test point for this pin.</td>
<td>Yes</td>
</tr>
<tr>
<td>4</td>
<td>RESET_N</td>
<td>I</td>
<td>Active-low hard reset. When this pin is asserted low, the module is placed in the Reset state. When this pin is asserted high, the module is out of reset and functions normally. Connect to a host output that defaults low at power-up. If the host output is tri-stated, add a 1 MΩ pull-down resistor to ensure a low level at power-up.</td>
<td>Yes</td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td>–</td>
<td>No connection</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>NC</td>
<td>–</td>
<td>No connection</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td>–</td>
<td>No connection</td>
<td>-</td>
</tr>
<tr>
<td>8</td>
<td>NC</td>
<td>–</td>
<td>No connection</td>
<td>-</td>
</tr>
<tr>
<td>9</td>
<td>GND_1</td>
<td>Ground</td>
<td>Ground</td>
<td>-</td>
</tr>
<tr>
<td>10</td>
<td>SDIO_SPI_CFG</td>
<td>I</td>
<td>Connect to VDDIO through a 1MΩ resistor to enable the SPI interface. Connect to ground to enable SDIO interface.</td>
<td>No</td>
</tr>
<tr>
<td>11</td>
<td>WAKE</td>
<td>I</td>
<td>Host wake control.</td>
<td>Yes</td>
</tr>
<tr>
<td>12</td>
<td>GND_2</td>
<td>Ground</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>13</td>
<td>IRQN</td>
<td>O</td>
<td>The ATWILC1000-MR110xB device interrupt output. Connect to a host interrupt pin.</td>
<td>Yes</td>
</tr>
<tr>
<td>14</td>
<td>SD_DAT3</td>
<td>SDIO=I/O UART=O</td>
<td>SDIO Data Line 3 from the ATWILC1000-MR110xB when module is configured for SDIO.</td>
<td>Yes</td>
</tr>
<tr>
<td>15</td>
<td>SD_DAT2/SPI_RXD</td>
<td>SDIO=I/O SPI=I</td>
<td>SDIO Data Line 2 signal from ATWILC1000-MR110xB when module is configured for SDIO. SPI MOSI (Master Out Slave In) pin when module is configured for SPI.</td>
<td>Yes</td>
</tr>
</tbody>
</table>
## ATWILC1000-MR110xB
### Pinout and Package Information

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
<th>Programmable Pull up Resistor</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>SD_DAT1/ SPI_SSN</td>
<td>SDIO=I/O, SPI=I</td>
<td>SDIO Data Line 1 from ATWILC1000-MR110xB when module is configured for SDIO. Active low SPI slave select from the ATWILC1000 when module is configured for SPI.</td>
<td>Yes</td>
</tr>
<tr>
<td>17</td>
<td>SD_DAT0/ SPI_TXD</td>
<td>SDIO=I/O, SPI=O</td>
<td>SDIO Data Line 0 from the ATWILC1000-MR110xB when module is configured for SDIO. SPI MISO (Master In Slave Out) pin from ATWILC1000 when module is configured for SPI.</td>
<td>Yes</td>
</tr>
<tr>
<td>18</td>
<td>SD_CMD/ SPI_CLK</td>
<td>SDIO=I/O, SPI=I</td>
<td>SDIO CMD line from ATWILC1000-MR110xB when module is configured for SDIO. SPI Clock from ATWILC1000 when module is configured for SPI.</td>
<td>Yes</td>
</tr>
<tr>
<td>19</td>
<td>SD_CLK</td>
<td>SDIO=I, UART=I</td>
<td>SDIO clock line for the ATWILC1000-MR110xB when module is configured for SDIO.</td>
<td>Yes</td>
</tr>
<tr>
<td>20</td>
<td>VBATT</td>
<td>Power supply</td>
<td>Power supply pin for the DC/DC convertor.</td>
<td>Yes</td>
</tr>
<tr>
<td>21</td>
<td>GPIO_1(^1)</td>
<td>I/O</td>
<td>General purpose I/O</td>
<td>Yes</td>
</tr>
<tr>
<td>22</td>
<td>CHIP_EN</td>
<td>I</td>
<td>Module enable. High level enables module, low level places module in Power-Down mode. Connect to a host Output that defaults low at power-up. If the host output is tri-stated, add a 1MΩ pull-down resistor if necessary to ensure a low level at power-up.</td>
<td>No</td>
</tr>
<tr>
<td>23</td>
<td>VDDIO</td>
<td>Power supply</td>
<td>I/O power supply. Must match host I/O voltage.</td>
<td>-</td>
</tr>
<tr>
<td>24</td>
<td>1P3V_TP</td>
<td>-</td>
<td>1.3V VDD Core Test Point. Decouple with 10 uF and 0.01 uF to GND close to pin 24.</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>GPIO_3(^1)</td>
<td>I/O</td>
<td>General purpose I/O. By default, UART receive input to ATWILC1000-MR110xB. Used only for development debug purposes. It is recommended to add test point for this pin.</td>
<td>Yes</td>
</tr>
<tr>
<td>26</td>
<td>GPIO_4(^1)</td>
<td>I/O</td>
<td>General purpose I/O.</td>
<td>Yes</td>
</tr>
<tr>
<td>Pin No.</td>
<td>Name</td>
<td>Type</td>
<td>Description</td>
<td>Programmable Pull up Resistor</td>
</tr>
<tr>
<td>--------</td>
<td>------------</td>
<td>------</td>
<td>-----------------------------------------------------------------------------</td>
<td>-------------------------------</td>
</tr>
<tr>
<td>27</td>
<td>GPIO_5(^1)</td>
<td>I/O</td>
<td>General purpose I/O. By default, UART transmit output from ATWILC1000-MR110xB. Used only for development debug purposes. It is recommended to add test point for this pin.</td>
<td>Yes</td>
</tr>
<tr>
<td>28</td>
<td>GND_3</td>
<td>Ground</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>29</td>
<td>Paddle</td>
<td>Ground</td>
<td>Exposed paddle GND. This pad must be soldered to system ground</td>
<td>-</td>
</tr>
</tbody>
</table>

**Note:** Usage of the GPIO functionality is not supported by the WILC1000 FW. The datasheet will be updated once the support for this feature is added.

The following table provides the ATWILC1000-MR110xB module package dimensions.

**Table 3-2. ATWILC1000-MR110xB Module Package Information**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package Size</td>
<td>21.7 x 14.7 x 2.1</td>
<td>mm</td>
</tr>
<tr>
<td>Pad Count</td>
<td>28</td>
<td>-</td>
</tr>
<tr>
<td>Total Thickness</td>
<td>2.11</td>
<td>mm</td>
</tr>
<tr>
<td>Pad Pitch</td>
<td>1.016</td>
<td></td>
</tr>
<tr>
<td>Pad Width</td>
<td>0.82</td>
<td></td>
</tr>
<tr>
<td>Exposed Pad size</td>
<td>3.7 x 3.7</td>
<td></td>
</tr>
</tbody>
</table>
4. Electrical Specifications

4.1 Absolute Ratings
The absolute maximum ratings for this module are listed in the following table.

Table 4-1. ATWILC1000-MR110xB Module Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBATT</td>
<td>Input supply voltage</td>
<td>-0.3</td>
<td>5.0</td>
<td>V</td>
</tr>
<tr>
<td>VDDIO</td>
<td>I/O voltage</td>
<td>-0.3</td>
<td>5.0</td>
<td>V</td>
</tr>
</tbody>
</table>

⚠️ CAUTION ⚠️ Stresses beyond those listed under "Absolute Maximum Ratings" cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods affects the device reliability.

4.2 Recommended Operating Conditions
The recommended operating conditions for this module are listed in the following table.

Table 4-2. ATWILC1000-MR110xB Module Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBATT</td>
<td>3.0</td>
<td>3.3</td>
<td>4.2</td>
<td>V</td>
</tr>
<tr>
<td>VDDIO</td>
<td>2.7</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>Operating</td>
<td>-40</td>
<td>+85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note:
1. VBATT should be equal to or greater than VDDIO.
2. The voltage of VDDIO is dependent on system I/O voltage.
3. Test Conditions: -40°C to +85°C

4.3 Receiver Performance
The following are typical conditions for radio receiver performance:

VBATT at 3.3V; VDDIO at 3.3V; temperature at 25°C and WLAN Channel 6 (2437 MHz).

The following table provides the receiver performance characteristics for the module.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>-</td>
<td>2,412</td>
<td>-</td>
<td>2,472</td>
<td>MHz</td>
</tr>
<tr>
<td>Sensitivity 802.11b</td>
<td>1 Mbps DSSS</td>
<td>-</td>
<td>-94</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>2 Mbps DSSS</td>
<td>-</td>
<td>-91</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>5.5 Mbps DSSS</td>
<td>-</td>
<td>-89</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>11 Mbps DSSS</td>
<td>-</td>
<td>-86</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td>Sensitivity 802.11g</td>
<td>6 Mbps OFDM</td>
<td>-</td>
<td>-88</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>9 Mbps OFDM</td>
<td>-</td>
<td>-87</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>12 Mbps OFDM</td>
<td>-</td>
<td>-86</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>18 Mbps OFDM</td>
<td>-</td>
<td>-84</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>24 Mbps OFDM</td>
<td>-</td>
<td>-82</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>36 Mbps OFDM</td>
<td>-</td>
<td>-78</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>48 Mbps OFDM</td>
<td>-</td>
<td>-74</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>54 Mbps OFDM</td>
<td>-</td>
<td>-73</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td>Sensitivity 802.11n (BW at 20 MHz)</td>
<td>MCS 0</td>
<td>-</td>
<td>-87</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>MCS 1</td>
<td>-</td>
<td>-85</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>MCS 2</td>
<td>-</td>
<td>-83</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>MCS 3</td>
<td>-</td>
<td>-80</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>MCS 4</td>
<td>-</td>
<td>-76</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>MCS 5</td>
<td>-</td>
<td>-73</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>MCS 6</td>
<td>-</td>
<td>-71</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>MCS 7</td>
<td>-</td>
<td>-69</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td>Maximum Receive Signal Level</td>
<td>1-11 Mbps DSSS</td>
<td>-</td>
<td>0</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>6-54 Mbps OFDM</td>
<td>-</td>
<td>-5</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>MCS 0 – 7</td>
<td>-</td>
<td>-5</td>
<td>-</td>
<td>dBm</td>
</tr>
<tr>
<td>Adjacent Channel Rejection</td>
<td>1 Mbps DSSS (30 MHz offset)</td>
<td>-</td>
<td>50</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>11 Mbps DSSS (25 MHz offset)</td>
<td>-</td>
<td>43</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>6 Mbps OFDM (25 MHz offset)</td>
<td>-</td>
<td>40</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>54 Mbps OFDM (25 MHz offset)</td>
<td>-</td>
<td>25</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>MCS 0 – 20 MHz BW (25 MHz offset)</td>
<td>-</td>
<td>40</td>
<td>-</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>MCS 7 – 20 MHz BW (25 MHz offset)</td>
<td>-</td>
<td>20</td>
<td>-</td>
<td>dB</td>
</tr>
</tbody>
</table>
### Cellular Blocker Immunity

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>776-794 MHz CDMA</td>
<td>-</td>
<td>-14</td>
<td>-14</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>824-849 MHz GSM</td>
<td>-</td>
<td>-10</td>
<td>-10</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>880-915 MHz GSM</td>
<td>-</td>
<td>-10</td>
<td>-10</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>1710-1785 MHz GSM</td>
<td>-</td>
<td>-15</td>
<td>-15</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>1850-1910 MHz GSM</td>
<td>-</td>
<td>-15</td>
<td>-15</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>1850-1910 MHz WCDMA</td>
<td>-</td>
<td>-24</td>
<td>-24</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>1920-1980 MHz WCDMA</td>
<td>-</td>
<td>-24</td>
<td>-24</td>
<td></td>
<td>dBm</td>
</tr>
</tbody>
</table>

### Transmitter Performance

The following are typical conditions for radio transmitter performance:

- VBAT at 3.3 V; VDDIO at 3.3V; temperature at 25°C and WLAN Channel 6 (2437 MHz).

The following table provides the transmitter performance characteristics for the module.

**Table 4-4. Transmitter Performance**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Unit</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>-</td>
<td>MHz</td>
<td>2,412</td>
<td>-</td>
<td>2,472</td>
</tr>
<tr>
<td>Output Power1-2, ON_Transmit</td>
<td>802.11b 1Mbps</td>
<td>dBm</td>
<td>-</td>
<td>17.6</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>802.11b 11Mbps</td>
<td>dBm</td>
<td>-</td>
<td>18.2</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>802.11g 6Mbps</td>
<td>dBm</td>
<td>-</td>
<td>18.7</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>802.11g 54Mbps</td>
<td>dBm</td>
<td>-</td>
<td>16.7</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>802.11n MCS 0</td>
<td>dBm</td>
<td>-</td>
<td>17.3</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>802.11n MCS 7</td>
<td>dBm</td>
<td>-</td>
<td>13.8</td>
<td>-</td>
</tr>
<tr>
<td>Tx Power Accuracy</td>
<td>-</td>
<td>dB</td>
<td>-</td>
<td>±1.5²</td>
<td>-</td>
</tr>
<tr>
<td>Carrier Suppression</td>
<td>802.11b mode</td>
<td>dBc</td>
<td>-</td>
<td>-19.4</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>802.11g mode</td>
<td>dBc</td>
<td>-</td>
<td>-27.5</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>802.11n mode</td>
<td>dBc</td>
<td>-</td>
<td>-21.1</td>
<td>-</td>
</tr>
</tbody>
</table>
### Electrical Specifications

#### Parameter |
<table>
<thead>
<tr>
<th>Description</th>
<th>Unit</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Out of Band Transmit Power</td>
<td>76-108 dBm/Hz</td>
<td>-</td>
<td>-125</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>776-794 dBm/Hz</td>
<td>-</td>
<td>-125</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>869-960 dBm/Hz</td>
<td>-</td>
<td>-125</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>925-960 dBm/Hz</td>
<td>-</td>
<td>-125</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>1570-1580 dBm/Hz</td>
<td>-</td>
<td>-125</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>1805-1880 dBm/Hz</td>
<td>-</td>
<td>-125</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>1930-1990 dBm/Hz</td>
<td>-</td>
<td>-125</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>2110-2170 dBm/Hz</td>
<td>-</td>
<td>-125</td>
<td>-</td>
</tr>
<tr>
<td>Harmonic Output Power&lt;sup&gt;4&lt;/sup&gt;</td>
<td>2&lt;sup&gt;nd&lt;/sup&gt; dBm/MHz</td>
<td>-</td>
<td>-28</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>3&lt;sup&gt;rd&lt;/sup&gt; dBm/MHz</td>
<td>-</td>
<td>-33</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>4&lt;sup&gt;th&lt;/sup&gt; dBm/MHz</td>
<td>-</td>
<td>-40</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>5&lt;sup&gt;th&lt;/sup&gt; dBm/MHz</td>
<td>-</td>
<td>-28</td>
<td>-</td>
</tr>
</tbody>
</table>

#### Note:
1. Measured at 802.11 spec compliant EVM/Spectral Mask.
2. Measured at RF balun output.
3. Operating temperature range is -40°C to +85°C. RF performance is assured at room temperature of 25°C with a 2-3dB change at boundary conditions.
4. Measured at 11Mbps, DG(Digital Gain)= -7, WLAN Channel 6 (2437 MHz).
5. With respect to TX power, different (higher/lower) RF output power settings may be used for specific antennas and/or enclosures, in which case recertification may be required.
6. The availability of some specific channels and/or operational frequency bands are country dependent and should be programmed at the Host product factory to match the intended destination. Regulatory bodies prohibit exposing the settings to the end user. This requirement needs to be taken care of via host implementation.
7. The RF parameters for the ATWILC1000-MR110UB will be approximately 1 dB less than the values in the table. This insertion loss accounts for PCB trace losses, and the filter network loss to the u.FL connector.

### 4.5 Timing Characteristics

#### 4.5.1 SPI Timing

The SPI timing is shown in the following figure.
Figure 4-1. SPI Timing Diagram (SPI MODE CPOL=0, CPHA=0)

The SPI timing parameters are provided in the following table.

Table 4-5. SPI Slave Timing Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Input Frequency²</td>
<td>$f_{\text{SCK}}$</td>
<td>-</td>
<td>48</td>
<td>MHz</td>
</tr>
<tr>
<td>Clock Low Pulse Width</td>
<td>$t_{\text{WL}}$</td>
<td>4</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Clock High Pulse Width</td>
<td>$t_{\text{WH}}$</td>
<td>5</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Clock Rise Time</td>
<td>$t_{\text{LH}}$</td>
<td>0</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>Clock Fall Time</td>
<td>$t_{\text{HL}}$</td>
<td>0</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>TXD Output Delay³</td>
<td>$t_{\text{ODLY}}$</td>
<td>4</td>
<td>9 from SCK fall 12.5 from SCK rise</td>
<td>ns</td>
</tr>
<tr>
<td>RXD Input Setup Time</td>
<td>$t_{\text{ISU}}$</td>
<td>1</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>RXD Input Hold Time</td>
<td>$t_{\text{IHD}}$</td>
<td>5</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>SSN Input Setup Time</td>
<td>$t_{\text{SUSSN}}$</td>
<td>3</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>SSN Input Hold Time</td>
<td>$t_{\text{HDSSN}}$</td>
<td>5.5</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>
Note:
1. Timing is applicable to all SPI modes.
2. Maximum clock frequency specified is limited by the SPI slave interface internal design; actual maximum clock frequency can be lower and depends on the specific PCB layout.
3. Timing is based on 15pF output loading.

4.5.2 SDIO Timing
The SDIO Slave interface timing is shown in following figure.

Figure 4-2. SDIO Timing Diagram

Slave timing parameters are provided in the following table.

Table 4-6. SDIO Timing Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Input Frequency¹</td>
<td>f_PP</td>
<td>0</td>
<td>50</td>
<td>MHz</td>
</tr>
<tr>
<td>Clock Low Pulse Width</td>
<td>tWL</td>
<td>9</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Clock High Pulse Width</td>
<td>tWH</td>
<td>4.5</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Clock Rise Time</td>
<td>t_LH</td>
<td>0</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Clock Fall Time</td>
<td>t_HL</td>
<td>0</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>Input Setup Time</td>
<td>t_ISU</td>
<td>6</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Input Hold Time</td>
<td>t_IH</td>
<td>4</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>Output Delay²</td>
<td>t_ODLY</td>
<td>3</td>
<td>11</td>
<td></td>
</tr>
</tbody>
</table>

¹ Maximum clock frequency specified is limited by the SDIO Slave interface internal design; actual maximum clock frequency can be lower and depends on the specific PCB layout.
² Timing based on 15pF output loading.
### 4.5.3 \( \text{I}^2\text{C} \) Timing

The following figure illustrates \( \text{I}^2\text{C} \) Slave timing.

**Figure 4-3. \( \text{I}^2\text{C} \) Timing Diagram**

The following table provides \( \text{I}^2\text{C} \) Slave timing parameters.

**Table 4-7. \( \text{I}^2\text{C} \) Timing Parameters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCL Clock Frequency</td>
<td>( f_{\text{SCL}} )</td>
<td>0</td>
<td>400</td>
<td>kHZ</td>
<td>-</td>
</tr>
<tr>
<td>SCL Low Pulse Width</td>
<td>( t_{\text{WL}} )</td>
<td>1.3</td>
<td>-</td>
<td>µs</td>
<td>-</td>
</tr>
<tr>
<td>SCL High Pulse Width</td>
<td>( t_{\text{WH}} )</td>
<td>0.6</td>
<td>-</td>
<td>µs</td>
<td>-</td>
</tr>
<tr>
<td>SCL, SDA Fall Time</td>
<td>( t_{\text{HL}} )</td>
<td>-</td>
<td>300</td>
<td>ns</td>
<td>-</td>
</tr>
<tr>
<td>SCL, SDA Rise Time</td>
<td>( t_{\text{LH}} )</td>
<td>-</td>
<td>300</td>
<td>ns</td>
<td>This is dictated by external components</td>
</tr>
<tr>
<td>START Setup Time</td>
<td>( t_{\text{SUSTA}} )</td>
<td>0.6</td>
<td>-</td>
<td>µs</td>
<td>-</td>
</tr>
<tr>
<td>START Hold Time</td>
<td>( t_{\text{HDSTA}} )</td>
<td>0.6</td>
<td>-</td>
<td>µs</td>
<td>-</td>
</tr>
<tr>
<td>SDA Setup Time</td>
<td>( t_{\text{SUDAT}} )</td>
<td>100</td>
<td>-</td>
<td>ns</td>
<td>-</td>
</tr>
<tr>
<td>SDA Hold Time</td>
<td>( t_{\text{HDDAT}} )</td>
<td>0</td>
<td>-</td>
<td>ns</td>
<td>Slave and Master Default Programming Option</td>
</tr>
<tr>
<td></td>
<td></td>
<td>40</td>
<td>-</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Min</td>
<td>Max</td>
<td>Units</td>
<td>Remarks</td>
</tr>
<tr>
<td>---------------------------------</td>
<td>--------</td>
<td>-----</td>
<td>-----</td>
<td>-------</td>
<td>---------</td>
</tr>
<tr>
<td>STOP Setup time</td>
<td>$t_{\text{SUSTO}}$</td>
<td>0.6</td>
<td>-</td>
<td>µs</td>
<td>-</td>
</tr>
<tr>
<td>Bus Free Time Between STOP and START</td>
<td>$t_{\text{BUF}}$</td>
<td>1.3</td>
<td>-</td>
<td>µs</td>
<td>-</td>
</tr>
<tr>
<td>Glitch Pulse Reject</td>
<td>$t_{\text{PR}}$</td>
<td>0</td>
<td>50</td>
<td>ns</td>
<td>-</td>
</tr>
</tbody>
</table>
5. Power Management

The ATWILC1000-MR110xB module has several device states:

- **On states:**
  - ON_Transmit – device actively transmits an 802.11 signal. Highest output power and nominal current consumption.
  - ON_Receive – device actively receives an 802.11 signal. Lowest sensitivity and nominal current consumption.
  - ON_Doze – device is powered on but it does not actively transmit or receive the data.
  - Power_Down – device core supply is powered off.

The following pins are used to switch between the ON and Power_Down states:

- CHIP_EN – this pin (pin 22) enables or disables the DC/DC converter.
- VDDIO – I/O supply voltage from external supply.

In the ON states, VDDIO is ON and CHIP_EN is high (at VDDIO voltage level). To change from the ON states to Power_Down state, connect the RESETN and CHIP_EN pin to logic low (GND) by following the power down sequence mentioned in 5.3 Power-Up/Down Sequence. When VDDIO is off and CHIP_EN is low, the chip is powered off with no leakage (also see 5.2 Restrictions for Power States).

5.1 Current Consumption in Various Device States

The following table provides this module's current consumption in various device states.

Table 5-1. Current Consumption

<table>
<thead>
<tr>
<th>Device State</th>
<th>Code Rate</th>
<th>Output Power (dBm)</th>
<th>Current Consumption$^1$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>I$_{VBATT}$</td>
</tr>
<tr>
<td>ON_Transmit</td>
<td>802.11b 1Mbps</td>
<td>17.6</td>
<td>266 mA</td>
</tr>
<tr>
<td></td>
<td>802.11b 11Mbps</td>
<td>18.5</td>
<td>239 mA</td>
</tr>
<tr>
<td></td>
<td>802.11g 6Mbps</td>
<td>18.6</td>
<td>249 mA</td>
</tr>
<tr>
<td></td>
<td>802.11g 54Mbps</td>
<td>16.9</td>
<td>173 mA</td>
</tr>
<tr>
<td></td>
<td>802.11n MCS 0</td>
<td>17.7</td>
<td>253 mA</td>
</tr>
<tr>
<td></td>
<td>802.11n MCS 7</td>
<td>14.0</td>
<td>164 mA</td>
</tr>
<tr>
<td>ON_Receive</td>
<td>802.11b 1Mbps</td>
<td>N/A</td>
<td>63 mA</td>
</tr>
<tr>
<td></td>
<td>802.11b 11Mbps</td>
<td>N/A</td>
<td>63 mA</td>
</tr>
<tr>
<td></td>
<td>802.11g 6Mbps</td>
<td>N/A</td>
<td>63 mA</td>
</tr>
<tr>
<td></td>
<td>802.11g 54Mbps</td>
<td>N/A</td>
<td>63 mA</td>
</tr>
<tr>
<td></td>
<td>802.11n MCS 0</td>
<td>N/A</td>
<td>63 mA</td>
</tr>
<tr>
<td></td>
<td>802.11n MCS 7</td>
<td>N/A</td>
<td>63 mA</td>
</tr>
<tr>
<td>ON_Doze</td>
<td>N/A</td>
<td>N/A</td>
<td>380µA</td>
</tr>
</tbody>
</table>
5.2 Restrictions for Power States

When no power is supplied to the device, the DC/DC Converter output and VDDIO are both turned off (at ground potential). In this case, a voltage cannot be applied to the device pins because each pin contains an ESD diode from the pin to supply. This diode will turn on when voltage higher than one diode-drop is supplied to the pin.

If a voltage must be applied to the signal pads while the chip is in a low power state, the VDDIO supply must be on, so the Sleep mode or power-down state must be used.

Similarly, to prevent the pin-to-ground diode from turning on, do not apply a voltage that is more than one diode-drop below ground to any pin.

5.3 Power-Up/Down Sequence

The following figure illustrates the power-up/down sequence for the ATWILC1000-MR110xB module.

Figure 5-1. Power-Up/Down Sequence

The following table provides power-up/down sequence timing parameters.
Table 5-2. Power-Up/Down Sequence Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
<th>Description</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_A )</td>
<td>0</td>
<td>-</td>
<td>ms</td>
<td>VBAT rise to VDDIO rise</td>
<td>VBAT and VDDIO can rise simultaneously or connected together. VDDIO must not rise before VBAT.</td>
</tr>
<tr>
<td>( t_B )</td>
<td>0</td>
<td>-</td>
<td>ms</td>
<td>VDDIO rise to CHIP_EN rise</td>
<td>CHIP_EN must not rise before VDDIO. CHIP_EN must be driven high or low and must not be left floating.</td>
</tr>
<tr>
<td>( t_C )</td>
<td>5</td>
<td>-</td>
<td>ms</td>
<td>CHIP_EN rise to RESETN rise</td>
<td>This delay is required to stabilize the XO clock before RESETN removal. RESETN must be driven high or low and must not be left floating.</td>
</tr>
<tr>
<td>( t_{A'} )</td>
<td>0</td>
<td>-</td>
<td>ms</td>
<td>VDDIO fall to VBAT fall</td>
<td>VBAT and VDDIO fall simultaneously or connected together. VBAT must not fall before VDDIO.</td>
</tr>
<tr>
<td>( t_{B'} )</td>
<td>0</td>
<td>-</td>
<td>ms</td>
<td>CHIP_EN fall to VDDIO fall</td>
<td>VDDIO must not fall before CHIP_EN. CHIP_EN and RESETN must fall simultaneously.</td>
</tr>
<tr>
<td>( t_{C'} )</td>
<td>0</td>
<td>-</td>
<td>ms</td>
<td>RESETN fall to VDDIO fall</td>
<td>VDDIO must not fall before RESETN. RESETN and CHIP_EN fall simultaneously.</td>
</tr>
</tbody>
</table>

5.4 Digital I/O Pin Behavior During Power-Up Sequences

The following table represents the digital I/O pin states corresponding to the device power modes.

Table 5-3. Digital I/O Pin Behavior in Different Device States

<table>
<thead>
<tr>
<th>Device State</th>
<th>VDDIO</th>
<th>CHIP_EN</th>
<th>RESET N</th>
<th>Output Driver</th>
<th>Input Driver</th>
<th>Pull Up/Down Resistor (96 kOhm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power_Down: core supply OFF</td>
<td>High</td>
<td>Low</td>
<td>Low</td>
<td>Disabled (Hi-Z)</td>
<td>Disabled</td>
<td>Disabled</td>
</tr>
<tr>
<td>Power-On Reset: core supply and hard reset ON</td>
<td>High</td>
<td>High</td>
<td>Low</td>
<td>Disabled (Hi-Z)</td>
<td>Disabled</td>
<td>Enabled</td>
</tr>
<tr>
<td>Power-On Default: core supply ON, device out of reset and not programmed</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>Disabled (Hi-Z)</td>
<td>Enabled</td>
<td>Enabled</td>
</tr>
<tr>
<td>On_Doze/ On_Transmit/ On_Receive: core supply ON, device programmed by firmware</td>
<td>High</td>
<td>High</td>
<td>High</td>
<td>Programmed by firmware for each pin: enabled or disabled</td>
<td>Opposite of Output Driver state</td>
<td>Programmed by firmware for each pin: enabled or disabled</td>
</tr>
</tbody>
</table>
6. CPU and Memory Subsystems

6.1 Processor
This ATWILC1000-MR110xB module has a Cortus APS3 32-bit processor. This processor performs many of the MAC functions including but not limited to association, authentication, power management, security key management, and MSDU aggregation/deaggregation. In addition, the processor provides flexibility for various modes of operation, such as STA and AP modes.

6.2 Memory Subsystem
The APS3 core uses a 128 KB instruction/boot ROM along with a 160 KB instruction RAM and a 64 KB data RAM. In addition, the device uses a 128 KB shared RAM, accessible by the processor and MAC that allows the APS3 core to perform various data management tasks on the Tx and Rx data packets.

6.3 Nonvolatile Memory (eFuse)
This ATWILC1000-MR110xB module has 768 bits of nonvolatile eFuse memory that is read by the CPU after device reset. This nonvolatile One-Time-Programmable (OTP) memory is used to store customer-specific parameters, such as MAC address; various calibration information, such as Tx power, crystal frequency offset etc; and other software-specific configuration parameters. The eFuse is partitioned into six 128 bit banks. Each bank has the same bit map, mentioned in the following figure. The purpose of the first 80 bits in each bank is fixed, and the remaining 48 bits are general purpose software-dependent bits. Each bank is programmed independently, which allows for several updates of the device parameters following the initial programming. For example, if the MAC address has to be changed, Bank 1 has to be programmed with the new MAC address along with the values of TX gain correction and frequency offset if they are used and programmed in the Bank 0. The contents of Bank 0 have to be invalidated in this case by programming the Invalid bit in the Bank 0. This will allow the firmware to use the MAC address from Bank 1.

By default, all the ATWILC1000-MR110PB and ATWILC1000-MR110UB modules are programmed with the MAC address and the Frequency Offset bits of Bank 0.
Figure 6-1. eFuse Bit Map

- Used
- Invalid
- Version
- Reserved

- MAC ADDR
- Used

- Flags
- 8

- 48

- 8
- TX Gain Correction

- 16
- Used
- Freq Offset

- Bank 0
- MAC ADDR
- G
- FO

- Bank 1
- Bank 2
- Bank 3
- Bank 4
- Bank 5

- 128 Bits
7. **WLAN Subsystem**

The WLAN subsystem is composed of the Media Access Controller (MAC), Physical Layer (PHY), and the radio.

7.1 **MAC**

7.1.1 **Description**

This module is designed to operate at low power, while providing high data throughput. The IEEE 802.11 MAC functions are implemented with a combination of dedicated datapath engines, hardwired control logic, and a low power, high-efficiency microprocessor. The combination of dedicated logic with a programmable processor provides optimal power efficiency and real time response while providing the flexibility to accommodate evolving standards and future feature enhancements.

The dedicated datapath engines are used to implement data path functions with heavy computational requirements. For example, a Frame Check Sequence (FCS) engine checks the Cyclic Redundancy Check (CRC) of the transmitting and receiving packets, and a cipher engine performs all the required encryption and decryption operations for the WEP, WPA-TKIP, WPA2 CCMP-AES and WPA2 Enterprise security requirements.

Control functions, which have real time requirements, are implemented using hardwired control logic modules. These logic modules offer real time response while maintaining configurability through the processor. Examples of hardwired control logic modules are the channel access control module (implements EDCA/HCCA, Beacon Tx control, interframe spacing, and so on), protocol timer module (responsible for the Network Access vector, back-off timing, timing synchronization function, and slot management), MAC Protocol Data Unit (MPDU) handling module, aggregation/deaggregation module, block ACK controller (implements the protocol requirements for burst block communication), and Tx/Rx control Finite State Machine (FSM) (coordinate data movement between PHY and MAC interface, cipher engine, and the Direct Memory Acces (DMA) interface to the Tx/Rx FIFOs).

Following are the characteristics of MAC functions implemented solely in software on the microprocessor:

- Functions with high memory requirements or complex data structures. Examples are association table management and power save queuing.
- Functions with low computational load or without critical real time requirements. Examples are authentication and association.
- Functions that require flexibility and upgradeability. Examples are beacon frame processing and QoS scheduling.

7.1.2 **Features**

The ATWILC1000-MR110xB IEEE 802.11 MAC supports the following functions:

- IEEE 802.11b/g/n
- IEEE 802.11e WMM QoS EDCA/PCF multiple access categories traffic scheduling
- Advanced IEEE 802.11n features:
  - Transmission and reception of aggregated MPDUs (A-MPDU)
  - Transmission and reception of aggregated MSDUs (A-MSDU)
  - Immediate block acknowledgment
  - Reduced Interframe Spacing (RIFS)
• Supports IEEE 802.11i and WFA security with key management
  – WEP 64/128
  – WPA-TKIP
  – 128-bit WPA2 CCMP (AES)
  – WPA2 Enterprise
• Advanced power management
  – Standard IEEE 802.11 Power save mode
  – Wi-Fi alliance WMM-PS (U-APSD)
• RTS-CTS and CTS self support
• Supports either STA or AP mode in the infrastructure basic service set mode
• Supports concurrent mode of operation
• Supports Independent Basic Service Set (IBSS)

7.2 PHY

The ATWILC1000-MR110xB module WLAN PHY is designed to achieve reliable and power-efficient physical layer communication specified by IEEE 802.11 b/g/n in single stream mode with 20 MHz bandwidth. The advanced algorithms are used to achieve maximum throughput in a real world communication environment with impairments and interference. The PHY implements all the required functions such as Fast Fourier Transform (FFT), filtering, Forward Error Correction (FEC) that is a Viterbi decoder, frequency, timing acquisition and tracking, channel estimation and equalization, carrier sensing, clear channel assessment and automatic gain control.

Features

The IEEE 802.11 PHY supports the following functions:

• Single antenna 1x1 stream in 20 MHz channels
• Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, and 11 Mbps
• Supports IEEE 802.11g OFDM modulation: 6, 9, 12, 18, 24, 36, 48, and 54 Mbps
• Supports IEEE 802.11n HT modulations MCS0-7, 20 MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, and 72.2 Mbps
• IEEE 802.11n mixed mode operation
• Per packet Tx power control
• Advanced channel estimation/equalization, automatic gain control, CCA, carrier/symbol recovery and frame detection

7.2.1 Features

The IEEE 802.11 PHY supports the following functions:

• Single antenna 1x1 stream in 20 MHz channels
• Supports IEEE 802.11b DSSS-CCK modulation: 1, 2, 5.5, and 11 Mbps
• Supports IEEE 802.11g OFDM modulation: 6, 9, 12, 18, 24, 36, 48, and 54 Mbps
• Supports IEEE 802.11n HT modulations MCS0-7, 20 MHz, 800 and 400ns guard interval: 6.5, 7.2, 13.0, 14.4, 19.5, 21.7, 26.0, 28.9, 39.0, 43.3, 52.0, 57.8, 58.5, 65.0, and 72.2 Mbps
• IEEE 802.11n mixed mode operation
• Per packet Tx power control
7.3 Radio
This section describes the properties and characteristics of the ATWILC1000- MR110xB and Wi-Fi radio transmit and receive performance capabilities of the device. The performance measurements are taken at the RF pin assuming 50Ω impedance; the RF performance is assured for room temperature of 25°C with a derating of 2-3dB at boundary conditions.

Measurements were taken under typical conditions: VBATT at 3.3V; VDDIO at 3.3V ,and temperature at +25°C.

Table 7-1. Features and Properties

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module Part Number</td>
<td>ATWILC1000-MR110xB</td>
</tr>
<tr>
<td>WLAN Standard</td>
<td>IEEE 802.11b/g/n, Wi-Fi compliant</td>
</tr>
<tr>
<td>Host Interface</td>
<td>SPI, SDIO</td>
</tr>
<tr>
<td>Dimension</td>
<td>L x W x H: 21.7 x 14.7 x 2.1 (typical) mm</td>
</tr>
<tr>
<td>Frequency range</td>
<td>2.412 GHz ~ 2.472 GHz (2.4 GHz ISM band)</td>
</tr>
<tr>
<td>Number of channels</td>
<td>11 for North America, 13 for Europe</td>
</tr>
<tr>
<td>Modulation</td>
<td>802.11b: DQPSK, DBPSK, CCK</td>
</tr>
<tr>
<td></td>
<td>802.11g/n: OFDM/64-QAM,16-QAM, QPSK, BPSK</td>
</tr>
<tr>
<td>Data rate</td>
<td>802.11b: 1, 2, 5.5, 11 Mbps</td>
</tr>
<tr>
<td></td>
<td>802.11g: 6, 9, 12, 18, 24, 36, 48, 54 Mbps</td>
</tr>
<tr>
<td>Data rate (20 MHz, short GI,400ns)</td>
<td>802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2 Mbps</td>
</tr>
<tr>
<td>Operating temperature(1)</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>-40°C to 125°C</td>
</tr>
<tr>
<td>Humidity</td>
<td>Operating humidity 10% to 95% non-condensing</td>
</tr>
<tr>
<td></td>
<td>Storage humidity 5% to 95% non-condensing</td>
</tr>
</tbody>
</table>

Note:
1. RF performance is assured at room temperature of 25°C with a 2-3db change at boundary conditions.
8. **External Interfaces**

This section describes the various host and debug interfaces of the ATWILC1000-MR110xB module.

The ATWILC1000-MR110xB external interfaces include:

- I²C for debug
- SPI/SDIO for control and data transfer
- UART for debug
- General purpose Input/Output GPIO pins

8.1 **Interfacing with the Host Microcontroller**

This section describes how to interface the ATWILC1000-MR110xB module with the host microcontroller. The interface is comprised of a slave SPI/SDIO and additional control signals, as shown in the following figure. Additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

![Figure 8-1. Interfacing with the Host Microcontroller](image)

<table>
<thead>
<tr>
<th>Module Pin</th>
<th>Function(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>RESET_N</td>
</tr>
<tr>
<td>11</td>
<td>WAKE</td>
</tr>
<tr>
<td>13</td>
<td>IRQ_N</td>
</tr>
<tr>
<td>22</td>
<td>CHIP_EN</td>
</tr>
<tr>
<td>16</td>
<td>SPI_SSN/SD_DATA1</td>
</tr>
</tbody>
</table>
Note:

1. Logic input for module pin SDIO_SPI_CFG(10) determines whether SDIO or SPI slave interface is enabled. Connect SDIO_SPI_CFG to VDDIO through a 1MΩ resistor to enable the SPI interface. Connect SDIO_SPI_CFG to ground to enable SDIO interface.
2. It is recommended to place test points for pins I2C_SDA(3), I2C_SCL(2), GPIO_3(25) and GPIO_5(27) in the design.

8.2 SPI Slave Interface

The SPI slave interface can be enabled by connecting the SDIO_SPI_CFG pin to VDDIO. This SPI interface is used to exchange the control and 802.11 data. The SPI is a full duplex slave-synchronous serial interface that is available following reset when pin 10 (SDIO_SPI_CFG) is connected to VDDIO.

The SPI interface pin mapping configuration is provided in the following table.

Table 8-2. SPI Interface Pin Mapping

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>SDIO_SPI_CFG: Must be connected to VDDIO</td>
</tr>
<tr>
<td>16</td>
<td>SSN: Active-Low Slave Select</td>
</tr>
<tr>
<td>15</td>
<td>MOSI: Serial Data Receive</td>
</tr>
<tr>
<td>18</td>
<td>SCK: Serial Clock</td>
</tr>
<tr>
<td>17</td>
<td>MISO: Serial Data Transmit</td>
</tr>
</tbody>
</table>

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial master and other serial slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip and also initiate DMA transfers.

The SPI SSN, MOSI, MISO and SCK pins of this module have internal programmable pull up resistors. These resistors are programmed to be disabled. Otherwise, if any of the SPI pins are driven to a low level while this module is in the Low-Power Sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module.

The SPI slave interface supports four standard modes as determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) settings. These modes are illustrated in the following table. See also: Table 4-5, SPI Slave Modes in the datasheet: http://ww1.microchip.com/downloads/en/DeviceDoc/70005326B.pdf
Table 8-3. SPI Slave Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>CPOL</th>
<th>CPHA</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Note:** The ATWILC1000 firmware uses “SPI Mode 0” to communicate with the host.

The red lines in the following figure correspond to clock phase at 0 and the blue lines correspond to clock phase at 1.

**Figure 8-2. SPI Slave Clock Polarity and Clock Phase Timing**

8.3 **SDIO Slave Interface**

The SDIO interface is enabled by connecting the SDIO_SPI_CFG pin to ground. This SDIO interface is used to exchange the control and 802.11 data. The SDIO interface is available after reset when pin 10 (SDIO_SPI_CFG) is connected to ground.

This SDIO is a full speed interface. The interface supports the 1-bit/4-bit SD transfer mode at the clock range of 0-50 MHz. The host uses this interface to read and write from any register within the chip and also configures this module for DMA data transfer.

The SDIO interface pin mapping configuration is provided in the following table.

**Table 8-4. ATWILC1000 SDIO Interface Pin Mapping**

<table>
<thead>
<tr>
<th>Pin #</th>
<th>SDIO Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>SDIO_SPI_CFG: Must be connected to ground</td>
</tr>
<tr>
<td>14</td>
<td>DAT3: Data 3</td>
</tr>
<tr>
<td>15</td>
<td>DAT2: Data 2</td>
</tr>
<tr>
<td>16</td>
<td>DAT1: Data 1</td>
</tr>
</tbody>
</table>
The SDIO card is detected when it is inserted into an SDIO host. During the normal initialization and interrogation of the card by the host, the card identifies itself as an SDIO device. The host software obtains the card information in a tuple (linked list) format and determines if that card’s I/O function(s) are acceptable to activate. If the card is acceptable, it is allowed to power-up fully and start the I/O function(s) built into the card.

The SD memory card communication is based on an advanced 9-pin interface (clock, command, four data and three power lines) designed to operate at maximum operating frequency of 50 MHz.

### 8.3.1 Features
- Compliant with SDIO card specification version 2.0
- Host clock rate variable between 0 and 50 MHz
- Supports 1-bit/4-bit SD bus modes
- Allows card to interrupt host
- Responds to direct read/write (IO52) and extended read/write (IO53) transactions
- Supports suspend/resume operation

### 8.4 UART Debug Interface
This module has a Universal Asynchronous Receiver/Transmitter (UART) interface on J25(RxD) and J27(TxD) pins. This interface should be used only for debugging purposes. The UART is compatible with the RS-232 standard, where ATWILC1000-MR110xB operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

The following is the default configuration for the UART interface of ATWILC1000-MR110xB:
- Baud rate: 115200
- Data: 8 bit
- Parity: None
- Stop bit: 1 bit
- Flow control: None

It also has Rx and Tx FIFOs, which ensure reliable high speed reception and low software overhead transmission. FIFO size is 4x8 for both Rx and Tx direction. The UART has status registers that show the number of received characters available in the FIFO and various error conditions; in addition, it has the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in the following figure. This example shows 7-bit data (0x45), odd parity, and two stop bits.
8.5 \textit{I}^2\textit{C} Slave Interface

This module provides an \textit{I}^2\textit{C} bus slave that allows for easy debugging of the ATWILC1000-MR110xB devices. It supports \textit{I}^2\textit{C} bus Version 2.1 – 2000.

The \textit{I}^2\textit{C} interface is used only for debug. This interface is a two-wire serial interface consisting of a serial data line (SDA, Pin 17) and a serial clock (SCL, Pin 18). It responds to seven bit address value 0x60. This module \textit{I}^2\textit{C} interface operates in standard mode (with data rates up to 100Kb/s) and fast mode (with data rates up to 400Kb/s).

The \textit{I}^2\textit{C} is a synchronous serial interface. The SDA line is a bidirectional signal and changes only when the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire AND functions on the bus. The devices on the bus are limited to the 400pF capacitance. Data is transmitted in byte packages.

For specific information, refer to the Philips Specification entitled “The I2C -Bus Specification, Version 2.1.”
9. **Notes on Interfacing with the ATWILC1000-MR110xB**

**Programmable Pull up Resistors**

The ATWILC1000-MR110xB module provides programmable pull up resistors on various pins. The purpose of these resistors is to keep any unused input pins from floating, which causes excess current to flow through the input buffer from the VDDIO supply. Any unused pin on the device must leave these pull up resistors enabled, so that the pin will not float. The default state at power-up is for the pull up resistor to be enabled; however, any pin that is used must have the pull up resistor disabled. The reason for this is that if any pins are driven to a low level while the device is in the low power sleep state, current flows from the VDDIO supply through the pull up resistors, increasing the current consumption of the module. Since the value of the pull up resistor is approximately 100 kOhm, the current through any pull up resistor that is being driven low is VDDIO/100K. For VDDIO = 3.3V, the current is approximately 33 µA. The pins that are used and have programmable the pull up resistor disabled should always be actively driven to either a high or low level and not be allowed to float.
10. **Application Reference Design**

This section provides the reference schematic for ATWILC1000-MR110xB module with SPI and SDIO host interfaces.

**Figure 10-1. ATWILC1000-MR110xB Reference Schematic - SDIO Host Interface**

![Reference Schematic - SDIO Host Interface](image)

**Table 10-1. ATWILC1000-MR110xB Reference Schematic - SDIO Host Interface - Bill of Materials**

<table>
<thead>
<tr>
<th>Item</th>
<th>Qty.</th>
<th>Reference</th>
<th>Value</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Footprint</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>9</td>
<td>R2, R3,</td>
<td>0 R</td>
<td>RESISTOR, Thick Film, 0 ohm</td>
<td>Yageo Corporation</td>
<td>RC0402JR-070RL</td>
<td>0402</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R4, R5,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R6, R7,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R8, R9,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R10,</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R2-R10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>R2-R10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>U1</td>
<td></td>
<td>Wi-Fi Module</td>
<td>Microchip Technology Inc.</td>
<td>ATWILC1000-MR110xB</td>
<td></td>
</tr>
</tbody>
</table>
Figure 10-2. ATWILC1000-MR110xB Reference Schematic - SPI Host Interface

Table 10-2. ATWILC1000-MR110xB Reference Schematic - SPI Host Interface - Bill of Materials

<table>
<thead>
<tr>
<th>Item</th>
<th>Qty.</th>
<th>Reference</th>
<th>Value</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Footprint</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>R1</td>
<td>1 M</td>
<td>RESISTOR, Thick Film, 1 M ohm, 0402</td>
<td>Yageo Corporation</td>
<td>RC0100FR-071ML</td>
<td>0402</td>
</tr>
<tr>
<td>2</td>
<td>9</td>
<td>R2, R3, R4, R5, R6, R7, R8, R9, R10</td>
<td>0 R</td>
<td>RESISTOR, Thick Film, 0 ohm, 0402</td>
<td>Yageo Corporation</td>
<td>RC0402JR-070RL</td>
<td>0402</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>U1</td>
<td>ATWILC1000-MR110xB</td>
<td>Wi-Fi Module</td>
<td>Microchip Technology Inc.</td>
<td>ATWILC1000-MR110xB</td>
<td></td>
</tr>
</tbody>
</table>
11. **Module Outline Drawings**

The ATWILC1000-MR110PB module package details are outlined in the following figure. Dimensions are in mm.

*Figure 11-1. Module Drawings – ATWILC1000-MR110PB - Top, Bottom and Side Views*

The ATWILC1000-MR110UB module package details are outlined in the following figure. Dimensions are in mm.
This section provides the outline drawing for the recommended footprint for the ATWILC1000-MR110xB module. It is imperative that the center Ground Pad is provided, with an array of GND vias to provide a good ground and act as thermal sink for the ATWILC1000-MR110xB module.
Figure 11-3. Recommended Solder Pad Footprint

NOTE: THIS PAD MUST BE TIED TO GND.

SOLDER PAD FOOTPRINT

Drawing not to scale. Untoleranced dimensions. Units=mm.
12. **Design Consideration**
   This section provides the guidelines on placement and routing to achieve the best performance.

12.1 **ATWILC1000-MR110PB Placement and Routing Guidelines**
   It is critical to follow the recommendations listed below to achieve the best RF performance:

   - The module must be placed on host board. The printed antenna area must overlap with the carrier board. The portion of the module containing the antenna should not stick out over the edge of the host board. The antenna is designed to work properly when it is sitting directly on top of a 1.5mm thick printed circuit board. Figure 12-2 shows the best, poor and worst case module placements in host board.

   - If the module is placed at the edge of the host board, a minimum 22mm by 5mm area directly under the antenna must be clear of all metal on all layers of the board. “In-land” placement is acceptable; however, deepness of keep-out area must grove to: module edge to host board edge plus 5 mm.
     **Note:** Do not place the module in the middle of the host board or far away from the host board edge.

   - Follow the module placement, keepout, host PCB cutout recommendation as shown in Figure 12-1
     - Avoid routing any traces in the highlighted region on the top layer of the host board which will be directly below the module area.
     - Follow the electrical keepout layer recommendation as shown in Figure 12-1. There should be no copper in all layers of the host board in this region. Avoid placing any components (like mechanical spacers, bumpon etc) in the recommended electrical keepout area.
     - Place GND polygon pour below the module with the recommended boundary in the top layer of the host board as shown in Figure 12-1. Do not have any breaks in this GND plane.
     - Place sufficient GND vias in the highlighted area below the module for better RF performance.
     - It is recommended to have a 3x3 grid of GND vias solidly connecting the exposed GND paddle of the module to the inner layer ground plane. This will act as a good ground and thermal conduction for the ATWILC1000-MR110PB module. The GND vias should have a minimum via hole size of 0.3mm.
     - Follow the mechanical boundary of the host PCB as shown in the Figure 12-1
   - Keep the large metal objects away from antenna to avoid electromagnetic field blocking.
   - Do not enclose the antenna within a metal shield.
   - Keep any components which may radiate noise or signals within the 2.4 GHz – 2.5 GHz frequency band away from the antenna and if possible, shield those components. Any noise radiated from the host board in this frequency band will degrade the sensitivity of the module.
   - Make sure the width of the traces routed to GND, VDDIO and VBAT rails are sufficiently larger for handling the peak Tx current consumption.
12.2 Printed PCB Antenna Performance of ATWILC1000-MR110PB

The printed PCB antenna on the ATWILC1000-MR110PB is a meandered Inverted F Antenna (IFA). The antenna is fed via matching network, which is matched for the module installed on 1.5mm thick main board. Main board thickness deviation by ±1mm changes RX/TX performance by ±1dB maximum referring to RX/TX performance with default antenna matching network and installed on 1.5mm thick main board (FR-4 substrate).

Measured antenna gain is -0.3dBi.

Antenna Radiation Pattern
Following figures illustrate the antenna radiation pattern. During the measurement, the printed antenna is placed in the XZ plane with Y axis being perpendicular to the module and pointing to the back of the module.

**Figure 12-3. Antenna Radiation Pattern when Phi = 0 degree**

**Figure 12-4. Antenna Radiation Pattern when Phi = 90 degree**
Figure 12-5. Antenna Radiation Pattern when Theta = 90 degree
12.3 ATWILC1000-MR110UB Placement and Routing Guidelines

The ATWILC1000-MR110UB module has an Ultra Small Miniature RF Connector (u.FL) for the external antenna.

The choice of antenna is limited to the antenna types for which the module was tested and approved. For a list of tested and approved antennas that may be used with the module, refer to the respective country in the Regulatory Approval section.

An approved list of external antennas tested and certified with ATWILC1000-MR110UB module is shown in the Table 15-1.

It is critical to follow the recommendations listed below to achieve the best RF performance:

1. Avoid routing any traces on the top layer of the host board which will be directly below the module area.
2. Place GND polygon pour below the complete module area. Do not have any breaks in this GND plane.
3. Place sufficient GND vias in the GND polygon pour below the module area for better RF performance.

4. It is recommended to have a 3x3 grid of GND vias solidly connecting the exposed GND paddle of the module to the inner layer ground plane of the host board. This will act as a good ground and thermal conduction path for the ATWILC1000-MR110UB module. The GND vias should have a minimum via hole size of 0.3mm.

5. Keep the large metal objects away from external antenna to avoid electromagnetic field blocking.

6. Do not enclose the external antenna within a metal shield.

7. Keep any components which may radiate noise or signals within the 2.4 GHz – 2.5 GHz frequency band away from the external antenna and if possible, shield those components. Any noise radiated from the host board in this frequency band will degrade the sensitivity of the module.

8. Make sure the width of the traces routed to GND, VDDIO and VBAT rails are sufficiently larger for handling the peak Tx current consumption.
13. **Reflow Profile Information**

This section provides the guidelines for the reflow process to get the module soldered to the customer’s design.

13.1 **Storage Condition**

13.1.1 **Moisture Barrier Bag Before Opening**

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product shall be 12 months from the date the bag is sealed.

13.1.2 **Moisture Barrier Bag Open**

Humidity indicator cards must be blue, indicating that the humidity is <30%.

13.2 **Baking Conditions**

This module is rated at MSL level 3. After the sealed bag is opened, no baking is required within 168 hours as long as the devices are held at ≤ 30°C/60% RH or stored at < 10% RH.

The module requires baking before mounting if:

- The sealed bag has been open for more than 168 hours
- The humidity indicator card reads more than 10%
- SIPs need to be baked for eight hours at 125°C

13.3 **Reflow Oven**

**Cleaning**

The exposed ground paddle helps to self-align the module, avoiding pad misalignment. The use of no-clean solder pastes is recommended. Full drying of no-clean paste fluxes must be ensured as a result of the reflow process. This may require longer reflow profiles and/or peak temperatures toward the high end of the process window as recommended by the solder paste vendor. It is believed that uncured flux residues could lead to corrosion and/or shorting in accelerated testing and possibly the field.

**Rework**

Rework is to remove the mounted SIP package and replace with a new unit. It is recommended that once ATWILC1000-MR110xB has been removed it should never be reused. During the rework process, the mounted module and PCB are heated partially, and the module is removed. It is recommended to heat-proof the proximity of the mounted parts and junctions and use the best nozzle for rework that is suited to the module size.

For reflow process guidelines, refer to the Solder Reflow Recommendation Application Note.
14. **Module Assembly Considerations**

The ATWILC1000-MR110xB modules are assembled with an EMI Shield to ensure compliance with EMI emission and immunity rules. The EMI shield is made of a tin-plated steel (SPTE) and is not hermetically sealed. Solutions like IPA and similar solvents can be used to clean the ATWILC1000-MR110xB module; however, cleaning solutions that contain acid should never be used on the module.

The ATWILC1000-MR110xB modules are manufactured without any conformal coating applied. It is the customer’s responsibility if a conformal coating is specified and applied to the ATWILC1000- MR110xB module.
15. **Regulatory Approval**

Regulatory approvals received:

ATWILC1000-MR110PB

- United States/FCC ID: 2ADHKATWILC1000
- Canada/ISED:
  - IC: 20266-ATWILC1000
  - HVIN: ATWILC1000-MR110PB
  - PMN: ATWILC1000-MR110PB
- Europe/CE
- Japan/MIC: 005-101763
- Korea/KCC: R-CRM-mcp-WILC1000MR110P
- Taiwan/NCC: CCAN18LP0310T7
- China/SRRC: CMIIT ID: 2018DJ1313

ATWILC1000-MR110UB

- United States/FCC ID: 2ADHKATWILC1000U
- Canada/ISED:
  - IC: 20266-WILC1000UB
  - HVIN: ATWILC1000-MR110UB
  - PMN:
- Europe/CE

15.1 **United States**

The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules have received Federal Communications Commission (FCC) CFR47 Telecommunications, Part 15 Subpart C “Intentional Radiators” single-modular approval in accordance with Part 15.212 Modular Transmitter approval. Single-modular transmitter approval is defined as a complete RF transmission sub-assembly, designed to be incorporated into another device, that must demonstrate compliance with FCC rules and policies independent of any host. A transmitter with a modular grant can be installed in different end-use products (referred to as a host, host product, or host device) by the grantee or other equipment manufacturer, then the host product may not require additional testing or equipment authorization for the transmitter function provided by that specific module or limited module device.

The user must comply with all of the instructions provided by the Grantee, which indicate installation and/or operating conditions necessary for compliance.

A host product itself is required to comply with all other applicable FCC equipment authorization regulations, requirements, and equipment functions that are not associated with the transmitter module portion. For example, compliance must be demonstrated: to regulations for other transmitter components within a host product; to requirements for unintentional radiators (Part 15 Subpart B), such as digital devices, computer peripherals, radio receivers, etc.; and to additional authorization requirements for the non-transmitter functions on the transmitter module (i.e., Verification or Declaration of Conformity) as appropriate (e.g., Bluetooth and Wi-Fi transmitter modules may also contain digital logic functions).
15.1.1 Labeling and User Information Requirements
The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules have been labeled with their own FCC ID numbers. If the FCC ID is not visible when the module is installed inside another device, then the outside of the finished product into which the module is installed must display a label referring to the enclosed module. This exterior label can use wording as follows:

For the ATWILC1000-MR110PB:

<table>
<thead>
<tr>
<th>Contains Transmitter Module FCC ID: 2ADHKATWILC1000 or</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contains FCC ID: 2ADHKATWILC1000</td>
</tr>
</tbody>
</table>
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

For the ATWILC1000-MR110UB:

<table>
<thead>
<tr>
<th>Contains Transmitter Module FCC ID: 2ADHKATWILC1000U or</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contains FCC ID: 2ADHKATWILC1000U</td>
</tr>
</tbody>
</table>
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

A user’s manual for the finished product should include the following statement:

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Additional information on labeling and user information requirements for Part 15 devices can be found in KDB Publication 784748, which is available at the FCC Office of Engineering and Technology (OET) Laboratory Division Knowledge Database (KDB) https://apps.fcc.gov/oetcf/kdb/index.cfm

15.1.2 RF Exposure
All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).
From the FCC Grant: Output power listed is conducted. This transmitter is restricted for use with the specific antenna(s) tested in this application for Certification.

In the end product, the antenna(s) used with this transmitter must be installed to provide a separation distance of at least 6.5 cm from all persons and must not be co-located or operation in conjunction with any other antenna or transmitter. User and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying the RF exposure compliance.

15.1.3 Approved Antenna Types
To maintain modular approval in the United States, only the antenna types that have been tested shall be used. It is permissible to use a different antenna, provided the same antenna type and antenna gain (equal to or less than) is used. An antenna type comprises antennas having similar in-band and out-of-band radiation patterns.

Testing the ATWILC1000-MR110UB module was performed with the antenna types listed in Recommended External Antenna list.

Table 15-1. List of External Antenna - Antenna Gain at 2.5 GHz (dBi)

<table>
<thead>
<tr>
<th>Item</th>
<th>P/N</th>
<th>Manufacturer</th>
<th>Ant Gain 2.4GHz (dBi)</th>
<th>Antenna Type</th>
<th>ATWILC1000-MR110UB</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>FCC/ISED</td>
<td>CE</td>
</tr>
<tr>
<td>1</td>
<td>W3525B039</td>
<td>Pulse Electronics Corporation</td>
<td>2.0</td>
<td>PCB</td>
<td>X X</td>
</tr>
<tr>
<td>2</td>
<td>RN-SMA-4</td>
<td>Microchip</td>
<td>2.2</td>
<td>Dipole</td>
<td>X X</td>
</tr>
<tr>
<td>3</td>
<td>RFMTA870920IMLB301</td>
<td>WALSIN</td>
<td>1.8</td>
<td>Dipole</td>
<td>X X</td>
</tr>
<tr>
<td>4</td>
<td>RFMTA331215IMAB701</td>
<td>WALSIN</td>
<td>3.8</td>
<td>Metal Stamp</td>
<td>X X</td>
</tr>
<tr>
<td>5</td>
<td>RFMTA331240IMAB701</td>
<td>WALSIN</td>
<td>3.0</td>
<td>Metal Stamp</td>
<td>X X</td>
</tr>
<tr>
<td>6</td>
<td>RFPCA381013IMAB701</td>
<td>WALSIN</td>
<td>4.5</td>
<td>PCB</td>
<td>X X</td>
</tr>
<tr>
<td>7</td>
<td>RFPCA381035IMAB701</td>
<td>WALSIN</td>
<td>2.7</td>
<td>PCB</td>
<td>X X</td>
</tr>
<tr>
<td>8</td>
<td>RFA-02-3-C5H1</td>
<td>Aristotle</td>
<td>3.0</td>
<td>Dipole</td>
<td>X X</td>
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<tr>
<td>9</td>
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<td>Aristotle</td>
<td>5.0</td>
<td>Dipole</td>
<td>X X</td>
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<td>PCB</td>
<td>X X</td>
</tr>
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<td>3.0</td>
<td>PCB/Flexi</td>
<td>X X</td>
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<td>12</td>
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<td>Microchip</td>
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<td>Dipole</td>
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<td>X X</td>
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<td>Item</td>
<td>P/N</td>
<td>Manufacturer</td>
<td>Ant Gain 2.4GHz (dBi)</td>
<td>Antenna Type</td>
<td>ATWILC1000-MR110UB</td>
</tr>
<tr>
<td>------</td>
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<td>86254</td>
<td>Delock</td>
<td>2.0</td>
<td>PCB</td>
<td>- X</td>
</tr>
</tbody>
</table>

**Note:**
1. X = Antennas covered under the certification
2. If the end-product using the module is designed to have an antenna port that is accessible to the end user, RP (Reverse Polarity)-SMA socket must be used.
3. If an RF coaxial cable is used between the module RF output and the enclosure, then an RP-SMA connector must be used in the enclosure wall for interface with antenna.

15.1.4 **Helpful Websites**

15.2 **Canada**
The ATWILC1000-MR110PB and ATWILC1000-MR110UB module have been certified for use in Canada under Innovation, Science and Economic Development Canada (ISED, formerly Industry Canada) Radio Standards Procedure (RSP) RSP-100, Radio Standards Specification (RSS) RSS-Gen and RSS-247. Modular approval permits the installation of a module in a host device without the need to recertify the device.

15.2.1 **Labeling and User Information Requirements**
Label Requirements (from RSP-100 Issue 11, Section 3): The host device shall be properly labeled to identify the module within the host device.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labeled to display the Innovation, Science and Economic Development Canada certification number of the module, preceded by the words "Contains", or similar wording expressing the same meaning, as follows:

For the ATWILC1000-MR110PB:
**Contains IC: 20266-ATWILC1000**

For the ATWILC1000-MR110UB:
**Contains IC: 20266-WILC1000UB**

User Manual Notice for License-Exempt Radio Apparatus (from Section 8.4 RSS-Gen, Issue 4, November 2014): User manuals for license-exempt radio apparatus shall contain the following or equivalent notice in a conspicuous location in the user manual or alternatively on the device or both:
This device complies with Industry Canada license exempt RSS standard(s). Operation is subject to the following two conditions:

(1) This device may not cause interference, and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Guidelines on Transmitter Antenna for License Exempt Radio Apparatus:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

15.2.2 RF Exposure
All transmitters regulated by Innovation, Science and Economic Development Canada (ISED) must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radio communication Apparatus (All Frequency Bands).

This transmitter is restricted for use with a specific antenna tested in this application for certification, and must not be co-located or operating in conjunction with any other antenna or transmitters within a host device, except in accordance with Canada multi-transmitter product procedures.

The installation of the transmitter must ensure that the antenna has a separation distance of at least 6.5 cm from all persons or compliance must be demonstrated according to the ISED SAR procedures.

15.2.3 Canada_Helpful Websites

15.3 Europe
The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules are Radio Equipment Directive (RED) assessed radio modules that are CE marked and have been manufactured and tested with the intention of being integrated into a final product.
The ATWILC1000-MR110PB and ATWILC1000-MR110UB modules have been tested to RED 2014/53/EU Essential Requirements for Health and Safety (Article (3.1(a)), Electromagnetic Compatibility (EMC) (Article 3.1(b)), and Radio (Article 3.2), and are summarized in Table 15-2 and Table 15-3.

The ETSI provides guidance on modular devices in "Guide to the application of harmonised standards covering articles 3.1b and 3.2 of the RED 2014/53/EU (RED) to multi-radio and combined radio and non-radio equipment" document available at http://www.etsi.org/deliver/etsi_eg/203300_203399/203367/01.01.01_60/eg_203367v010101p.pdf.

Note: To maintain conformance to the testing listed in Table 15-2 and Table 15-3, the module shall be installed in accordance with the installation instructions in this data sheet and shall not be modified.

When integrating a radio module into a completed product, the integrator becomes the manufacturer of the final product and is therefore responsible for demonstrating compliance of the final product with the essential requirements against the RED.

15.3.1 Labeling and User Information Requirements

The label on the final product which contains the ATWILC1000-MR110PB and ATWILC1000-MR110UB module must follow CE marking requirements.

Table 15-2. European Compliance Testing - ATWILC1000-MR110PB

<table>
<thead>
<tr>
<th>Certification</th>
<th>Standards</th>
<th>Article</th>
<th>Laboratory</th>
<th>Report Number</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>Health</td>
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<td></td>
<td>50092557 001</td>
<td>11 Aug 2017</td>
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<tr>
<td>EMC</td>
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<td>[3.1(b)]</td>
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<td>11 Aug 2017</td>
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<td>EN 301 489-17 V3.1.1 \ EN 301 489-17 V3.2.0</td>
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<tr>
<td>Radio</td>
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</tr>
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</table>
### Table 15-3. European Compliance Testing - ATWILC1000-MR110UB

<table>
<thead>
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<th>Certification</th>
<th>Standards</th>
<th>Article</th>
<th>Laboratory</th>
<th>Report Number</th>
<th>Date</th>
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<td>EN300 328 v2.1.1</td>
<td>(3.2)</td>
<td></td>
<td>50125424 001</td>
<td>16 Mar 2018</td>
</tr>
</tbody>
</table>

#### 15.3.2 Conformity Assessment

From ETSI Guidance Note EG 203367, section 6.1 Non-radio products are combined with a radio product:

If the manufacturer of the combined equipment installs the radio product in a host non-radio product in equivalent assessment conditions (i.e. host equivalent to the one used for the assessment of the radio product) and according to the installation instructions for the radio product, then no additional assessment of the combined equipment against article 3.2 of the RED is required.

The European Compliance Testing listed in Table 15-2 was performed using the integral PCB antenna.

#### 15.3.3 Simplified EU Declaration of Conformity

Hereby, Microchip Technology Inc. declares that the radio equipment type ATWILC1000-MR110PB and ATWILC1000-MR110UB are in compliance with Directive 2014/53/EU.

The full text of the EU declaration of conformity is available at the following webpage: [http://www.microchip.com/design-centers/wireless-connectivity](http://www.microchip.com/design-centers/wireless-connectivity)

#### 15.3.4 Helpful Websites

A document that can be used as a starting point in understanding the use of Short Range Devices (SRD) in Europe is the European Radio Communications Committee (ERC) Recommendation 70-03 E, which can be downloaded from the European Communications Committee (ECC) at: [http://www.ecodocdb.dk/](http://www.ecodocdb.dk/).

Additional helpful web sites are:
15.4 Japan
The ATWILC1000-MR110PB has received type certification and is labeled with its own technical conformity mark and certification number as required to conform to the technical standards regulated by the Ministry of Internal Affairs and Communications (MIC) of Japan pursuant to the Radio Act of Japan.

Integration of this module into a final product does not require additional radio certification provided installation instructions are followed and no modifications of the module are allowed. Additional testing may be required:

- If the host product is subject to electrical appliance safety (for example, powered from an AC mains), the host product may require Product Safety Electrical Appliance and Material (PSE) testing. The integrator must contact their conformance laboratory to determine if this testing is required.
- There is a voluntary Electromagnetic Compatibility (EMC) test for the host product administered by VCCI: http://www.vcci.jp/vcci_e/index.html.

15.4.1 Labeling and User Information Requirements
The label on the final product which contains the ATWILC1000-MR110PB module must follow Japan marking requirements. The integrator of the module must refer to the labeling requirements for Japan available at the Ministry of Internal Affairs and Communications (MIC) website.

For the ATWILC1000-MR110PB module, due to a limited module size, the technical conformity logo and ID is displayed in the data sheet and/or packaging label and cannot be displayed on the module label. The final product in which this module is being used must have a label referring to the type certified module inside:

![Label](image)

15.4.2 Helpful Websites
- Association of Radio Industries and Businesses (ARIB): http://www.arib.or.jp/english/.

15.5 Korea
The ATWILC1000-MR110PB received certification of conformity in accordance with the Radio Waves Act. Integration of this module into a final product does not require additional radio certification provided installation instructions are followed and no modifications of the module are allowed.

15.5.1 Labeling and User Information Requirements
The label on the final product which contains the ATWILC1000-MR110PB module must follow KC marking requirements. The integrator of the module must refer to the labeling requirements for Korea available on the Korea Communications Commission (KCC) website.

The ATWILC1000-MR110PB module, is labeled with its own KC mark. The final product requires the KC mark and certificate number of the module:
15.5.2 Helpful Websites

- Korea Communications Commission (KCC): http://www.kcc.go.kr

15.6 Taiwan

The ATWILC1000-MR110PB module has received compliance approval in accordance with the Telecommunications Act. Customers seeking to use the compliance approval in their product must contact Microchip Technology Inc. sales or distribution partners to obtain a Letter of Authority.

Integration of this module into a final product does not require additional radio certification provided installation instructions are followed and no modifications of the module are allowed.

15.6.1 Labeling and User Information Requirements

For the ATWILC1000-MR110PB module, due to limited module size, the NCC mark and ID are displayed in the data sheet only and cannot be displayed on the module label.

The user's manual must contain below warning (for RF device) in traditional Chinese:

注意！

依據低功率電波輻射性電機管理辦法

第十二條 經型式認證合格之低功率射頻電機，非經許可，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。

第十四條 低功率射頻電機之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。

前項合法通信，指依電信規定作業之無線電信。

低功率射頻電機須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。
15.6.2 Helpful Website
National Communications Commission (NCC): http://www.ncc.gov.tw

15.7 China
The ATWILC1000-MR110PB module has received certification of conformity in accordance with the China MIIT Notice 2014-01 of State Radio Regulation Committee (SRRC) certification scheme. Integration of this module into a final product does not require additional radio certification, provided installation instructions are followed and no modifications of the module are allowed.

15.7.1 Labeling and User Information Requirements
The ATWILC1000-MR110PB module is labeled with its own CMIIT ID as follows:

CMIIT ID: 2018DJ1313

When Host system is using an approved Full Modular Approval (FMA) radio: The host must bear a label containing the statement “This device contains SRRC approved Radio module CMIIT ID: 2018DJ1313”.

15.8 Other Regulatory Information
• For information about other countries’ jurisdictions not covered here, refer to http://www.microchip.com/design-centers/wireless-connectivity/certifications
• Should other regulatory jurisdiction certification be required by the customer, or the customer needs to rectify the module for other reasons, contact Microchip for the required utilities and documentation
16. **Reference Documentation**

The following table provides the set of collateral documents to ease integration and device ramp.

**Table 16-1. Reference documents**

<table>
<thead>
<tr>
<th>Title</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATWILC1000/ATWILC3000 Wi-Fi Link Controller Linux® User Guide</td>
<td>This user guide describes how to run Wi-Fi on the ATWILC1000 SD card and to run Wi-Fi/BLE on the ATWILC3000 Shield board on the SAMA5D4 Xplained Ultra running with the Linux kernel 4.9.</td>
</tr>
<tr>
<td>ATWILC1000/ATWILC3000 Devices Linux Porting Guide</td>
<td>This user guide describes how to port the ATWILC1000 and ATWILC3000 Linux drivers to another platform and contains all the required modifications for driver porting.</td>
</tr>
<tr>
<td>ATWILC1000/ATWILC3000 Baremetal Wi-Fi®/BLE Link Controller Software Design Guide</td>
<td>This design guide helps the user in integrating ATWILC1000/ATWILC3000 in the application using RTOS from Advanced Software Framework (ASF).</td>
</tr>
</tbody>
</table>

**Note:**

For a complete listing of development support tools and documentation, visit [http://www.microchip.com/wwwproducts/en/ATWILC1000](http://www.microchip.com/wwwproducts/en/ATWILC1000) or refer to the customer support section for contacting the nearest Microchip field representative.
## Document Revision History

### Rev C - 05/2019

<table>
<thead>
<tr>
<th>Section</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Ordering Information and Module Marking</td>
<td>Updated Regulatory Certification</td>
</tr>
<tr>
<td>15. Regulatory Approval</td>
<td>• Updated with ATWILC1000-MR110PB information</td>
</tr>
<tr>
<td></td>
<td>• Added Table 15-3</td>
</tr>
<tr>
<td></td>
<td>• Added 15.4 Japan, 15.5 Korea, 15.6 Taiwan, and 15.7 China</td>
</tr>
</tbody>
</table>

### Rev B - 10/2017

<table>
<thead>
<tr>
<th>Section</th>
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<tr>
<td>MAC Features</td>
<td>Editorial updates</td>
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### Rev A - 08/2017

<table>
<thead>
<tr>
<th>Section</th>
<th>Changes</th>
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<tbody>
<tr>
<td>Document</td>
<td>• Updated from Atmel to Microchip template.</td>
</tr>
<tr>
<td></td>
<td>• Assigned a new Microchip document number. Previous version is Atmel 42503 revision C.</td>
</tr>
<tr>
<td></td>
<td>• ISBN number added.</td>
</tr>
<tr>
<td></td>
<td>• Updated module reference to ATWILC1000-MR110xB throughout the document.</td>
</tr>
<tr>
<td></td>
<td>• Removed reference to Bluetooth coexistence</td>
</tr>
<tr>
<td></td>
<td>• Added WFA certification details</td>
</tr>
<tr>
<td></td>
<td>• Updated block diagram Figure 2-1</td>
</tr>
<tr>
<td></td>
<td>• Updated pin description in Table 3-1</td>
</tr>
<tr>
<td></td>
<td>• Updated VDDIO absolute maximum voltage rating in Table 4-1 and added caution footnote</td>
</tr>
<tr>
<td></td>
<td>• Added operating temperature to Table 4-2</td>
</tr>
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<td></td>
<td>• Moved 4.4 Transmitter Performance, 4.3 Receiver Performance and 4.5 Timing Characteristics under 4. Electrical Specifications</td>
</tr>
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<td></td>
<td>• Updated description in 6.3 Nonvolatile Memory (eFuse)</td>
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<tr>
<td></td>
<td>• Revised the 4.4 Transmitter Performance and 4.3 Receiver Performance</td>
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<td>• Updated 10. Application Reference Design</td>
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<td>• Added 12. Design Consideration</td>
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<td>• Updated 16. Reference Documentation</td>
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### Rev C - 11/2016
<table>
<thead>
<tr>
<th>Section</th>
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</thead>
</table>
| Document | • Updated the device pinout drawing Figure 3-1 to make it easier to read  
  • Added section 11.5 regarding PCBA coatings  
  • Updated Marking diagram in Figure 1-1  
  • Revised values for Transmit Power and added notes in Table 4-4  
  • Added Pins and Agencies to Ordering Information in Table 1-1  
  • Added section 12.3 ATWILC1000-MR110UB Placement and Routing Guidelines  
  • Added Certification Notices  
  • Added 15. Regulatory Approval  
  • Updated Description to indicate both the MR110PB and MR110UB are covered  
  • Removed "With seamless roaming capabilities" from description  
  • Revised features to only support SPI and SDIO hosts.  
  • Removed references to WAPI  
  • Removed UART  
  • Moved Solder Pad drawing to be with POD drawings as in Figure 11-1  
  • Minor edits |

**Rev B - 5/2016**

<table>
<thead>
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</table>
| Document | • Revised POD drawings in 11. Module Outline Drawings  
  • Revised Footprint drawing in 11. Module Outline Drawings  
  • Removed Module schematics and BOM’s  
  • Added Reflow profile 13. Reflow Profile Information  
  • Updated SDIO timing content in SDIO Slave Timing  
  • Added footnotes to recommended operating ratings in Recommended Operating Conditions  
  • Updated SPI timing content in SPI Slave Timing |

**Rev A - 8/2015**

<table>
<thead>
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</thead>
</table>
| Document | Updated due to changes from ATWILC100A(42380D) to ATWILC1000B:  
  • Updated power numbers and description, added high-power and low-power modes  
  • Updated radio performance numbers  
  • Fixed typos in SPI interface timing  
  • Added hardware accelerators in feature list (security and checksum)  
  • Increased instruction RAM size from 128KB to 160KB  
  • Improved and corrected description of Coexistence interface  
  • Miscellaneous minor updates and corrections |
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- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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<thead>
<tr>
<th>AMERICAS</th>
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<th>ASIA/PACIFIC</th>
<th>EUROPE</th>
</tr>
</thead>
</table>
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Chandler, AZ 85224-6199  
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Fax: 480-792-7277  
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http://www.microchip.com/support  
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