ATSAMB11XR Family Errata

The ATSAMB11XR family of devices that you have received conform functionally to the current device data sheet located on the Microchip website: http://www.microchip.com/wwwproducts/en/ATSAMB11-ZR, except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Chip ID listed in the table below.

The errata described in this document will be addressed in future revisions of the ATSAMB11XR family silicon.

Table 1. ATSAMB11XR Family Silicon Device Identification

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Chip ID 0x4000B000[23:0]</th>
<th>Silicon Rev</th>
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<tbody>
<tr>
<td>ATSAMB11-XR2100A</td>
<td>0x2000B1</td>
<td>B0</td>
</tr>
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</table>

Note: Bits 0-23 of register with address 0x4000B000 contain the chip ID of the device.
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1. **Errata Details**

1.1 **I²C Master Interface**

I²C Master Interface does not support repeated start condition and clock stretching by slave.

**Work around**
None.

**Affected Silicon Revisions**

<table>
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1.2 **ADC**

When ADC is configured to operate in TDM (Time Division Multiplexing) mode, the ADC result for each channel is stored in the register corresponding to the previous channel as detailed. However, there is no issue with the functionality of the ADC. The ADC can be configured to operate in time domain multiplexing between four ADC input channels (GPIO_MS1, GPIO_MS2, GPIO_MS3 and GPIO_MS4) which are sampled in each ADC conversion cycle. This can be achieved by configuring the bits `RF_PMU_REGS1.SADC_CHN_CTRL=0` and `RF_PMU_REGS1.SADC_CHN_SEL[0:2]=0`.

The results for each conversion are stored in the following registers from the register group `LPMCU_MISC_REGS0`:

- Result of ADC for channel GPIO_MS4(ch3) stored in `SENS_ADC_CH2_DATA`
- Result of ADC for channel GPIO_MS3(ch2) stored in `SENS_ADC_CH1_DATA`
- Result of ADC for channel GPIO_MS2(ch1) stored in `SENS_ADC_CH0_DATA`
- Result of ADC for channel GPIO_MS1(ch0) stored in `SENS_ADC_CH3_DATA`

**Work around**
Read the results of ADC conversion for each ADC channel from the register as indicated above.

**Affected Silicon Revisions**

<table>
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## 2. Document Revision History

### Rev D - 08/2018

<table>
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<tr>
<td>DS80000763D</td>
<td>• Updated Table 1.</td>
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<td>• Changed B1 to B0 in Errata Details</td>
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### Rev C - 04/2018

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<td>DS80000763C</td>
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### Rev B - 09/2017

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<td>DS80000763B</td>
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### Rev A - 09/2017

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<td>DS80000763A</td>
<td>Initial release</td>
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