Introduction

The Microchip® ATA5577M3C is a contactless RFID IC (R/W-RFID) in the 100 kHz to 150 kHz frequency range applications. It is the Mega-Pad version of Microchip ATA5577M1, with programmable Q5 functionality and configuration register mapping. Unlike ATA5577M1/M2, the ATA5577M3C antenna capacity is not adjusted during production. Although the ATA5577M1/M2 datasheet is valid, this document provides an overview of the differences between ATA5577M1/M2 and ATA5577M3C.

Features

- Contactless Power Supply
- Contactless Read/Write Data Transmission
- Radio Frequency $f_{RF}$ from 100 kHz to 150 kHz
- Basic Mode, Extended Mode or Q5 Mode
- Compatible to Microchip T5557, ATA5567, and T5555B
- Replacement for Microchip e5551/T5551 in Most Common Operation Modes
- Configurable for ISO/IEC 11784/785 Compatibility
- 363-Bit EEPROM Memory in Total: 11 Blocks × (32 Bits + 1 Lock-Bit)
  - 7 × 32 bits EEPROM user memory including 32-bit password memory
  - 2 × 32 bits unique ID
  - 1 × 32-bit option register in EEPROM to set up the analog front end:
    - Clock detection level
    - Gap detection level
    - Improved downlink timing
    - Clamp voltage
    - Modulation voltage
    - Soft modulation switching
    - Write damping like the Microchip T5557/ATA5567 or with resistor
    - Downlink protocol
    - Q5-functionality and Q5-configuration register mapping
  - 1 × 32-bit configuration register in EEPROM to set up:
    - Data rate:
      - RF/128, binary selectable or
      - Fixed Basic mode rates
    - Modulation/coding:
      - Bi-phase, Manchester, FSK, PSK, NRZ
• Other Options:
  – Password mode
  – Max block feature
  – Direct Access mode
  – Sequence terminator(s)
  – Blockwise write protection (Lock bit)
  – Answer-On-Request (AOR) mode
  – Inverse data output
  – Disable Test mode access
  – Fast downlink (~6Kbits/s versus ~3Kbits/s)
  – OTP functionality
  – Init delay (~67ms)

• On-Chip Antenna Capacitor:
  – 330pF
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1. Memory

The memory is a 363-bit EEPROM, which is arranged in 11 blocks of 33 bits each. Page 0 contains 8 blocks and page 1 contains 3 blocks. All 33 bits of a block, including the Lock bit, are programmed simultaneously.

Block 0 of page 0 contains the mode and configuration data, which is not transmitted during regular read operations. Block 7 of page 0 may be used as a write protection password.

Block 3 of page 1 contains the option register, which is also not transmitted during regular read operation.

Bit 0 of every block is the Lock bit for that block. Once locked, the block (including the Lock bit itself) is not re-programmable through the RF field.

**Note:** The memory map is the same as that of ATA5577M1/M2.

**Figure 1-1. Memory Map**

1.1 Traceability Data for the ATA5577M3C

The traceability data is defined as follows:
Table 1-1. Arrangement of Traceability Data

<table>
<thead>
<tr>
<th>Denotation</th>
<th>Bit</th>
<th>Bitcount</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LSB first:</td>
<td>IC revision: D00-D01</td>
<td>2</td>
<td>D00 is LSB of IC revision</td>
</tr>
<tr>
<td>Lot ID:</td>
<td>D02-D42</td>
<td>17</td>
<td>D02 is LSB of lot ID</td>
</tr>
<tr>
<td>Wafer no.:</td>
<td>D43-D53</td>
<td>5</td>
<td>D43 is LSB of wafer no.</td>
</tr>
<tr>
<td>DoW:</td>
<td>D60-D91</td>
<td>14</td>
<td>D60 is LSB of DoW</td>
</tr>
<tr>
<td>RFU:</td>
<td>D92-D93</td>
<td>2</td>
<td>D92 is LSB of RFU</td>
</tr>
</tbody>
</table>

The traceability data in Q5 mode is always sent with Manchester RF/64 - independently of configuration register setting.
2. **Functional Specification**

This chapter describes the ATA5577M3C state diagram, modes of operation, and register configurations.

2.1 **AFE Option Register for the ATA5577M3C**

The ATA5577M3C has an additional bit in the AFE Option Register: Bit #23 controls the Q5 functionality.

*Figure 2-1. Block 3 Page 1 AFE Option Mapping ATA5577M3C*

<table>
<thead>
<tr>
<th>L</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
<th>11</th>
<th>12</th>
<th>13</th>
<th>14</th>
<th>15</th>
<th>16</th>
<th>17</th>
<th>18</th>
<th>19</th>
<th>20</th>
<th>21</th>
<th>22</th>
<th>23</th>
<th>24</th>
<th>25</th>
<th>26</th>
<th>27</th>
<th>28</th>
<th>29</th>
<th>30</th>
<th>31</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Note:**

1. If the Option Key is 6 or 9, the front end options are activated; for all other values they take on the default state (all 0). If the Option Key is 6, then the complete page 1 (i.e., option register and traceability data) cannot be overwritten by any Test Write command. Therefore, if the Lock bits of the three blocks of page 1 are set and the Option Key is 6, then all of page 1’s blocks are locked against change.

2. Weak field condition

2.2 **Configuration Register**

The ATA5577M3C offers three different modes of operation:
Basic mode is the default mode.

Table 2-1. Modes of Operation for the ATA5577M3C

<table>
<thead>
<tr>
<th>Mode of Operation</th>
<th>AFE Option Register (p1, bl3)</th>
<th>Configuration Register (p0, bl0)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Option Key (bit 1 to 4)</td>
<td>Q5 Mode (bit 23)</td>
</tr>
<tr>
<td>Basic mode</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>X-mode</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>Q5 Mode</td>
<td>= 0110 or 1001</td>
<td>1</td>
</tr>
</tbody>
</table>

2.2.1 Basic Mode

If bit 15 of the Configuration register block 0 page 0 is reset (‘0’) then the IC operates in Basic mode. Additionally, bit 23 in AFE Option register block 3 page 1 has to be reset (‘0’) (or the Option Key has to be unequal to ‘6’ or ‘9’).

Note: The configuration mapping in Basic mode is the same as it is in ATA5577M1/M2.

Figure 2-2. Block 0 Page 0 – Configuration Mapping in Basic Mode

Note:
1. If Master Key is 6, the Test mode access is disabled
2. If Master Key is neither 6 nor 9, the Extended Function mode and Init Delay are disabled
2.2.2 Extended Mode

If bit 15 of the Configuration register block 0 page 0 is set ('1') and Master Key = ‘6’ or ‘9’ then the IC operates in Extended mode. Additionally, bit 23 in AFE Option register block 3 page 1 has to be reset ('0') (or the Option Key has to be unequal to ‘6’ or ‘9’).

Note: The configuration mapping in X-mode is the same as it is in ATA5577M1/M2.

Figure 2-3. Block 0 Page 0 – Configuration Map in Extended Mode (X-mode)

![Extended Mode Configuration Map](image)

Note:
1. If Master Key is 6 and bit 15 is set, the Test mode access is disabled and the Extended mode is active
2. If Master Key is 9 and bit 15 is set, the Extended mode is enabled

2.2.3 Q5 Mode

If bit 23 in AFE Option Register block 3 page 1 is set ('1') and Option key is ‘6’ or ‘9’ then the IC operates in Q5 mode.

Figure 2-4. Block 0 Page 0 – Configuration Map in Q5 Mode

![Q5 Mode Configuration Map](image)

Note:
1. If Master Key is 6 the Test mode access is disabled
2. AOR, PWD and Fast Write are only enabled when Master Key is 6 or 9
2.3 Initialization

The Power-on-Reset (POR) circuit remains active until an adequate voltage threshold is reached. This, in turn, triggers the default initialization delay sequence. During this configuration period of 128 field clocks, the ATA5577M3C is initialized with the configuration data stored in EEPROM block 0, and with the AFE options stored in block 3 page 1. Modulation is switched off during initialization.

Any field gap which occurs during this initialization phase restarts the complete sequence. After this initialization time, the ATA5577M3C enters Regular-Read mode (if not programmed in AOR mode) and modulation starts automatically using the parameters defined in the Configuration and AFE Option register.

2.4 Functional Diagram

Figure 2-5. Functional Diagram

2.5 Capacitance

The ATA5577M3C offers 330pF of on-chip capacitance which are not trimmed during the production process.
Note: The tolerance of the on-chip resonance capacitor is ±15% over whole production. The capacitor tolerance is ±3% at 3σ on a wafer basis.

2.6 ATA5577M3C Delivery State Configuration

This section describes the memory content after production test.

Table 2-2. Delivery State for the ATA5577M3C

<table>
<thead>
<tr>
<th>Page</th>
<th>Block</th>
<th>(L) 32-bit Data</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>(0) 6001 F004</td>
<td>Manchester RF/64, Maxblock = 2</td>
</tr>
<tr>
<td>1</td>
<td>(0) FF8C A64A</td>
<td>Fixed ID</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>(0) 98F8 C802</td>
<td>Fixed ID</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>(0) 0000 0000</td>
<td>All ‘0’</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>(0) 0000 0000</td>
<td>All ‘0’</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>(0) 0000 0000</td>
<td>All ‘0’</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>(0) xxxx xxxx</td>
<td>Variable BCD coded LotID and Wafer#</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>(0) 0000 0000</td>
<td>All ‘0’</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>(L) FFxx xxxx</td>
<td>Traceability data according to Figure 2-2</td>
</tr>
<tr>
<td>2</td>
<td>(L) xxxx xxxx</td>
<td>Traceability data according to Figure 2-2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>(0) 65C0 0200</td>
<td>SM one pulse weak, Clamp Hi, Mod Lo, Q5 Mode</td>
<td></td>
</tr>
</tbody>
</table>

Note: (L) means Lock bit is set for that block.
3. Electrical Specifications

3.1 Absolute Maximum Ratings

Absolute maximum ratings for the ATA5577M3C are listed below.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum DC current into Coil1/Coil2</td>
<td>(I_{coil})</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td>Maximum AC current into Coil1/Coil2 (f = 125) kHz</td>
<td>(I_{coil\ p})</td>
<td>20</td>
<td>mA</td>
</tr>
<tr>
<td>Power dissipation (dice) (Free-Air condition, time of application: (1s))</td>
<td>(P_{tot})</td>
<td>100</td>
<td>mW</td>
</tr>
<tr>
<td>Electrostatic discharge maximum to ANSI/ESDSTM5.1-2001 standard (HBM)</td>
<td>(V_{max})</td>
<td>2000</td>
<td>V</td>
</tr>
<tr>
<td>Operating ambient temperature range</td>
<td>(T_{amb})</td>
<td>-40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature range (data retention reduced)</td>
<td>(T_{stg})</td>
<td>-40 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

**CAUTION** Stresses listed under **Absolute Maximum Ratings** may cause permanent damage to the device. This is a stress rating only. The functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect the device reliability.

3.2 Electrical Characteristics

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Test Conditions</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Type*</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF frequency</td>
<td></td>
<td>(f_{RF})</td>
<td>100</td>
<td>125</td>
<td>150</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Supply current (without current consumed by the external LC tank circuit)</td>
<td>(T_{amb} = 25^\circ)C(^{(1)})</td>
<td>(I_{DD})</td>
<td>—</td>
<td>1.5</td>
<td>3</td>
<td>(\mu)A</td>
<td>T</td>
</tr>
<tr>
<td>Read - full temperature range</td>
<td></td>
<td>—</td>
<td>—</td>
<td>2</td>
<td>5</td>
<td>(\mu)A</td>
<td>Q</td>
</tr>
<tr>
<td>Programming - full temperature range</td>
<td></td>
<td>—</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>(\mu)A</td>
<td>Q</td>
</tr>
</tbody>
</table>
### ATA5577M3C

#### Electrical Specifications

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Test Conditions</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Type*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coil voltage (AC supply)</td>
<td>POR threshold (50mV hysteresis)</td>
<td>$V_{\text{coil pp}}$</td>
<td>—</td>
<td>3.6</td>
<td>—</td>
<td>V</td>
<td>Q</td>
</tr>
<tr>
<td>Read mode and write command(2)</td>
<td></td>
<td>—</td>
<td>6</td>
<td>—</td>
<td>$V_{\text{clamp}}$</td>
<td>V</td>
<td>Q</td>
</tr>
<tr>
<td>Program EEPROM(2)</td>
<td></td>
<td>—</td>
<td>8</td>
<td>—</td>
<td>$V_{\text{clamp}}$</td>
<td>V</td>
<td>Q</td>
</tr>
<tr>
<td>Start-up time</td>
<td>$V_{\text{coil pp}} = 6V$</td>
<td>$t_{\text{startup}}$</td>
<td>—</td>
<td>2.5</td>
<td>—</td>
<td>ms</td>
<td>Q</td>
</tr>
<tr>
<td>Clamp voltage (depends on settings in option register)</td>
<td>3 mA current into Coil1/2</td>
<td>$V_{\text{pp clamp lo}}$</td>
<td>—</td>
<td>11</td>
<td>—</td>
<td>V</td>
<td>Q</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{pp clamp med}}$</td>
<td>—</td>
<td>13</td>
<td>—</td>
<td>V</td>
<td>Q</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{pp clamp hi}}$</td>
<td>14</td>
<td>17</td>
<td>21</td>
<td>V</td>
<td>T</td>
</tr>
<tr>
<td></td>
<td>20mA current into Coil1/2</td>
<td>$V_{\text{pp clamp med}}$</td>
<td>13</td>
<td>15</td>
<td>18</td>
<td>V</td>
<td>T</td>
</tr>
<tr>
<td>Modulation parameters (depends on settings in option register)</td>
<td>3mA current into Coil1/2 and modulation ON</td>
<td>$V_{\text{pp mod lo}}$</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>V</td>
<td>T</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{pp mod med}}$</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>V</td>
<td>Q</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{pp mod hi}}$</td>
<td>—</td>
<td>7</td>
<td>—</td>
<td>V</td>
<td>Q</td>
</tr>
<tr>
<td></td>
<td>20mA current into Coil1/2 and modulation ON</td>
<td>$V_{\text{pp mod med}}$</td>
<td>6</td>
<td>7.5</td>
<td>9</td>
<td>V</td>
<td>T</td>
</tr>
<tr>
<td>Thermal stability</td>
<td>$V_{\text{mod lo}/T_{\text{amb}}}$</td>
<td>—</td>
<td>—1</td>
<td>—</td>
<td>—</td>
<td>mV/°C</td>
<td>Q</td>
</tr>
<tr>
<td>Clock detection level (depends on settings in Option register)</td>
<td>$V_{\text{coil pp}} = 8V$</td>
<td>$V_{\text{clkdet lo}}$</td>
<td>—</td>
<td>250</td>
<td>—</td>
<td>mV</td>
<td>Q</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{clkdet med}}$</td>
<td>400</td>
<td>550</td>
<td>730</td>
<td>mV</td>
<td>T</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{clkdet hi}}$</td>
<td>—</td>
<td>800</td>
<td>—</td>
<td>mV</td>
<td>Q</td>
</tr>
<tr>
<td>Gap detection level (depends on settings in Option register)</td>
<td>$V_{\text{coil pp}} = 8V$</td>
<td>$V_{\text{gapdet lo}}$</td>
<td>—</td>
<td>250</td>
<td>—</td>
<td>mV</td>
<td>Q</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{gapdet med}}$</td>
<td>400</td>
<td>550</td>
<td>730</td>
<td>mV</td>
<td>T</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{gapdet hi}}$</td>
<td>—</td>
<td>850</td>
<td>—</td>
<td>mV</td>
<td>Q</td>
</tr>
<tr>
<td>Parameters</td>
<td>Test Conditions</td>
<td>Symbol</td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
<td>Unit</td>
<td>Type*</td>
</tr>
<tr>
<td>-----------------------------</td>
<td>---------------------------------------------------------------------------------</td>
<td>--------</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
</tr>
<tr>
<td>Programming time</td>
<td>From last command gap to re-enter Read mode (64 + 648 internal clocks)</td>
<td>Tprog</td>
<td>5</td>
<td>5.7</td>
<td>6</td>
<td>ms</td>
<td>T</td>
</tr>
<tr>
<td>Endurance</td>
<td>Erase all/Write all(^{(3)})</td>
<td>n_cycle</td>
<td>100000</td>
<td>—</td>
<td>—</td>
<td>Cycles</td>
<td>Q</td>
</tr>
<tr>
<td>Data retention</td>
<td>Top = 55°C(^{(3)})</td>
<td>t_retention</td>
<td>10</td>
<td>20</td>
<td>50</td>
<td>Years</td>
<td>Q</td>
</tr>
<tr>
<td></td>
<td>Top = 150°C(^{(3)})</td>
<td>t_retention</td>
<td>96</td>
<td>—</td>
<td>—</td>
<td>hrs</td>
<td>T</td>
</tr>
<tr>
<td></td>
<td>Top = 250°C(^{(3)})</td>
<td>t_retention</td>
<td>24</td>
<td>—</td>
<td>—</td>
<td>hrs</td>
<td>Q</td>
</tr>
<tr>
<td>Resonance capacitor(^{(4)})</td>
<td>Mask option(^{(5)}) (V_{coil_{pp}} = 1\text{V})</td>
<td>(C_r)</td>
<td>280</td>
<td>330</td>
<td>380</td>
<td>pF</td>
<td>T</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>179</td>
<td>210</td>
<td>241</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>68</td>
<td>80</td>
<td>92</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*) Type means: T = directly or indirectly tested during production; Q: ensured based on initial product qualification data

**Note:**

1. IDD measurement setup: EEPROM programmed to 00 ... 000 (erase all); chip in modulation defeat.
2. Current into Coil1/Coil2 is limited to 10mA.
3. Since EEPROM performance is influenced by assembly processes, Microchip cannot confirm the parameters for -DDW (tested die on unsawn wafer) delivery.
4. The tolerance of the on-chip resonance capacitor is ±15% over whole production. The capacitor tolerance is ±3% at 3σ on a wafer basis.
5. See ordering information.
4. Ordering Information

Following table describes the ordering details for the ATA5577M3C modules.

Table 4-1. Ordering Details

<table>
<thead>
<tr>
<th>Model Number/Order Codes</th>
<th>On-Chip Capacity</th>
<th>Description</th>
<th>Package Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATA5577M3330C-DDB</td>
<td>330pF</td>
<td>6” sawn wafer on foil with ring, thickness 150µm (approx. 6 mil)</td>
<td>Figure 5-1</td>
</tr>
<tr>
<td>ATA5577M3330C-DBB</td>
<td>330pF</td>
<td><strong>Available on request</strong> 6” sawn wafer on foil with ring, thickness 285µm (approx. 11mil) plus gold bumps 25µm</td>
<td>—</td>
</tr>
<tr>
<td>ATA5577M3330C-DBQ</td>
<td>330pF</td>
<td>Die in blister tape, thickness 280µm (approx. 11mil) plus gold bumps 25µm</td>
<td>Figure 5-2</td>
</tr>
<tr>
<td>ATA5577M3330C-DUQW</td>
<td>330pF</td>
<td>Die in blister tape, thickness 150µm (approx. 6mil) plus gold bumps 25µm</td>
<td>Figure 5-3</td>
</tr>
<tr>
<td>ATA5577M3331C-DBB</td>
<td>330pF</td>
<td>6” sawn wafer on foil with ring, thickness 150µm (approx. 6mil) plus gold bumps 25µm</td>
<td>Figure 5-4</td>
</tr>
</tbody>
</table>
5. **Package Information**

Figure 5-1. Microchip ATA5577M3xxxC-DDB 150µm

Die Dimensions
20:1

Dimensions in mm

Orientation on frame

Option
xxx
330

Label:
Prod: ATA5577M3xxxC-DDB
Plot no:
Wafer no:
Qty:

Wafer ATA5577M3xxxC-DDB
UV Tape Adwill D176
6" Wafer frame, plastic thickness 2.5mm
Figure 5-2. Microchip ATA5577M3xxxC-DBQ with Gold Bumps

Die Dimensions
20:1

technical drawings according to DIN specifications

Label acc. "Packaging and Packing Spec."

cover tape

carrier tape

"X"

reel Ø330

Option xxx
330

Option

0.5

1.52

1.3
Figure 5-3. Microchip ATA5577M3xxx-C-DUQW with Gold Bumps

Die Dimensions
20:1

technical drawings according to DIN specifications

Die Dimension (0.08)

0.177±0.015

0.04×45°

0.2

0.324

Packing acc. IEC 60286-3

ATA5577M3330C-DUQW
Specification Tape and reel
Dimensions in mm

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Datasheet

DS70005396A-page 17
Figure 5-4. Microchip ATA5577M3xxxC-DBB 150µm

Die Dimensions
20:1

Dimensions in mm

Orientation on frame

Option
xxx
330

Label:
Prod: ATA5577M3xxxC-DBB
Lot no:
Wafer no:
Qty:

Wafer ATA5577M3xxxC-DBB
UV Tape Adwill D176
6" Wafer frame, plastic thickness 2.5mm
### Document Revision History

#### Table 6-1. Document Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Section</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>05/2019</td>
<td>Document</td>
<td>Initial Revision</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Updated from Atmel to Microchip template</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Assigned a new Microchip document number. Previous version is 9188C–RFID–</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>07/14.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Added new part ATA5577M3330C-DUQW.</td>
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</table>

#### Table 6-2. Atmel Revision History

<table>
<thead>
<tr>
<th>Revision No.</th>
<th>History</th>
</tr>
</thead>
<tbody>
<tr>
<td>9188C-RFID-07/14</td>
<td>• Section 8 “Ordering Information” on page 11 updated</td>
</tr>
<tr>
<td></td>
<td>• Section 10 “Package Information” on pages 13 to 14 updated</td>
</tr>
<tr>
<td>9188B-RFID-07/12</td>
<td>• Section 7 “Electrical Characteristics” Note 4 on pages 9 to 10 changed</td>
</tr>
</tbody>
</table>
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