AT24CM01

I²C-Compatible (Two-Wire)
Serial EEPROM 1-Mbit (131,072 x 8)

Features

• Low-Voltage and Standard Voltage Operation:
  – \( V_{CC} = 1.7\text{V} \) to 5.5V
  – \( V_{CC} = 2.5\text{V} \) to 5.5V
• Internally Organized as 131,072 x 8 (1M)
• Industrial Temperature Range: -40°C to +85°C
• I²C-Compatible (Two-Wire) Serial Interface:
  – 100 kHz Standard mode, 1.7V to 5.5V
  – 400 kHz Fast mode, 1.7V to 5.5V
  – 1 MHz Fast Mode Plus (FM+), 2.5V to 5.5V
• Schmitt Triggers, Filtered Inputs for Noise Suppression
• Bidirectional Data Transfer Protocol
• Write-Protect Pin for Full Array Hardware Data Protection
• Ultra Low Active Current (3 mA maximum) and Standby Current (6 µA maximum)
• 256-byte Page Write Mode:
  – Byte write and partial page writes allowed
• Random and Sequential Read Modes
• Self-Timed Write Cycle:
  – All Write operations complete within 5 ms maximum
• Built in Error Detection and Correction
• High Reliability:
  – Endurance: 1,000,000 write cycles
  – Data retention: 100 years
• Green Package Options (Lead-free/Halide-free/RoHS compliant)
• Die Sale Options: Wafer Form and Bumped Wafers

Packages

• 8-Lead SOIC, 8-Lead SOIJ, 8-Lead TSSOP and 8-Ball WLCSP
# Table of Contents

Features.......................................................................................................................... 1

Packages......................................................................................................................... 1

1. Package Types (not to scale).................................................................................... 4

2. Pin Descriptions......................................................................................................... 5
   2.1. Device Address Inputs (A1, A2).............................................................................. 5
   2.2. Ground................................................................................................................... 5
   2.3. Serial Data (SDA).................................................................................................. 5
   2.4. Serial Clock (SCL)................................................................................................ 5
   2.5. Write-Protect (WP).............................................................................................. 6
   2.6. Device Power Supply............................................................................................ 6

3. Description................................................................................................................. 7
   3.1. System Configuration Using Two-Wire Serial EEPROMs................................. 7
   3.2. Block Diagram...................................................................................................... 8

4. Electrical Characteristics........................................................................................... 9
   4.1. Absolute Maximum Ratings................................................................................ 9
   4.2. DC and AC Operating Range.............................................................................. 9
   4.3. DC Characteristics.............................................................................................. 9
   4.4. AC Characteristics............................................................................................ 10
   4.5. Electrical Specifications...................................................................................... 11

5. Device Operation and Communication.................................................................... 13
   5.1. Clock and Data Transition Requirements............................................................ 13
   5.2. Start and Stop Conditions................................................................................... 13
   5.3. Acknowledge and No-Acknowledge................................................................... 14
   5.4. Standby Mode..................................................................................................... 14
   5.5. Software Reset................................................................................................... 15

6. Memory Organization.............................................................................................. 16
   6.1. Device Addressing.............................................................................................. 16

7. Write Operations....................................................................................................... 18
   7.1. Byte Write........................................................................................................... 18
   7.2. Page Write........................................................................................................... 18
   7.3. Acknowledge Polling.......................................................................................... 19
   7.4. Write Cycle Timing............................................................................................. 20
   7.5. Write Protection................................................................................................. 20

8. Read Operations....................................................................................................... 21
   8.1. Current Address Read......................................................................................... 21
   8.2. Random Read.................................................................................................... 21
1. **Package Types (not to scale)**

**8-Lead SOIC/SOIJ/TSSOP**
(Top View)

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>NC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V&lt;sub&gt;CC&lt;/sub&gt;</td>
</tr>
<tr>
<td>A1</td>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>WP</td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SCL</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>SDA</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>

**8-Ball WLCSP**
(Top View)

- V<sub>CC</sub>
- WP
- NC
- SCL
- A<sub>1</sub>
- SDA
- A<sub>2</sub>
- GND
2. Pin Descriptions

The descriptions of the pins are listed in Table 2-1.

Table 2-1. Pin Function Table

<table>
<thead>
<tr>
<th>Name</th>
<th>8-Lead SOIC</th>
<th>8-Pad SOJ</th>
<th>8-Lead TSSOP</th>
<th>8-Ball WLCSP</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>NC</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>E1</td>
<td>Not Connected</td>
</tr>
<tr>
<td>A1(1)</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>D2</td>
<td>Device Address Input</td>
</tr>
<tr>
<td>A2(1)</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>C3</td>
<td>Device Address Input</td>
</tr>
<tr>
<td>GND</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>E3</td>
<td>Ground</td>
</tr>
<tr>
<td>SDA</td>
<td>5</td>
<td>5</td>
<td>5</td>
<td>A3</td>
<td>Serial Data</td>
</tr>
<tr>
<td>SCL</td>
<td>6</td>
<td>6</td>
<td>6</td>
<td>B2</td>
<td>Serial Data</td>
</tr>
<tr>
<td>WP(1)</td>
<td>7</td>
<td>7</td>
<td>7</td>
<td>C1</td>
<td>Write-Protect</td>
</tr>
<tr>
<td>VCC</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>A1</td>
<td>Device Power Supply</td>
</tr>
</tbody>
</table>

Note:
1. If the A2, A1 or WP pins are not driven, they are internally pulled down to GND. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once these pins are biased above the CMOS input buffer’s trip point (~0.5 x VCC), the pull-down mechanism disengages. Microchip recommends connecting these pins to a known state whenever possible.

2.1 Device Address Inputs (A1, A2)

The A1 and A2 pins are device address inputs that are hardwired (directly to GND or to VCC) for compatibility with other two-wire Serial EEPROM devices. When the pins are hardwired, as many as four devices may be addressed on a single bus system. A device is selected when a corresponding hardware and software match is true. If these pins are left floating, the A1 and A2 pins will be internally pulled down to GND. However, due to capacitive coupling that may appear in customer applications, Microchip recommends always connecting the address pins to a known state. When using a pull-up resistor, Microchip recommends using 10 kΩ or less.

2.2 Ground

The ground reference for the power supply. GND should be connected to the system ground.

2.3 Serial Data (SDA)

The SDA pin is an open-drain bidirectional input/output pin used to serially transfer data to and from the device. The SDA pin must be pulled high using an external pull-up resistor (not to exceed 10 kΩ in value) and may be wire-ORed with any number of other open-drain or open-collector pins from other devices on the same bus.

2.4 Serial Clock (SCL)

The SCL pin is used to provide a clock to the device and to control the flow of data to and from the device. Command and input data present on the SDA pin is always latched in on the rising edge of SCL, while output data on the SDA pin is clocked out on the falling edge of SCL. The SCL pin must either be forced high when the serial bus is idle or pulled high using an external pull-up resistor.
2.5 Write-Protect (WP)

The write-protect input, when connected to GND, allows normal write operations. When the WP pin is connected directly to $V_{CC}$, all write operations to the protected memory are inhibited.

If the pin is left floating, the WP pin will be internally pulled down to GND. However, due to capacitive coupling that may appear in customer applications, Microchip recommends always connecting the WP pin to a known state. When using a pull-up resistor, Microchip recommends using 10 kΩ or less.

Table 2-2. Write-Protect

<table>
<thead>
<tr>
<th>WP Pin Status</th>
<th>Part of the Array Protected</th>
</tr>
</thead>
<tbody>
<tr>
<td>At $V_{CC}$</td>
<td>Full Array</td>
</tr>
<tr>
<td>At GND</td>
<td>Normal Write Operations</td>
</tr>
</tbody>
</table>

2.6 Device Power Supply

The $V_{CC}$ pin is used to supply the source voltage to the device. Operations at invalid $V_{CC}$ voltages may produce spurious results and should not be attempted.
3. **Description**

The AT24CM01 provides 1,048,576 bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 131,072 words of eight bits each. The device's cascading feature allows up to four devices to share a common two-wire bus. This device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential. The device is available in space-saving 8-lead SOIC, 8-Lead TSSOP, 8-Lead SOIJ and 8-ball WLCSP packages. All packages operate from 1.7V to 5.5V.

3.1 **System Configuration Using Two-Wire Serial EEPROMs**
3.2 Block Diagram
4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Temperature under bias: -55°C to +125°C
Storage temperature: -65°C to +150°C
$V_{CC}$: 6.25 V
Voltage on any pin with respect to ground: -1.0 V to +7.0 V
DC output current: 5.0 mA
ESD protection: >3 kV

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 DC and AC Operating Range

Table 4-1. DC and AC Operating Range

<table>
<thead>
<tr>
<th>AT24CM01</th>
<th>Operating Temperature (Case)</th>
<th>Industrial Temperature Range</th>
<th>-40°C to +85°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$ Power Supply</td>
<td>Low-Voltage Grade</td>
<td>1.7V to 5.5V</td>
<td></td>
</tr>
</tbody>
</table>

4.3 DC Characteristics

Table 4-2. DC Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Minimum</th>
<th>Typical(1)</th>
<th>Maximum</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, 1.7V Option</td>
<td>$V_{CC1}$</td>
<td>1.7</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>$V_{CC}$ = 5.0V, Read at 400 kHz</td>
</tr>
<tr>
<td>Supply Voltage, 2.5V Option</td>
<td>$V_{CC2}$</td>
<td>2.5</td>
<td>—</td>
<td>5.5</td>
<td>V</td>
<td>$V_{CC}$ = 5.0V, Read at 400 kHz</td>
</tr>
<tr>
<td>Supply Current</td>
<td>$I_{CC}$</td>
<td>—</td>
<td>—</td>
<td>2.0</td>
<td>mA</td>
<td>$V_{CC}$ = 5.0V, Write at 400 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>3.0</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

(1) Manufacturer recommends $V_{CC} = 5.0$ V but device operates from 1.7 V to 5.5 V.
### Electrical Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Minimum</th>
<th>Typical&lt;sup&gt;(1)&lt;/sup&gt;</th>
<th>Maximum</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standby Current</td>
<td>I&lt;sub&gt;SB&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>1.0</td>
<td>μA</td>
<td>(V_{CC} = 1.7\text{V}, V_{IN} = V_{CC}) or (V_{SS})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>2.0</td>
<td>μA</td>
<td>(V_{CC} = 2.5\text{V}, V_{IN} = V_{CC}) or (V_{SS})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>3.0</td>
<td>μA</td>
<td>(V_{CC} = 3.6\text{V}, V_{IN} = V_{CC}) or (V_{SS})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>—</td>
<td>6.0</td>
<td>μA</td>
<td>(V_{CC} = 5.5\text{V}, V_{IN} = V_{CC}) or (V_{SS})</td>
</tr>
<tr>
<td>Input Leakage Current</td>
<td>I&lt;sub&gt;LI&lt;/sub&gt;</td>
<td>—</td>
<td>0.10</td>
<td>3.0</td>
<td>μA</td>
<td>(V_{IN} = V_{CC}) or (V_{SS})</td>
</tr>
<tr>
<td>Output Leakage Current</td>
<td>I&lt;sub&gt;LO&lt;/sub&gt;</td>
<td>—</td>
<td>0.05</td>
<td>3.0</td>
<td>μA</td>
<td>(V_{OUT} = V_{CC}) or (V_{SS})</td>
</tr>
<tr>
<td>Input Low Level</td>
<td>V&lt;sub&gt;IL&lt;/sub&gt;</td>
<td>-0.6</td>
<td>—</td>
<td>(V_{CC} \times 0.3)</td>
<td>V</td>
<td>Note 2</td>
</tr>
<tr>
<td>Input High Level</td>
<td>V&lt;sub&gt;IH&lt;/sub&gt;</td>
<td>(V_{CC} \times 0.7)</td>
<td>—</td>
<td>(V_{CC} + 0.5)</td>
<td>V</td>
<td>Note 2</td>
</tr>
<tr>
<td>Output Low Level</td>
<td>V&lt;sub&gt;OL1&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>0.2</td>
<td>V</td>
<td>(V_{CC} = 1.7\text{V}, I_{OL} = 0.15\text{mA})</td>
</tr>
<tr>
<td>Output Low Level</td>
<td>V&lt;sub&gt;OL2&lt;/sub&gt;</td>
<td>—</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
<td>(V_{CC} = 3.0\text{V}, I_{OL} = 2.1\text{mA})</td>
</tr>
</tbody>
</table>

**Note:**

1. Typical values characterized at \(T_{A} = +25°C\) unless otherwise noted.
2. This parameter is characterized but is not 100% tested in production.

### 4.4 AC Characteristics

**Table 4-3. AC Characteristics<sup>(1)</sup>**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>(V_{CC} = 1.7\text{V} \text{ to } 5.5\text{V})</th>
<th>(V_{CC} = 2.5\text{V} \text{ to } 5.5\text{V})</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Frequency, SCL</td>
<td>(f_{SCL})</td>
<td>Min. 400 Max. 1000 kHz</td>
<td>Min. 500 Max. 450 ns</td>
<td>kHz</td>
</tr>
<tr>
<td>Clock Pulse Width Low</td>
<td>(t_{LOW})</td>
<td>1,300</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Clock Pulse Width High</td>
<td>(t_{HIGH})</td>
<td>600</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Input Filter Spike Suppression (SCL,SDA)&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>(t_{I})</td>
<td>100</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Clock Low to Data Out Valid</td>
<td>(t_{AA})</td>
<td>50</td>
<td>900</td>
<td>ns</td>
</tr>
<tr>
<td>Bus Free Time between Stop and Start&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>(t_{BUF})</td>
<td>1,300</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Start Hold Time</td>
<td>(t_{HD,STA})</td>
<td>600</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Start Set-up Time</td>
<td>(t_{SU,STA})</td>
<td>600</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Fast Mode</td>
<td>Fast Mode Plus</td>
<td>Units</td>
</tr>
<tr>
<td>---------------------------</td>
<td>--------</td>
<td>-----------</td>
<td>----------------</td>
<td>-------</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC}$ = 1.7V to 5.5V</td>
<td>$V_{CC}$ = 2.5V to 5.5V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td>Data In Hold Time</td>
<td>$t_{HD, DAT}$</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>Data In Set-up Time</td>
<td>$t_{SU, DAT}$</td>
<td>100</td>
<td>100</td>
<td>ns</td>
</tr>
<tr>
<td>Inputs Rise Time$^{(2)}$</td>
<td>$t_{R}$</td>
<td>—</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>Inputs Fall Time$^{(2)}$</td>
<td>$t_{F}$</td>
<td>—</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>Stop Condition Set-up Time</td>
<td>$t_{SU, STO}$</td>
<td>600</td>
<td>250</td>
<td>ns</td>
</tr>
<tr>
<td>Data Out Hold Time</td>
<td>$t_{DH}$</td>
<td>50</td>
<td>50</td>
<td>ns</td>
</tr>
<tr>
<td>Write Cycle Time</td>
<td>$t_{WR}$</td>
<td>—</td>
<td>5</td>
<td>ms</td>
</tr>
</tbody>
</table>

Note:
1. AC measurement conditions:
   - $C_L$: 100 pF
   - $R_{PUP}$ (SDA bus line pull-up resistor to $V_{CC}$): 1.3 kΩ (1000 kHz), 4 kΩ (400 kHz)
   - Input pulse voltages: $0.3 \times V_{CC}$ to $0.7 \times V_{CC}$
   - Input rise and fall times: $\leq 50$ ns
   - Input and output timing reference voltages: $0.5 \times V_{CC}$
2. These parameters are determined through product characterization and are not 100% tested in production.

Figure 4-1. Bus Timing

4.5 Electrical Specifications

4.5.1 Power-Up Requirements and Reset Behavior
During a power-up sequence, the $V_{CC}$ supplied to the AT24CM01 should monotonically rise from GND to the minimum $V_{CC}$ level, as specified in Table 4-1, with a slew rate no faster than 0.1 V/µs.

4.5.1.1 Device Reset
To prevent inadvertent write operations or any other spurious events from occurring during a power-up sequence, the AT24CM01 includes a Power-on Reset (POR) circuit. Upon power-up, the device will not
respond to any commands until the $V_{CC}$ level crosses the internal voltage threshold ($V_{POR}$) that brings the device out of Reset and into Standby mode.

The system designer must ensure the instructions are not sent to the device until the $V_{CC}$ supply has reached a stable value greater than or equal to the minimum $V_{CC}$ level. Additionally, once the $V_{CC}$ is greater than or equal to the minimum $V_{CC}$ level, the bus master must wait at least $t_{PUP}$ before sending the first command to the device. See Table 4-4 for the values associated with these power-up parameters.

**Table 4-4. Power-Up Conditions**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PUP}$</td>
<td>Time required after $V_{CC}$ is stable before the device can accept commands</td>
<td>100</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td>$V_{POR}$</td>
<td>Power-on Reset Threshold Voltage</td>
<td>—</td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>$t_{POFF}$</td>
<td>Minimum time at $V_{CC} = 0V$ between power cycles</td>
<td>500</td>
<td>—</td>
<td>ms</td>
</tr>
</tbody>
</table>

**Note:**

1. These parameters are characterized but they are not 100% tested in production.

If an event occurs in the system where the $V_{CC}$ level supplied to the AT24CM01 drops below the maximum $V_{POR}$ level specified, it is recommended that a full-power cycle sequence be performed by first driving the $V_{CC}$ pin to GND, waiting at least the minimum $t_{POFF}$ time and then performing a new power-up sequence in compliance with the requirements defined in this section.

### 4.5.2 Pin Capacitance

**Table 4-5. Pin Capacitance**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Test Condition</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{I/O}$</td>
<td>Input/Output Capacitance (SDA)</td>
<td>8</td>
<td>pF</td>
<td>$V_{I/O} = 0V$</td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance (A0, A1, A2 and SCL)</td>
<td>6</td>
<td>pF</td>
<td>$V_{IN} = 0V$</td>
</tr>
</tbody>
</table>

**Note:**

1. This parameter is characterized but is not 100% tested in production.

### 4.5.3 EEPROM Cell Performance Characteristics

**Table 4-6. EEPROM Cell Performance Characteristics**

<table>
<thead>
<tr>
<th>Operation</th>
<th>Test Condition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write Endurance$^{(1)}$</td>
<td>$T_A = 25^\circ C$, $V_{CC} = 3.3V$, Page Write mode</td>
<td>1,000,000</td>
<td>—</td>
<td>Write Cycles</td>
</tr>
<tr>
<td>Data Retention$^{(1)}$</td>
<td>$T_A = 55^\circ C$</td>
<td>100</td>
<td>—</td>
<td>Years</td>
</tr>
</tbody>
</table>

**Note:**

1. Performance is determined through characterization and the qualification process.
5. **Device Operation and Communication**

The AT24CM01 operates as a slave device and utilizes a simple I^2^C-compatible two-wire digital serial interface to communicate with a host controller, commonly referred to as the bus master. The master initiates and controls all read and write operations to the slave devices on the serial bus, and both the master and the slave devices can transmit and receive data on the bus.

The serial interface is comprised of just two signal lines: Serial Clock (SCL) and Serial Data (SDA). The SCL pin is used to receive the clock signal from the master, while the bidirectional SDA pin is used to receive command and data information from the master as well as to send data back to the master. Data is always latched into the AT24CM01 on the rising edge of SCL and always output from the device on the falling edge of SCL. Both the SCL and SDA pins incorporate integrated spike suppression filters and Schmitt Triggers to minimize the effects of input spikes and bus noise.

All command and data information is transferred with the Most Significant bit (MSb) first. During bus communication, one data bit is transmitted every clock cycle, and after eight bits (one byte) of data have been transferred, the receiving device must respond with either an Acknowledge (ACK) or a No-Acknowledge (NACK) response bit during a ninth clock cycle (ACK/NACK clock cycle) generated by the master. Therefore, nine clock cycles are required for every one byte of data transferred. There are no unused clock cycles during any read or write operation, so there must not be any interruptions or breaks in the data stream during each data byte transfer and ACK or NACK clock cycle.

During data transfers, data on the SDA pin must only change while SCL is low, and the data must remain stable while SCL is high. If data on the SDA pin changes while SCL is high, then either a Start or a Stop condition will occur. Start and Stop conditions are used to initiate and end all serial bus communication between the master and the slave devices. The number of data bytes transferred between a Start and a Stop condition is not limited and is determined by the master. In order for the serial bus to be idle, both the SCL and SDA pins must be in the logic high state at the same time.

5.1 **Clock and Data Transition Requirements**

The SDA pin is an open-drain terminal and therefore must be pulled high with an external pull-up resistor. SCL is an input pin that can either be driven high or pulled high using an external pull-up resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a Start or Stop condition as defined below. The relationship of the AC timing parameters with respect to SCL and SDA for the AT24CM01 are shown in the timing waveform in Figure 4-1. The AC timing characteristics and specifications are outlined in AC Characteristics.

5.2 **Start and Stop Conditions**

5.2.1 **Start Condition**

A Start condition occurs when there is a high-to-low transition on the SDA pin while the SCL pin is at a stable logic ‘1’ state and will bring the device out of Standby mode. The master uses a Start condition to initiate any data transfer sequence; therefore, every command must begin with a Start condition. The device will continuously monitor the SDA and SCL pins for a Start condition but will not respond unless one is detected. Refer to Figure 5-1 for more details.

5.2.2 **Stop Condition**

A Stop condition occurs when there is a low-to-high transition on the SDA pin while the SCL pin is stable in the logic ‘1’ state.
The master can use the Stop condition to end a data transfer sequence with the AT24CM01, which will subsequently return to Standby mode. The master can also utilize a repeated Start condition instead of a Stop condition to end the current data transfer if the master will perform another operation. Refer to Figure 5-1 for more details.

5.3 Acknowledge and No-Acknowledge

After every byte of data is received, the receiving device must confirm to the transmitting device that it has successfully received the data byte by responding with what is known as an Acknowledge (ACK). An ACK is accomplished by the transmitting device first releasing the SDA line at the falling edge of the eighth clock cycle followed by the receiving device responding with a logic ‘0’ during the entire high period of the ninth clock cycle.

When the AT24CM01 is transmitting data to the master, the master can indicate that it is done receiving data and wants to end the operation by sending a logic ‘1’ response to the AT24CM01 instead of an ACK response during the ninth clock cycle. This is known as a No-Acknowledge (NACK) and is accomplished by the master sending a logic ‘1’ during the ninth clock cycle, at which point the AT24CM01 will release the SDA line so the master can then generate a Stop condition.

The transmitting device, which can be the bus master or the Serial EEPROM, must release the SDA line at the falling edge of the eighth clock cycle to allow the receiving device to drive the SDA line to a logic ‘0’ to ACK the previous 8-bit word. The receiving device must release the SDA line at the end of the ninth clock cycle to allow the transmitter to continue sending new data. A timing diagram has been provided in Figure 5-1 to better illustrate these requirements.

Figure 5-1. Start Condition, Data Transitions, Stop Condition and Acknowledge

5.4 Standby Mode

The AT24CM01 features a low-power Standby mode that is enabled when any one of the following occurs:

- A valid power-up sequence is performed (see Power-Up Requirements and Reset Behavior).
- A Stop condition is received by the device unless it initiates an internal write cycle (see Write Operations).
- At the completion of an internal write cycle (see Write Operations).
5.5 Software Reset

After an interruption in protocol, power loss or system Reset, any two-wire device can be protocol reset by clocking SCL until SDA is released by the EEPROM and goes high. The number of clock cycles until SDA is released by the EEPROM will vary. The software Reset sequence should not take more than nine dummy clock cycles. Once the software Reset sequence is complete, new protocol can be sent to the device by sending a Start condition followed by the protocol. Refer to Figure 5-2 for an illustration.

Figure 5-2. Software Reset

In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device (see Power-Up Requirements and Reset Behavior).
6. Memory Organization
The AT24CM01 is internally organized as 512 pages of 256 bytes each.

6.1 Device Addressing
Accessing the device requires an 8-bit device address byte following a Start condition to enable the device for a read or write operation. Since multiple slave devices can reside on the serial bus, each slave device must have its own unique address so the master can access each device independently.

The Most Significant four bits of the device address byte is referred to as the device type identifier. The device type identifier '1010' (Ah) is required in bits 7 through 4 of the device address byte (see Table 6-1).

Following the 4-bit device type identifier are the hardware slave address bits, A2 and A1. These bits can be used to expand the address space by allowing up to four Serial EEPROM devices on the same bus. The A2 and A1 values must correlate with the voltage level on the corresponding hardwired device address input pins A2 and A1. The A2 and A1 pins use an internal proprietary circuit that automatically biases it to a logic '0' state if the pin is allowed to float. In order to operate in a wide variety of application environments, the pull-down mechanism is intentionally designed to be somewhat strong. Once these pins are biased above the CMOS input buffer’s trip point (~0.5 x VCC), the pull-down mechanism disengages. Microchip recommends connecting the A2 and A1 pin to a known state whenever possible.

Following the A2 and A1 hardware slave address bits is bit A16 (bit 1 of the device address byte), which is the Most Significant bit of the memory array word address. Refer to Table 6-1 to review the bit position.

The eighth bit (bit 0) of the device address byte is the Read/Write Select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon the successful comparison of the device address byte, the AT24CM01 will return an ACK. If a valid comparison is not made, the device will NACK.

Table 6-1. Device Addressing

<table>
<thead>
<tr>
<th>Package</th>
<th>Device Type Identifier</th>
<th>Hardware Slave Address Bits</th>
<th>Most Significant Bit of the Word Address</th>
<th>R/W Select</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit 7 Bit 6 Bit 5 Bit 4</td>
<td>Bit 3 Bit 2 Bit 1 Bit 0</td>
<td>A2 A1 A16 R/W</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SOIC, SOIJ, TSSOP, WLCSP</td>
<td>1 0 1 0 A2 A1 A16 R/W</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

For all operations except the current address read, two 8-bit word address bytes must be transmitted to the device immediately following the device address byte. The word address bytes consist of the remaining 16 bits of the 17-bit memory array word address, and are used to specify which byte location in the EEPROM to start reading or writing.

The first word address byte contains the next eight bits of the word address (A15 through A8) in bit positions seven through zero, as seen in Table 6-2. Upon completion of the first word address byte, the AT24CM01 will return an ACK.
Table 6-2. First Word Address Byte

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>A15</td>
<td>A14</td>
<td>A13</td>
<td>A12</td>
<td>A11</td>
<td>A10</td>
<td>A9</td>
<td>A8</td>
</tr>
</tbody>
</table>

Next, the second word address byte is sent to the device which provides the remaining eight bits of the word address (A7 through A0). Upon completion of the second word address byte, the AT24CM01 will return an ACK. See Table 6-3 to review these bit positions.

Table 6-3. Second Word Address Byte

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>A7</td>
<td>A6</td>
<td>A5</td>
<td>A4</td>
<td>A3</td>
<td>A2</td>
<td>A1</td>
<td>A0</td>
</tr>
</tbody>
</table>
7. Write Operations

All write operations for the AT24CM01 begin with the master sending a Start condition, followed by a device address byte with the R/W bit set to logic ‘0’, and then by the word address byte. The data value(s) to be written to the device immediately follow the word address byte.

7.1 Byte Write

The AT24CM01 supports the writing of a single 8-bit byte. Selecting a data word in the AT24CM01 requires 17-bit word address.

Upon receipt of the proper device address and the word address bytes, the EEPROM will send an Acknowledge. The device will then be ready to receive the 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will respond with an ACK. The addressing device, such as a bus master, must then terminate the write operation with a Stop condition. At that time, the EEPROM will enter an internally self-timed write cycle, which will be completed within tWR, while the data word is being programmed into the nonvolatile EEPROM. All inputs are disabled during this write cycle, and the EEPROM will not respond until the write is complete.

Figure 7-1. Byte Write

7.2 Page Write

A page write operation allows up to 256 bytes to be written in the same write cycle, provided all bytes are in the same row of the memory array (where address bits A16 through A8 are the same). Partial page writes of less than 256 bytes are also allowed.

A page write is initiated the same way as a byte write, but the bus master does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the bus master can transmit up to 255 additional data words. The EEPROM will respond with an ACK after each data word is received. Once all data to be written has been sent to the device, the bus master must issue a Stop condition (see Figure 7-2) at which time the internally self-timed write cycle will begin.

The lower eight bits of the word address are internally incremented following the receipt of each data word. The higher order address bits are not incremented and retain the memory page row location. Page
Write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. When the incremented word address reaches the page boundary, the address counter will rollover to the beginning of the same page. Nevertheless, creating a rollover event should be avoided as previously loaded data in the page could become unintentionally altered.

Figure 7-2. Page Write

7.3 Acknowledge Polling

An Acknowledge Polling routine can be implemented to optimize time-sensitive applications that would prefer not to wait the fixed maximum write cycle time ($t_{WR}$). This method allows the application to know immediately when the Serial EEPROM write cycle has completed, so a subsequent operation can be started.

Once the internally self-timed write cycle has started, an Acknowledge Polling routine can be initiated. This involves repeatedly sending a Start condition followed by a valid device address byte with the R/W bit set at logic ‘0’. The device will not respond with an ACK while the write cycle is ongoing. Once the internal write cycle has completed, the EEPROM will respond with an ACK, allowing a new read or write operation to be immediately initiated. A flowchart has been included below in Figure 7-3 to better illustrate this technique.

Figure 7-3. Acknowledge Polling Flowchart
7.4 Write Cycle Timing

The length of the self-timed write cycle ($t_{WR}$) is defined as the amount of time from the Stop condition that begins the internal write cycle to the Start condition of the first device address byte sent to the AT24CM01 that it subsequently responds to with an ACK. Figure 7-4 has been included to show this measurement. During the internally self-timed write cycle, any attempts to read from or write to the memory array will not be processed.

**Figure 7-4. Write Cycle Timing**

7.5 Write Protection

The AT24CM01 utilizes a hardware data protection scheme that allows the user to write-protect the entire memory contents when the WP pin is at $V_{CC}$ (or a valid $V_{IH}$). No write protection will be set if the WP pin is at GND or left floating.

**Table 7-1. AT24CM01 Write-Protect Behavior**

<table>
<thead>
<tr>
<th>WP Pin Voltage</th>
<th>Part of the Array Protected</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Full Array</td>
</tr>
<tr>
<td>GND</td>
<td>None — Write Protection Not Enabled</td>
</tr>
</tbody>
</table>

The status of the WP pin is sampled at the Stop condition for every byte write or page write operation prior to the start of an internally self-timed write cycle. Changing the WP pin state after the Stop condition has been sent will not alter or interrupt the execution of the write cycle.

If an attempt is made to write to the device while the WP pin has been asserted, the device will acknowledge the device address, word address and data bytes, but no write cycle will occur when the Stop condition is issued. The device will immediately be ready to accept a new read or write command.
8. Read Operations

Read operations are initiated the same way as write operations with the exception that the Read/Write Select bit in the device address byte must be a logic ‘1’. There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

8.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the V\textsubscript{CC} is maintained to the part. The address roll-over during a read is from the last byte of the last page to the first byte of the first page of the memory.

A current address read operation will output data according to the location of the internal data word address counter. This is initiated with a Start condition, followed by a valid device address byte with the R/W bit set to logic ‘1’. The device will ACK this sequence and the current address data word is serially clocked out on the SDA line. All types of read operations will be terminated if the bus master does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the master may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.

Figure 8-1. Current Address Read

8.2 Random Read

A random read begins in the same way as a byte write operation does to load in a new data word address. This is known as a “dummy write” sequence; however, the data byte and the Stop condition of the byte write must be omitted to prevent the part from entering an internal write cycle. Once the device address and word address are clocked in and acknowledged by the EEPROM, the bus master must generate another Start condition. The bus master now initiates a current address read by sending a Start condition, followed by a valid device address byte with the R/W bit set to logic ‘1’. The EEPROM will ACK the device address and serially clock out the data word on the SDA line. All types of read operations will be terminated if the bus master does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the master may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.
8.3 Sequential Read

Sequential reads are initiated by either a current address read or a random read. After the bus master receives a data word, it responds with an Acknowledge. As long as the EEPROM receives an ACK, it will continue to increment the word address and serially clock out sequential data words. When the maximum memory address is reached, the data word address will roll-over and the sequential read will continue from the beginning of the memory array. All types of read operations will be terminated if the bus master does not respond with an ACK (it NACKs) during the ninth clock cycle. After the NACK response, the master may send a Stop condition to complete the protocol, or it can send a Start condition to begin the next sequence.
9. Device Default Condition from Microchip

The AT24CM01 is delivered with the EEPROM array set to logic ‘1’, resulting in FFh data in all locations.
10. Packaging Information

10.1 Package Marking Information

AT24CM01: Package Marking Information

<table>
<thead>
<tr>
<th>8-lead SOIC</th>
<th>8-lead SOIJ</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATMLHYWN###%</td>
<td>COATMLHYWW</td>
</tr>
<tr>
<td>YYWWNNN</td>
<td>ATHYWW</td>
</tr>
<tr>
<td></td>
<td>NNN</td>
</tr>
<tr>
<td>8-lead TSSOP</td>
<td>8-ball WLCSP</td>
</tr>
<tr>
<td>ATHYWN###%</td>
<td></td>
</tr>
<tr>
<td>CO</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: ⚫ designates pin 1
Note 2: Package drawings are not to scale

Catalog Number Truncation

AT24CM01 Truncation Code ###: 2G

Date Codes

<table>
<thead>
<tr>
<th>Y = Year</th>
<th>M = Month</th>
<th>WW = Work Week of Assembly</th>
<th>% = Minimum Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>4: 2014</td>
<td>8: 2018</td>
<td>A: January 02: Week 2</td>
<td>D: 2.5V min</td>
</tr>
<tr>
<td>5: 2015</td>
<td>9: 2019</td>
<td>B: February 04: Week 4</td>
<td>M: 1.7V min</td>
</tr>
<tr>
<td>6: 2016</td>
<td>0: 2020</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>7: 2017</td>
<td>1: 2021</td>
<td>L: December 52: Week 52</td>
<td>...</td>
</tr>
</tbody>
</table>

Country of Assembly

<table>
<thead>
<tr>
<th>CO = Country of Origin</th>
</tr>
</thead>
</table>

Device Grade

<table>
<thead>
<tr>
<th>H or U = Industrial Grade</th>
</tr>
</thead>
</table>

Atmel Truncation

| AT = Atmel |
| ATM: Atmel |
| ATML: Atmel |

Lot Number or Trace Code

| NNN = Alphanumeric Trace Code (2 Characters for Small Packages) |

© 2019 Microchip Technology Inc. Datasheet 20006170A-page 24
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 1 of 2
### 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

#### Note:
For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

---

**Dimensions and Tolerances**

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Standoff</td>
<td>§</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Chamfer (Optional)</td>
<td>h</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Footprint</td>
<td>L1</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>φ</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
<tr>
<td>Mold Draft Angle Top</td>
<td>α</td>
</tr>
<tr>
<td>Mold Draft Angle Bottom</td>
<td>β</td>
</tr>
</tbody>
</table>

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

---

Microchip Technology Drawing No. C04-057-SN Rev D Sheet 2 of 2
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

---

<table>
<thead>
<tr>
<th>Units</th>
<th>MILTIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C</td>
</tr>
<tr>
<td>Contact Pad Width (X8)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X8)</td>
<td>Y1</td>
</tr>
</tbody>
</table>

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev B
8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
# AT24CM01

## Packaging Information

### 8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging)

![8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]](image)

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension</td>
<td>MIN</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Standoff §</td>
<td>A1</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
</tr>
<tr>
<td>Overall Width</td>
<td>E</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>E1</td>
</tr>
<tr>
<td>Overall Length</td>
<td>D</td>
</tr>
<tr>
<td>Foot Length</td>
<td>L</td>
</tr>
<tr>
<td>Lead Thickness</td>
<td>C</td>
</tr>
<tr>
<td>Lead Width</td>
<td>B</td>
</tr>
<tr>
<td>Mold Draft Angle</td>
<td>G1</td>
</tr>
<tr>
<td>Lead Angle</td>
<td>G2</td>
</tr>
<tr>
<td>Foot Angle</td>
<td>G3</td>
</tr>
</tbody>
</table>

**Notes:**
1. SOIJ, JEITA/EIAJ Standard, Formerly called SOIC
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

Microchip Technology Drawing No. C04-056C Sheet 2 of 2
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Overall Width</td>
<td>Z1</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
</tr>
<tr>
<td>Contact Pad Width (X8)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X8)</td>
<td>Y1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

**Units** | **MILLIMETERS**
---|---
**Dimension Limits** | **MIN** | **NOM** | **MAX**
Number of Pins | N | 8 |
Pitch | e | 0.65 BSC |
Overall Height | A | – | – | 1.20 |
Molded Package Thickness | A2 | 0.80 | 1.00 | 1.05 |
Standoff | A1 | 0.05 | – | 0.15 |
Overall Width | E | 6.40 BSC |
Molded Package Width | E1 | 4.30 | 4.40 | 4.50 |
Molded Package Length | D | 2.90 | 3.00 | 3.10 |
Foot Length | L | 0.45 | 0.60 | 0.75 |
Footprint | L1 | 1.00 REF |
Foot Angle | φ | 0° | – | 8° |
Lead Thickness | c | 0.09 | – | 0.20 |
Lead Width | b | 0.19 | – | 0.30 |

**Notes:**
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B
8-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
</tr>
<tr>
<td>Contact Pitch</td>
<td>E</td>
</tr>
<tr>
<td>Contact Pad Spacing</td>
<td>C1</td>
</tr>
<tr>
<td>Contact Pad Width (X8)</td>
<td>X1</td>
</tr>
<tr>
<td>Contact Pad Length (X8)</td>
<td>Y1</td>
</tr>
<tr>
<td>Distance Between Pads</td>
<td>G</td>
</tr>
</tbody>
</table>

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2086A
**COMMON DIMENSIONS**  
(Unit of Measure = mm)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>NOTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.460</td>
<td>0.499</td>
<td>0.538</td>
<td></td>
</tr>
<tr>
<td>A1</td>
<td>0.164</td>
<td>-</td>
<td>0.224</td>
<td></td>
</tr>
<tr>
<td>A2</td>
<td>0.280</td>
<td>0.305</td>
<td>0.330</td>
<td>Contact Microchip for details</td>
</tr>
<tr>
<td>E</td>
<td></td>
<td></td>
<td></td>
<td>Contact Sales for details</td>
</tr>
<tr>
<td>e</td>
<td>0.866</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>e2</td>
<td>0.500</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>d</td>
<td>1.000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>d2</td>
<td>0.500</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>b</td>
<td>0.239</td>
<td>0.269</td>
<td>0.299</td>
<td></td>
</tr>
</tbody>
</table>

*Dimensions are NOT to scale.*

### Pin Assignment Matrix

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Vcc</td>
<td>WP</td>
<td>NC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>SCL</td>
<td></td>
<td>A1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>SDA</td>
<td>A2</td>
<td>GND</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at [http://www.microchip.com/packaging](http://www.microchip.com/packaging).
11. Revision History

Revision A (March 2019)
Updated to Microchip template. Microchip DS20006170 replaces Atmel document 8812. Corrected \( t_{\text{LOW}} \) typo from 400 ns to 500 ns. Corrected \( t_{\text{AA}} \) typo from 550 ns to 450 ns. Updated Part Marking Information. Updated the “Software Reset” section. Added ESD rating. Removed lead finish designation. Updated trace code format in package markings. Updated section content throughout for clarification. Added a figure for “System Configuration Using Two-Wire Serial EEPROMs”. Added POR recommendations section. Updated SOIC, SOIJ and TSSOP package drawings to Microchip format.

Atmel Document 8812 Revision F (January 2015)
Updated the ordering information section, part markings, and the 8X and 8S2 package outline drawings.

Atmel Document 8812 Revision E (March 2013)
Updated document status from preliminary to complete. Corrected WLCSP pinout. Updated footers and disclaimer page.

Atmel Document 8812 Revision D (January 2013)
Corrected TSSOP pin label 7 to WP.

Atmel Document 8812 Revision C (December 2012)
Added WLCSP package. Updated part markings. Updated pinout diagram. Updated part markings. Corrected Byte Write figure from second typo error to first word address. Updated Sequential Read figure.

Atmel Document 8812 Revision B (July 2012)

Atmel Document 8812 Revision A (May 2012)
Initial release of this document.
The Microchip Web Site

Microchip provides online support via our web site at http://www.microchip.com/. This web site is used as a means to make files and information easily available to customers. Accessible by using your favorite Internet browser, the web site contains the following information:

- **Product Support** – Data sheets and errata, application notes and sample programs, design resources, user’s guides and hardware support documents, latest software releases and archived software
- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

Customer Change Notification Service

Microchip’s customer notification service helps keep customers current on Microchip products. Subscribers will receive e-mail notification whenever there are changes, updates, revisions or errata related to a specified product family or development tool of interest.


Customer Support

Users of Microchip products can receive assistance through several channels:

- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or Field Application Engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://www.microchip.com/support
Product Identification System

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

Product Family
24C = Standard I²C-compatible Serial EEPROM

Device Density
M = Megabit Family
01 = 1 Megabit

Shipping Carrier Option
B = Bulk (Tubes)
T = Tape and Reel, Standard Quantity Option
E = Tape and Reel, Extended Quantity Option

Operating Voltage
D = 2.5V to 5.5V
M = 1.7V to 5.5V

Device Grade or Wafer/Die Thickness
H or U = Industrial Temperature Range (-40°C to +85°C)
11 = 11mil Wafer Thickness

Package Option
SS = SOIC
S = SOIJ
X = TSSOP
U = WLCSP

Examples

<table>
<thead>
<tr>
<th>Device</th>
<th>Package</th>
<th>Package Drawing Code</th>
<th>Package Option</th>
<th>Voltage</th>
<th>Shipping Carrier Option</th>
<th>Device Grade</th>
</tr>
</thead>
<tbody>
<tr>
<td>AT24CM01-SSHD-B</td>
<td>SOIC</td>
<td>SN</td>
<td>SS</td>
<td>2.5V to 5.5V</td>
<td>Bulk (Tubes)</td>
<td>Industrial Temperature (-40°C to +85°C)</td>
</tr>
<tr>
<td>AT24CM01-SHMT</td>
<td>SOIJ</td>
<td>SM</td>
<td>SS</td>
<td>1.7V to 5.5V</td>
<td>Tape and Reel</td>
<td></td>
</tr>
<tr>
<td>AT24CM01-XHM-B</td>
<td>TSSOP</td>
<td>ST</td>
<td>X</td>
<td>1.7V to 5.5V</td>
<td>Bulk (Tubes)</td>
<td></td>
</tr>
<tr>
<td>AT24CM01-UUM-T</td>
<td>WLCSP</td>
<td>8U-6</td>
<td>U</td>
<td>1.7V to 5.5V</td>
<td>Tape and Reel</td>
<td></td>
</tr>
</tbody>
</table>

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
• Microchip is willing to work with the customer who is concerned about the integrity of their code.
• Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Legal Notice

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BitCloud, chipKIT, chipKIT logo, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Heldo, JukeBlox, KeeLoq, Kleer, LANCheck, LINK MD, maXStylus, maXTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.


SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestiC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.
Quality Management System Certified by DNV

ISO/TS 16949
Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company’s quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELIQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001:2000 certified.
### Worldwide Sales and Service

<table>
<thead>
<tr>
<th>AMERICAS</th>
<th>ASIA/PACIFIC</th>
<th>ASIA/PACIFIC</th>
<th>EUROPE</th>
</tr>
</thead>
</table>
| Corporate Office  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
http://www.microchip.com/support  
Web Address:  
www.microchip.com  
Atlanta  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455  
Austin, TX  
Tel: 512-257-3370  
Boston  
Westborough, MA  
Tel: 774-760-0087  
Fax: 774-760-0088  
Chicago  
Itasca, IL  
Tel: 630-285-0071  
Fax: 630-285-0075  
Dallas  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924  
Detroit  
Novi, MI  
Tel: 248-848-4000  
Houston, TX  
Tel: 281-894-5983  
Indianapolis  
Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453  
Los Angeles  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608  
Tel: 951-273-7800  
Raleigh, NC  
Tel: 919-844-7510  
New York, NY  
Tel: 631-435-6000  
San Jose, CA  
Tel: 408-735-9110  
Tel: 408-436-4270  
Canada - Toronto  
Tel: 905-695-1980  
Fax: 905-695-2078  
Australia - Sydney  
Tel: 61-2-9868-6733  
China - Beijing  
Tel: 86-10-8569-7000  
China - Chengdu  
Tel: 86-28-8665-5511  
China - Chongqing  
Tel: 86-23-8980-9588  
China - Dongguan  
Tel: 86-769-8702-9880  
China - Guangzhou  
Tel: 86-20-8755-8029  
China - Hangzhou  
Tel: 86-571-8792-8115  
China - Hong Kong SAR  
Tel: 852-2943-5100  
China - Nanjing  
Tel: 86-25-8473-2460  
China - Qingdao  
Tel: 86-632-8502-7355  
China - Shanghai  
Tel: 86-21-3326-8000  
China - Shenyang  
Tel: 86-24-2334-2829  
China - Shenzhen  
Tel: 86-755-8864-2200  
China - Suzhou  
Tel: 86-186-6233-1526  
China - Wuhan  
Tel: 86-27-5980-5300  
China - Xian  
Tel: 86-29-8833-7252  
China - Xiamen  
Tel: 86-592-2388138  
China - Zhuhai  
Tel: 86-755-3210040  
India - Bangalore  
Tel: 91-80-3090-4444  
India - New Delhi  
Tel: 91-11-4160-8631  
India - Pune  
Tel: 91-20-4121-0141  
Japan - Osaka  
Tel: 81-6-6152-7160  
Japan - Tokyo  
Tel: 81-3-8800-3770  
Korea - Daegu  
Tel: 82-53-744-4301  
Korea - Seoul  
Tel: 82-2-554-7200  
Malaysia - Kuala Lumpur  
Tel: 60-3-7651-7906  
Malaysia - Penang  
Tel: 60-4-227-8870  
Philippines - Manila  
Tel: 63-2-634-9065  
Singapore  
Tel: 65-6334-8870  
Taiwan - Hsin Chu  
Tel: 886-3-577-8366  
Taiwan - Kaohsiung  
Tel: 886-7-213-7830  
Taiwan - Taipei  
Tel: 886-2-2508-8600  
Thailand - Bangkok  
Tel: 66-2-694-1351  
Vietnam - Ho Chi Minh  
Tel: 84-28-5448-2100  
Austria - Wels  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393  
Denmark - Copenhagen  
Tel: 45-4450-2828  
Fax: 45-4485-2829  
Finland - Espoo  
Tel: 358-9-4520-820  
France - Paris  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79  
Germany - Garching  
Tel: 49-8931-9700  
Germany - Haan  
Tel: 49-2129-3766400  
Germany - Heilbronn  
Tel: 49-711-67-3636  
Germany - Karlsruhe  
Tel: 49-721-625370  
Germany - Munich  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44  
Germany - Rosenheim  
Tel: 49-8031-354-560  
Israel - Ra'anana  
Tel: 972-9-744-7705  
Italy - Milan  
Tel: 39-0331-742611  
Fax: 39-0331-466781  
Italy - Padova  
Tel: 39-049-7625286  
Netherlands - Drunen  
Tel: 31-416-690399  
Fax: 31-416-690340  
Norway - Trondheim  
Tel: 47-72884388  
Poland - Warsaw  
Tel: 48-22-3325737  
Romania - Bucharest  
Tel: 40-21-407-87-60  
Spain - Madrid  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91  
Sweden - Gothenberg  
Tel: 46-31-704-60-40  
Sweden - Stockholm  
Tel: 46-8-5900-4654  
UK - Wokingham  
Tel: 44-118-921-5800  
Fax: 44-118-921-5820