LAN9500i/LAN9500Ai Reference Design

Schematic Revision 2.4

Circuit Diagrams utilizing SMSC Products Are Included As A Means Of Illustrating Typical Semiconductor Applications: Consequently Complete Information Sufficient For Construction Purposes Is Not Necessarily Given. The Information Has Been Carefully Checked And Is Believed To Be Entirely Reliable. However, No Responsibility Is Assumed For Inaccuracies. Furthermore, Such Information Does Not Convey To The Purchaser Of The Semiconductor Devices Described Any License Under The Patent Rights Of SMSC Or Others. SMSC Reserves The Right To Make Changes At Any Time In Order To Improve Design And Supply The Best Product Possible.

<table>
<thead>
<tr>
<th>ITEM</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Title Page</td>
<td>1</td>
</tr>
<tr>
<td>LAN9500i/LAN9500Ai USB, Ethernet</td>
<td>2</td>
</tr>
</tbody>
</table>
NOTE:
Populate R8-R5 near LAN9500Ai. Place R6 and C1 near transformer.

NOTE:
Pin 7 is a no-connect (NC) for LAN9500Ai, but may be connected to VDD33A for backward compatibility with LAN9500 designs.

NOTE:
In an EMI constrained environment, populate these capacitors. These components must be placed close to the transformer.

NOTE:
For R14, see note, top left on this page.

NOTE:
For R6, see note, top left on this page.

LAN9500i/LAN9500Ai

Ethernet

Bypass and Filtering

Power

USB Connector

Optional Microwire Serial EEPROM