LAN83C185

High Performance Single Chip Low Power 10/100 Ethernet Physical Layer Transceiver (PHY)

PRODUCT FEATURES

- Single Chip Ethernet Phy
- Fully compliant with IEEE 802.3/802.3u standards
- 10BASE-T and 100BASE-TX support
- Supports Auto-negotiation and Parallel Detection
- Automatic Polarity Correction
- Integrated DSP with Adaptive Equalizer
- Baseline Wander (BLW) Correction
- Media Independent Interface (MII)
- 802.3u compliant register functions
- Vendor Specific register functions
- Comprehensive power management features
- General power-down mode
- Energy Detect power-down mode
- Low profile 64-pin TQFP package; lead-free RoHS compliant package also available
- Single +3.3V supply with 5V tolerant I/O
- 0.18 micron technology
- Low power consumption
- Operating Temperature 0°C to 70°C
- Internal +1.8V Regulator

Applications

- LAN on Motherboard
- 10/100 PCMCIA/CardBus Applications
- Embedded Telecom Applications
- Video Record/Playback Systems
- Cable Modems And Set-Top Boxes
- Digital Televisions
- Wireless Access Points

ORDER NUMBERS:
LAN83C185-JD FOR 64-PIN TQFP PACKAGE
LAN83C185-JT FOR 64-PIN TQFP LEAD-FREE ROHS COMPLIANT PACKAGE
General Description

The SMSC LAN83C185 is a low-power, highly integrated analog interface IC for high-performance embedded Ethernet applications. The LAN83C185 requires only a single +3.3V supply.

The LAN83C185 consists of an encoder/decoder, scrambler/descrambler, transmitter with wave-shaping and output driver, twisted-pair receiver with on-chip adaptive equalizer and baseline wander (BLW) correction, clock and data recovery, and Media Independent Interface (MII).

The LAN83C185 is fully compliant with IEEE 802.3/802.3u standards and supports both 802.3u-compliant and vendor-specific register functions. It contains a full-duplex 10-BASET/100BASE-TX transceiver and supports 10-Mbps (10BASE-T) operation on Category 3 and Category 5 unshielded twisted-pair cable, and 100-Mbps (100BASE-TX) operation on Category 5 unshielded twisted-pair cable.

Block Diagram

Figure 1 LAN83C185 Architectural Overview
## Package Outline

**Figure 2** 64 Pin TQFP Package Outline, 10X10X1.4 Body, 2 MM Footprint

**Table 1** 64 Pin TQFP Package Parameters

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOMINAL</th>
<th>MAX</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>~</td>
<td>~</td>
<td>1.60 Overall Package Height</td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
<td>~</td>
<td>0.15 Standoff</td>
</tr>
<tr>
<td>A2</td>
<td>1.35</td>
<td>~</td>
<td>1.45 Body Thickness</td>
</tr>
<tr>
<td>D</td>
<td>11.80</td>
<td>~</td>
<td>12.20 X Span</td>
</tr>
<tr>
<td>D1</td>
<td>9.80</td>
<td>~</td>
<td>10.20 X body Size</td>
</tr>
<tr>
<td>E</td>
<td>11.80</td>
<td>~</td>
<td>12.20 Y Span</td>
</tr>
<tr>
<td>E1</td>
<td>9.80</td>
<td>~</td>
<td>10.20 Y body Size</td>
</tr>
<tr>
<td>H</td>
<td>0.09</td>
<td>~</td>
<td>0.20 Lead Frame Thickness</td>
</tr>
<tr>
<td>L</td>
<td>0.45</td>
<td>0.60</td>
<td>0.75 Lead Foot Length</td>
</tr>
<tr>
<td>L1</td>
<td>~</td>
<td>1.00</td>
<td>~</td>
</tr>
<tr>
<td>e</td>
<td>~</td>
<td>0.50</td>
<td>Basic Lead Pitch</td>
</tr>
<tr>
<td>( \theta )</td>
<td>0°</td>
<td>~</td>
<td>7° Lead Foot Angle</td>
</tr>
<tr>
<td>W</td>
<td>0.17</td>
<td>0.22</td>
<td>0.27 Lead Width</td>
</tr>
<tr>
<td>R</td>
<td>0.08</td>
<td>~</td>
<td>~ Lead Shoulder Radius</td>
</tr>
<tr>
<td>R2</td>
<td>0.08</td>
<td>~</td>
<td>0.20 Lead Foot Radius</td>
</tr>
<tr>
<td>ccc</td>
<td>~</td>
<td>~</td>
<td>0.08 Coplanarity</td>
</tr>
</tbody>
</table>

**Notes:**
1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is \( \pm 0.04 \) mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm per side.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.