The PIC12C67X (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS30561), except for the anomalies described below.

**FIGURE 1: PIC12C67X VOLTAGE-FREQUENCY GRAPH, \(-40^\circ C \leq TA \leq +125^\circ C\)**

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
FIGURE 2: PIC12LC67X VOLTAGE-FREQUENCY GRAPH, \(-40^\circ C \leq T_A \leq 0^\circ C\)

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

FIGURE 3: PIC12LC67X VOLTAGE-FREQUENCY GRAPH, \(0^\circ C \leq T_A \leq +70^\circ C\)

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
FIGURE 4: PIC12LC67X VOLTAGE-FREQUENCY GRAPH, +70°C ≤ TA ≤ +85°C

Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.
Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS30561B), the following clarifications and corrections should be noted.

1. **Module: Register Summary (OSCCAL)**

   In Section 4.0, corrections for the Special Function Register Summary, Table 4-1, are shown.

   **TABLE 4-1: PIC12C67X SPECIAL FUNCTION REGISTER SUMMARY**

<table>
<thead>
<tr>
<th>Address</th>
<th>Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on Power-on Reset</th>
<th>Value on all other RESETS (3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8Fh</td>
<td>OSCCAL</td>
<td>CAL5</td>
<td>CAL4</td>
<td>CAL3</td>
<td>CAL2</td>
<td>CAL1</td>
<td>CAL0</td>
<td>—</td>
<td>—</td>
<td>1000 00—</td>
<td>——</td>
</tr>
</tbody>
</table>

   Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented read as '0'.
   Shaded locations are unimplemented, read as '0'.

   **Note 1:** These registers can be addressed from either bank.
   2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.
   3: Other (non Power-up) Resets include external RESET through MCLR and Watchdog Timer Reset.
   4: The IRP and RP1 bits are reserved on the PIC12C67X; always maintain these bits clear.
   5: The SCL (GP7) and SDA (GP6) bits are unimplemented on the PIC12C671/672 and read as '0'.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non Power-up) Resets include external RESET through MCLR and Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC12C67X; always maintain these bits clear.

5: The SCL (GP7) and SDA (GP6) bits are unimplemented on the PIC12C671/672 and read as '0'.

Note 1: These registers can be addressed from either bank.

2: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for the PC<12:8> whose contents are transferred to the upper byte of the program counter.

3: Other (non Power-up) Resets include external RESET through MCLR and Watchdog Timer Reset.

4: The IRP and RP1 bits are reserved on the PIC12C67X; always maintain these bits clear.

5: The SCL (GP7) and SDA (GP6) bits are unimplemented on the PIC12C671/672 and read as '0'.
2. Module: OSCCAL Register

Correction for the "OSCCAL" Register, Section 4.2.2.7, is shown.

4.2.2.7 OSCCAL REGISTER

The Oscillator Calibration (OSCCAL) Register is used to calibrate the internal 4 MHz oscillator. It contains six bits for calibration. Increasing the value increases the frequency.

REGISTER 4-7: OSCCAL REGISTER (ADDRESS 8Fh)

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAL5</td>
<td>CAL4</td>
</tr>
<tr>
<td>CAL3</td>
<td>CAL2</td>
</tr>
<tr>
<td>CAL1</td>
<td>CAL0</td>
</tr>
<tr>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

bit 7-2 CAL<5:0>: Calibration
bit 1-0 Unimplemented: Read as '0'

Legend:
R = Readable bit
W = Writable bit
U = Unimplemented bit, read as '0'
- n = Value at POR
'1' = Bit is set
'0' = Bit is cleared
x = Bit is unknown

3. Module: GPIO Register

Clarification to the "GPIO", Section 5.1 is provided. New I/O drawings were added.

5.1 GPIO

GPIO is an 8-bit I/O register. Only the low order 6 bits are used (GP<5:0>). Bits 6 and 7 (SDA and SCL, respectively) are used by the EEPROM peripheral on the PIC12CE673/674. Refer to Section 6.0 and Appendix B for use of SDA and SCL. Please note that GP3 is an input only pin. The configuration word can set several I/O's to alternate functions. When acting as alternate functions, the pins will read as '0' during port read.

Pins GP0, GP1 and GP3 can be configured with weak pull-ups and also with interrupt-on-change. The interrupt on change and weak pull-up functions are not pin selectable. If pin 4, (GP3), is configured as MCLR, a weak pull-up is always on. Interrupt-on-change for this pin is not set and GP3 will read as '0'. Interrupt-on-change is enabled by setting bit GPIE, INTCON<3>.

The interrupt can wake the device from SLEEP. The user, in the interrupt service routine, can clear the interrupt in the following manner:

a) Any read or write of GPIO will end the mismatch condition.

   b) Clear flag bit GPIF.

   A mismatch condition will continue to set flag bit GPIF. Reading GPIO will end the mismatch condition and allow flag bit GPIF to be cleared.

   Note that external oscillator use overrides the GPIO functions on GP4 and GP5.
FIGURE 5-2: GP2 Block Diagram

FIGURE 5-3: GP3 Block Diagram

FIGURE 5-4: GP4 Block Diagram

FIGURE 5-5: GP5 Block Diagram
4. Module: OSCCAL (Oscillator)
Corrections for the Internal 4 MHz RC Oscillator, Section 9.2.5, are shown.

9.2.5 INTERNAL 4 MHz RC OSCILLATOR

OSCCAL, when written to with the calibration value, will "trim" the internal oscillator to remove process variation from the oscillator frequency. Only bits<7:2> of OSCCAL are implemented, and bits<1:0> should be written as 0 for compatibility with future devices. The oscillator calibration location is not code protected.

5. Module: Initialization Condition (OSCCAL)
Corrections for Section 9.0, Initialization Conditions for all registers, Table 9-7, are shown.

TABLE 9-7: INITIALIZATION CONDITIONS FOR ALL REGISTERS

<table>
<thead>
<tr>
<th>Register</th>
<th>Power-on Reset</th>
<th>MCLR Resets WDT Reset</th>
<th>Wake-up via WDT or Interrupt</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSCCAL</td>
<td>1000 00--</td>
<td>uuuu uu--</td>
<td>uuuu uu--</td>
</tr>
</tbody>
</table>

Legend: u = unchanged, x = unknown, = unimplemented bit, read as '0', q = value depends on condition.

Note 1: One or more bits in INTCON and PIR1 will be affected (to cause wake-up).
2: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
3: See Table 9-5 for RESET value for specific condition.
4: If wake-up was due to A/D completing then bit 6 = 1, all other interrupts generating a wake-up will cause bit 6 = u.
5: If wake-up was due to A/D completing then bit 3 = 0, all other interrupts generating a wake-up will cause bit 3 = u.

Engineering Samples for the PIC12C671/2 may or may not follow this operational clarification for the OSCCAL register.
6. Module: DC Characteristics
Corrections for the DC Characteristics, Sections 12.3 and 12.4 are shown.

12.3 DC CHARACTERISTICS: PIC12C671/672 (Commercial, Industrial, Extended)
PIC12CE673/674 (Commercial, Industrial, Extended)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Characteristic</th>
<th>Sym</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D061</td>
<td>Input Leakage Current (Notes 2, 3)</td>
<td>IIL</td>
<td>8</td>
<td>130</td>
<td>250</td>
<td>μA</td>
<td>VSS ≤ VPIN ≤ VDD</td>
</tr>
<tr>
<td>D061A</td>
<td>GP3/MCLR (Note 5)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D061A</td>
<td>GP3/MCLR (Note 6)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D070</td>
<td>GPIO weak pull-up current (Note 4)</td>
<td>IPUR</td>
<td>50</td>
<td>250</td>
<td>400</td>
<td>μA</td>
<td>VDD = 5V, VPIN = VSS</td>
</tr>
</tbody>
</table>

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C67X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: Does not include GP3. For GP3 see parameters D061 and D061A.

5: This spec. applies to GP3/MCLR configured as external MCLR and GP3/MCLR configured as input with internal pull-up enabled.

6: This spec. applies when GP3/MCLR is configured as an input with pull-up disabled. The leakage current of the MCLR circuit is higher than the standard I/O logic.

12.4 DC CHARACTERISTICS: PIC12LC671/672 (Commercial, Industrial)
PIC12LCE673/674 (Commercial, Industrial)

<table>
<thead>
<tr>
<th>Param No.</th>
<th>Characteristic</th>
<th>Sym</th>
<th>Min</th>
<th>Typ†</th>
<th>Max</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>D061</td>
<td>Input Leakage Current (Notes 2, 3)</td>
<td>IIL</td>
<td>8</td>
<td>130</td>
<td>250</td>
<td>μA</td>
<td>VSS ≤ VPIN ≤ VDD</td>
</tr>
<tr>
<td>D061A</td>
<td>GP3/MCLR (Note 5)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D061A</td>
<td>GP3/MCLR (Note 6)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D070</td>
<td>GPIO weak pull-up current (Note 4)</td>
<td>IPUR</td>
<td>50</td>
<td>250</td>
<td>400</td>
<td>μA</td>
<td>VDD = 5V, VPIN = VSS</td>
</tr>
</tbody>
</table>

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC12C67X be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: Does not include GP3. For GP3 see parameters D061 and D061A.

5: This spec. applies to GP3/MCLR configured as external MCLR and GP3/MCLR configured as input with internal pull-up enabled.

6: This spec. applies when GP3/MCLR is configured as an input with pull-up disabled. The leakage current of the MCLR circuit is higher than the standard I/O logic.
7. **Module: GPIO Register**

Corrections for the GPIO pull-up resistor ranges are shown in Table 12-6.

**TABLE 12-6: GPIO PULL-UP RESISTOR RANGES**

<table>
<thead>
<tr>
<th>Vdd (Volts)</th>
<th>Temperature (°C)</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>GP0/GP1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.5</td>
<td>–40</td>
<td>38K</td>
<td>42K</td>
<td>63K</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>42K</td>
<td>48K</td>
<td>63K</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>85</td>
<td>42K</td>
<td>49K</td>
<td>63K</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>125</td>
<td>50K</td>
<td>55K</td>
<td>63K</td>
<td>Ω</td>
</tr>
<tr>
<td>5.5</td>
<td>–40</td>
<td>15K</td>
<td>17K</td>
<td>20K</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>18K</td>
<td>20K</td>
<td>23K</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>85</td>
<td>19K</td>
<td>22K</td>
<td>25K</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>125</td>
<td>22K</td>
<td>24K</td>
<td>28K</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>GP3(f)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.5</td>
<td>–40</td>
<td>65K</td>
<td>80K</td>
<td>850K</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>80K</td>
<td>100K</td>
<td>1150K</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>85</td>
<td>85K</td>
<td>110K</td>
<td>1300K</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>125</td>
<td>100K</td>
<td>120K</td>
<td>1500K</td>
<td>Ω</td>
</tr>
<tr>
<td>5.5</td>
<td>–40</td>
<td>50K</td>
<td>60K</td>
<td>600K</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>60K</td>
<td>65K</td>
<td>750K</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>85</td>
<td>65K</td>
<td>80K</td>
<td>900K</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>125</td>
<td>75K</td>
<td>90K</td>
<td>990K</td>
<td>Ω</td>
</tr>
</tbody>
</table>

* These parameters are characterized but not tested.

**Note 1:** The weak pull-up resistor and associated current for the GP3/MCLR pin is non-linear when the respective pin voltage is less than Vdd - 1.0V. See parameter D061 for GP3/MCLR pin current specifications.
8. Module: PACKAGING INFORMATION

Added 8-Lead Plastic Micro Leadframe Package (MF) and (MLF-S).

8-Lead Plastic Micro Leadframe Package (MF) 6x5 mm Body (MLF-S)

<table>
<thead>
<tr>
<th>Units</th>
<th>INCHES</th>
<th>MILLIMETERS*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimension Limits</td>
<td>MIN</td>
<td>NOM</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>n</td>
<td>8</td>
</tr>
<tr>
<td>Pitch</td>
<td>P</td>
<td>.050 BSC</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
<td>.033</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
<td>A2</td>
<td>.026</td>
</tr>
<tr>
<td>Standoff</td>
<td>A1</td>
<td>.000</td>
</tr>
<tr>
<td>Base Thickness</td>
<td>A3</td>
<td>.008 REF.</td>
</tr>
<tr>
<td>Overall Length</td>
<td>E</td>
<td>.194 BSC</td>
</tr>
<tr>
<td>Molded Package Length</td>
<td>E1</td>
<td>.184 BSC</td>
</tr>
<tr>
<td>Exposed Pad Length</td>
<td>E2</td>
<td>.152</td>
</tr>
<tr>
<td>Overall Width</td>
<td>D</td>
<td>.236 BSC</td>
</tr>
<tr>
<td>Molded Package Width</td>
<td>D1</td>
<td>.226 BSC</td>
</tr>
<tr>
<td>Exposed Pad Width</td>
<td>D2</td>
<td>.085</td>
</tr>
<tr>
<td>Lead Width</td>
<td>B</td>
<td>.014</td>
</tr>
<tr>
<td>Lead Length</td>
<td>L</td>
<td>.020</td>
</tr>
<tr>
<td>Tie Bar Width</td>
<td>R</td>
<td>.014</td>
</tr>
<tr>
<td>Mold Draft Angle Top</td>
<td>α</td>
<td>12°*</td>
</tr>
</tbody>
</table>

*Controlling Parameter

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC equivalent: pending

Drawing No. C04-113
8-Lead Plastic Micro Leadframe Package (MF) 6x5 mm Body (MLF-S)

<table>
<thead>
<tr>
<th>Units</th>
<th>INCHES</th>
<th>MILLIMETERS*</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>NOM</td>
</tr>
<tr>
<td>Dimension Limits</td>
<td>P</td>
<td>.050 BSC</td>
</tr>
<tr>
<td>Pad Width</td>
<td>B</td>
<td>.014</td>
</tr>
<tr>
<td>Pad Length</td>
<td>L</td>
<td>.020</td>
</tr>
<tr>
<td>Pad to Solder Mask</td>
<td>M</td>
<td>.005</td>
</tr>
</tbody>
</table>

*Controlling Parameter

Drawing No. C04-2113
REVISION HISTORY

Rev A Document (2/01)
Original errata document, which includes Figures 1, 2, and 3.

Rev B Document (6/00)
Under the Clarifications/Corrections, Items 1 through 7 were added.

Rev C Document (11/01)
Added Figure 1 and renumbered figures accordingly.
Under the Clarifications/Corrections, added Figures 5-1 through 5-5 added to Item 3.
Item 8, added 8-Lead Plastic Micro Leadframe Package (MF/MLF-S).
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