The PIC32MK General Purpose and Motor Control (GP/MC) family of devices that you have received functionally to the current Device Data Sheet (DS60001402D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MK General Purpose and Motor Control (GP/MC) family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (A2).

Data Sheet clarifications and corrections (if applicable) start on page 15 following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip’s programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select Window > Dashboard, and then click the Refresh Debug Tool Status icon ( ).
5. The part number and the Device and Revision ID values appear in the Output window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MK General Purpose and Motor Control (GP/MC) family silicon revisions are shown in Table 1.

### TABLE 1: SILICON DEVREV VALUES

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device ID(1)</th>
<th>Revision ID for Silicon Revision(1)</th>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC32MK1024MCF100</td>
<td>0x6201053</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIC32MK1024MCF064</td>
<td>0x6202053</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIC32MK0512MCF100</td>
<td>0x6204053</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIC32MK0512MCF064</td>
<td>0x6205053</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIC32MK1024GPE100</td>
<td>0x6207053</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIC32MK1024GPE064</td>
<td>0x6208053</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIC32MK0512GPE100</td>
<td>0x620A053</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIC32MK0512GPE064</td>
<td>0x620B053</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIC32MK1024GPD100</td>
<td>0x620D053</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIC32MK1024GPD064</td>
<td>0x620E053</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIC32MK0512GPD100</td>
<td>0x6210053</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIC32MK0512GPD064</td>
<td>0x6211053</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Refer to the “Memory Organization” and “Special Features” chapters in the current Device Data Sheet (DS60001402D) for detailed information on Device and Revision IDs for your specific device.
## TABLE 2: SILICON ISSUE SUMMARY

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Item</th>
<th>Issue Summary</th>
<th>Affected Revisions&lt;sup&gt;(1)&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary Oscillator</td>
<td>POSC</td>
<td>1.</td>
<td>Crystal primary oscillator (Posc) supports reduced operating range with restrictions.</td>
<td>X</td>
</tr>
<tr>
<td>Secondary Oscillator</td>
<td>SOSC</td>
<td>2.</td>
<td>The Secondary Oscillator (Sosc) does not support crystal operation.</td>
<td>X</td>
</tr>
<tr>
<td>Clocks</td>
<td>PBCLK6</td>
<td>3.</td>
<td>PBCLK6 defaults to 1:2 instead of 1:4.</td>
<td>X</td>
</tr>
<tr>
<td>FSCM</td>
<td></td>
<td>4.</td>
<td>Device falls back to LPRC instead of FRC on FSCM event.</td>
<td>X</td>
</tr>
<tr>
<td>VBAT</td>
<td>VBAT</td>
<td>5.</td>
<td>VBAT is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>VBAT</td>
<td>RTCC</td>
<td>6.</td>
<td>RTCC may lose Sosc clocks momentarily during a VDD to VBAT switch over event.</td>
<td>X</td>
</tr>
<tr>
<td>ADC</td>
<td>Level Trigger</td>
<td>7.</td>
<td>The ADC level trigger will not perform burst conversions in Debug mode.</td>
<td>X</td>
</tr>
<tr>
<td>ADC</td>
<td>Turbo Mode</td>
<td>8.</td>
<td>Turbo mode is not functional when two channels are linked for the purpose of increasing effective throughput.</td>
<td>X</td>
</tr>
<tr>
<td>ADC</td>
<td>DNL</td>
<td>9.</td>
<td>In Differential mode, DNL for code 3072 is not within specification.</td>
<td>X</td>
</tr>
<tr>
<td>ADC</td>
<td>AN26</td>
<td>10.</td>
<td>ADC input AN26 is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>ADC</td>
<td>Scan</td>
<td>11.</td>
<td>Scan list conversion will restart without finishing current scan list if new trigger occurs before scan completion with ADC7.</td>
<td>X</td>
</tr>
<tr>
<td>ADC</td>
<td>Scan</td>
<td>12.</td>
<td>Shared ADC7 has high Offset and Gain Error in Scan mode.</td>
<td>X</td>
</tr>
<tr>
<td>Op amp</td>
<td>Op amp</td>
<td>13.</td>
<td>Enabling an Op amp output control bit disables respective comparators output pin function if also enabled but comparator output status bit is still functional.</td>
<td>X</td>
</tr>
<tr>
<td>Op amp</td>
<td>Op amp</td>
<td>14.</td>
<td>Op amp output is always enabled regardless of output enable control bit if OPAMP is enabled.</td>
<td>X</td>
</tr>
<tr>
<td>Op amp</td>
<td>Op amp PGA Mode</td>
<td>15.</td>
<td>When used in PGA Unity Gain mode, an Op amp continues to function despite being disabled (i.e., AMPMOD = 0).</td>
<td>X</td>
</tr>
<tr>
<td>Op amp</td>
<td>Op amp PGA Mode</td>
<td>16.</td>
<td>Op amps in Unity Gain mode (i.e., ENPAGx bit (CFGCON2&lt;4, 2:0&gt; = 1) are non-functional.</td>
<td>X</td>
</tr>
<tr>
<td>Op amp</td>
<td>PSRR</td>
<td>17.</td>
<td>Op amp does not meet PSRR electrical specification.</td>
<td>X</td>
</tr>
<tr>
<td>Op amp</td>
<td>CMRR</td>
<td>18.</td>
<td>Op amps do not meet common mode voltage range (VCMR) specification.</td>
<td>X</td>
</tr>
<tr>
<td>DAC</td>
<td>INL</td>
<td>20.</td>
<td>Op amps do not meet gain margin specification.</td>
<td>X</td>
</tr>
<tr>
<td>DAC</td>
<td>DNL</td>
<td>21.</td>
<td>The DACs do not meet INL specification at AVDD less than 3V, and TA is greater than +85°C.</td>
<td>X</td>
</tr>
<tr>
<td>Timer1</td>
<td>Counter Async</td>
<td>22.</td>
<td>The DACs do not meet DNL specification at AVDD less than 3V.</td>
<td>X</td>
</tr>
<tr>
<td>Timer1</td>
<td>Sleep Async</td>
<td>23.</td>
<td>Timer1 in Asynchronous External Counter mode does not reflect the first count from an external ext T1CK input.</td>
<td>X</td>
</tr>
<tr>
<td>Timer1</td>
<td></td>
<td>24.</td>
<td>TMR1 register of Timer1 in Asynchronous mode remains at initial set value of five external clock pulses after wake-up from Sleep mode.</td>
<td>X</td>
</tr>
</tbody>
</table>

Note 1: Only those issues indicated in the last column apply to the current silicon revision.
## TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Item</th>
<th>Issue Summary</th>
<th>Affected Revisions(1)</th>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer1</td>
<td>Sleep</td>
<td>Async</td>
<td>25. Back-to-back writes to the TMR1 register are not allowed for four PBCLK2 cycles.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I/O</td>
<td>RTCC</td>
<td>26.</td>
<td>RTCC alarm output driver does not return to default/reset state on deep sleep wake-up through MCLR.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Deep Sleep</td>
<td>I/O</td>
<td>27.</td>
<td>Deep Sleep mode is non functional.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RCON</td>
<td>Register</td>
<td>28.</td>
<td>RCON status bits, VBPOR, PORIO, PORCORE, and VBAT, are inconsistent and cannot be used.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sleep</td>
<td>IPD</td>
<td>29.</td>
<td>3 mA increase in sleep when PB5DIV is disabled.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sleep</td>
<td>IPD</td>
<td>30.</td>
<td>Increase in sleep IPD current if USB pins D+ and D- are floating.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMP Status</td>
<td>Flags</td>
<td>31.</td>
<td>PMP input buffer full flag IBOF and out buffer underflow OBUF are set as soon as PMP is turned ON in Slave mode, when TTLEN = 1.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMP Slave</td>
<td>Mode</td>
<td>32.</td>
<td>CS is deasserting before RD in Slave mode.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTMU</td>
<td>Triggers</td>
<td>33.</td>
<td>Edge Sequencing mode (EDGSEQEN (CTMUCON&lt;2&gt;)) triggers are not functional</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTMU</td>
<td>TGEN</td>
<td>34.</td>
<td>When the TGEN bit is set, manual current sourcing (i.e., setting the EDG1STAT bit) from CTMU is not possible.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICAP</td>
<td>Debug</td>
<td>35.</td>
<td>Debug breakpoints are not supported when using Input Capture with DMA.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWM</td>
<td>Time Base</td>
<td>36.</td>
<td>Leading-edge Blanking (LED) in XPRES mode, XPRES bit (PWMCONx&lt;2&gt;) = 1, is not functional.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWM</td>
<td>I/O</td>
<td>37.</td>
<td>Alternate pin and I/O functions on unused PWM channels do not function when the PWM module is enabled.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWM</td>
<td>LEB</td>
<td>38.</td>
<td>Incorrect LEB trigger applied if dead time is enabled.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWM</td>
<td>Int.</td>
<td>39.</td>
<td>Multiple PWM Interrupts can occur for a single TRGIF, PWMLIF, and PWMHIF interrupt event, which causes the ISR to be re-executed multiple times if the PWM prescaler (i.e., PCLKDIV&lt;2:0&gt; bits (PTCON&lt;6:4&gt;)) or SCLKDIV&lt;2:0&gt; bits (STCON&lt;6:4&gt;) are greater than 5.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UART</td>
<td>TX/RX</td>
<td>40.</td>
<td>A UART Transmit Interrupt (UTXISEL&lt;1:0&gt; bits (UxSTA&lt;15:14&gt;) = '0b00) is generated and asserted while the transmit buffer contains at least one empty space and the UART Receiver Interrupt Flag bit (URXISEL&lt;1:0&gt; bits (UxSTA&lt;7:6&gt;) = '0b00) is asserted while the receive buffer is not empty and non-functional.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UART</td>
<td>TX</td>
<td>41.</td>
<td>A UART Transmit Interrupt (UTXISEL&lt;1:0&gt; bits = '0b01) is generated, but does not remain asserted when all of the characters have been transmitted.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UART</td>
<td>TX</td>
<td>42.</td>
<td>A UART Transmit Interrupt (UTXISEL&lt;1:0&gt; bits = '0b10) is generated but does not remain asserted while the transmit buffer is empty.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>UART</td>
<td>RX</td>
<td>43.</td>
<td>The UART Receive Interrupt flag (URXISEL&lt;1:0&gt; bits = '0b01) is asserted only when the receive buffer equals one-half full and not when the receive buffer is greater than one-half full.</td>
<td>X X</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.
### UART RX Interrupt (44)

The UART Receive Interrupt Flag bit (URXISEL<1:0> bits = '0b10) is asserted only when the receive buffer equals three-quarters full and not when the receive buffer is greater than three-quarters full.

### Reserved (45)

Reserved —

### CAN Interrupt (46)

The CAN Wake Interrupt Flag bit, WAKIF (CxINT<14>), is set even when the CAN module is disabled.

### Deadman Timer (DMT) Reset (47)

The Deadman Timer module does not cause a Non-maskable Interrupt (NMI) on a BAD1, BAD2, or DMTEVENT.

### Watchdog Timer (WDT) Reset (48)

Multiple valid key writes can be performed outside the Watchdog Timer window before a Reset occurs instead of the required single write.

### ICSP TDO (49)

The TDO pin becomes an output and toggles while programming on any of the ICSP PGECx/PGEDx pair.

### ViH Input Specification (50)

ViH(MIN) does not meet the electrical specification of \((0.65 \times VDD)\), but instead \(ViH(MIN) = (0.8 \times VDD)\).

### Cache Exception (51)

A Data Bus Error Exception can occur when prefetch cache is enabled (PREFEN<1:0> bits (CHECON<5:4>) = '0b01).

### BOR POR (52)

On a BOR event, and when the BORSEL bit (DEVCFG2<29>) = 0, the POR Status bit (RCON<1>) may also be erroneously set.

### BOR Reset (53)

On a BOR event, \(V_{POR} < V_{DD} < V_{BOR}\), a Reset is not generated when the BOR threshold is reached. System clocks will stop with all I/O pins function frozen in their present state until either \(V_{DD}\) falls to \(V_{POR}\) or \(V_{DD}\) returns to above \(V_{BOR}\).

### SPI2 PPS (54)

The SPI SS2R PPS register cannot be read nor used with bit instruction of the form SS2Rbits,SS2R as it is a read-modify-write command.

---

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.
Silicon Errata Issues

**Note 1:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. The table provided in each issue indicates which issues exist for a particular revision of silicon.

2: The following applies to the Affected Silicon Revision tables in each silicon issue:

- An ‘X’ indicates the issue is present in this revision of silicon.
- Shaded cells with an Em dash (‘—’) indicate that this silicon revision does not exist for this issue.
- Blank cells indicate an issue has been corrected or does not exist in this revision of silicon.

1. Module: Primary Oscillator

The Posc supports only specific crystal operation, as provided in [Table 3](#).

**Work around 1**

The Primary Oscillator (Posc) has been characterized to operate at 8 MHz and 12 MHz when the circuit shown in Figure 1 is implemented and the operating conditions provided in [Table 3](#) are met.

**Figure 1:** Posc CRYSTAL CIRCUIT

![Posc Crystal Circuit Diagram](image)

**Table 3:** CRYSTAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>Crystal Frequency (see Note 1)</th>
<th>Series Resistor Rs</th>
<th>Posc Gain Setting POSCGAIN&lt;1:0&gt; (DEVCFG0&lt;20:19&gt;)</th>
<th>Posc Boost Setting POSCBOOST (DEVCFG0&lt;21&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 MHz</td>
<td>2 kΩ</td>
<td>'0b00 (GAIN_0)</td>
<td>'0b1</td>
</tr>
<tr>
<td>12 MHz</td>
<td>1 kΩ</td>
<td>'0b00 (GAIN_0)</td>
<td>'0b1</td>
</tr>
<tr>
<td>24 MHz&lt;sup&gt;(3)&lt;/sup&gt;</td>
<td>0</td>
<td>'0b00 (GAIN_0)</td>
<td>'0b1</td>
</tr>
</tbody>
</table>

**Note 1:** Using any other crystal frequency will require special component selection and characterization.

2: A parallel resistor (RP) should not be used to increase the gain of the Posc.

3: Only 24 MHz crystals with a Mfg ESR ≤ 40Ω.

**Work around 2**

Alternatively, use an external clock or the Internal FRC Oscillator. Communication interfaces, such as CAN, USB, etc., with tighter clock accuracy requirements will not function with the FRC as clock source.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
<th>X</th>
<th>X</th>
</tr>
</thead>
</table>

2. Module: Secondary Oscillator

A crystal oscillator cannot be used as the input to the Secondary Oscillator (Sosc) pins, SOSCI and SOSCO.

**Work around**

Use an external clock source (32,768 Hz) applied to the SOSCO pin with the FSOSCEN bit (DEVCFG1<6>) set to ‘0’ (i.e., the Sosc pin is disabled through the Configuration Word) for a real-time clock base; otherwise, use the internal LPRC for non-precision requirements.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
<th>X</th>
<th>X</th>
</tr>
</thead>
</table>
3. Module: Clocks
The PB6DIV<6:0> (i.e., PBDIV<6:0> bits), default to '0b0000001 (1:2) instead of '0b0000011 (1:4). The max clock rate supported for the PBCLK6 bus is 30 MHz.

Work around
Set the PBDIV<6:0> bits = '0b0000011 (i.e., 1:4) assuming a 120 MHz SYSCLK. This is a register that requires an unlock sequence.

Affected Silicon Revisions

4. Module: FSCM
When the FCKSM<1:0> bits (DEVCFG1<15:14>) = '0b1x, clock fail monitoring is enabled, and a clock fail is detected. The SYSCLK source switches to the LPRC instead of the FRC as intended.

Work around
If the user has clock software clock switching enabled, FCKSM<1:0> = '0b11, they can perform a software clock switch to the FRC instead.

Affected Silicon Revisions

5. Module: VBAT
The VBAT pin is non-functional and it must be connected to VDD.

Work around
None.

Affected Silicon Revisions

6. Module: VBAT
RTCC may lose Sosc clocks momentarily during a VDD to VBAT switch over event.

Work around
None.

Affected Silicon Revisions

7. Module: ADC
The ADC level trigger, ADCTRGx register = '0b000010, will not perform burst conversions in Debug mode.

Work around
Do not use Debug mode with the ADC level triggers.

Affected Silicon Revisions

8. Module: ADC
Turbo mode, TRBEN bit (ADCCON1<31>) = 1, is not functional when two channels are linked for increasing effective throughput.

Work around
The user can still increase the effective throughput rate by interleaving ADC cores and trigger sources by connecting multiple dedicated high-speed ADCs to the same analog input and staggering the respective ADCx core triggers appropriately.

TABLE 4: INTERLEAVED ADC PERFORMANCE VDD > 2.5V

<table>
<thead>
<tr>
<th>Number of Interleaved ADC (12-bit mode)</th>
<th>Minimum TAD Sampling Time (SAMC)</th>
<th>Maximum Effective Sampling Rate (in Msps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>13</td>
<td>4.615</td>
</tr>
<tr>
<td>3</td>
<td>7</td>
<td>8.57</td>
</tr>
<tr>
<td>4</td>
<td>5</td>
<td>12</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
<td>15</td>
</tr>
<tr>
<td>6</td>
<td>3</td>
<td>20</td>
</tr>
</tbody>
</table>

9. Module: ADC
In Differential mode, code 3072 has a DNL of +3.

Work around
None.

Affected Silicon Revisions
10. Module: ADC

ADC input AN26 is not functional.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

11. Module: ADC

Scan list conversions defined in the ADCCSS1 register will restart without finishing the current scan list and do not generate an EOSRDY bit (ADCCON2<29>) end of scan interrupt status if a new trigger event from the STRGSRC<4:0> bits (ADCCON1<20:16>) trigger source occurs before the scan list completion on the shared ADC7 core.

Work around
Ensure that the STRGSRC<4:0> bits trigger source repetition rate > (sample + conversion) times of the sum of all ANx inputs defined in the ADCCSS1/ADCCSS2 registers.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

12. Module: ADC

Shared ADC7 has high Offset and Gain Error up to 38 Lsb in ADC7 Scan mode, as defined in the ADCCSS1/ADCCSS2 registers.

Work around
Increase the user-defined SAMC<9:0> bits (ADCCON2<25:16>) sample time register value by 4 TAD. This will reduce the ADC7 throughput that the user must consider, but it will reduce the gain and offset to less than 4 Lsb in 12-bit mode.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

13. Module: Op amp

Enabling the Op amp Output Enable bit, OAO (CMxCON<11>) = 1, disables the respective Comparator’s output pin function, CxOUT, on a different pin entirely if it was enabled, COE bit (CMxCON<14>); however, the Comparator Output Status is still functional.

Work around
None. The same Op amp/Comparator outputs cannot be enabled simultaneously.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

14. Module: Op amp

When the AMPPMOD bit (CMxCON<10>) = 1 (the Op amp is enabled), the Op amp output pin is active regardless of the state of the OAO bit (CMxCON<11>) Op amp output pin enable.

Work around
If the user does not want the Op amp output pin to be active, do not enable the Op amp until required.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
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<td>X</td>
</tr>
</tbody>
</table>

15. Module: Op amp

When used in 1x Unity Gain Buffer mode, an Op amp continues to function despite being disabled, (i.e., AMPPMOD bit (CMxCON<10>) = 0.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
<tr>
<td>X</td>
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</tbody>
</table>
16. Module: Op amp
Op amps in Unity Gain mode (i.e., ENPGAx bit (CFGCON2<20, 18, 17, 16>) = 1) are non-functional.

Work around
Do not use Op amp Unity Gain mode or use external 8x resistor signal attenuation network to Op amp input and then use op amp with 8x gain for net 1x signal gain.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
<tr>
<td>X</td>
<td></td>
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</tbody>
</table>

17. Module: Op amp
Op amp minimum PSRR electrical spec is -39 db versus -75 db typical.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
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<td></td>
</tr>
</tbody>
</table>

18. Module: Op amp
Op amps do not meet common mode voltage range specification between 0.4V-0.9V, where CMRR is reduced to < 28 db.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
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</tbody>
</table>

19. Module: Op amp
Op amps CMRR is < 28 db at input common mode voltages between 0.4V-0.9V, which is less than the electrical specification of 70 db minimum.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
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<td></td>
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</table>

20. Module: Op amp
Op amps do not meet the typical gain margin specification of 20, but are instead 15.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
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</tbody>
</table>

21. Module: DAC
DACs when sourcing IOUT(MAX) = -1.5 mA, do not meet INL ±4 Lsb specification when AVDD < 3.0V. and TA > 85ºC.

Work around
Do not use DACs to source > -0.75 mA at 2.6V < AVDD < 3.0V.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

22. Module: DAC
DACs do not meet DNL -1 Lsb min specification when AVDD < 3.0V. Worst case is -1.5 Lsb at 2.2V.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
<tr>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

23. Module: Timer1
Timer1 in Asynchronous External Counter mode, (i.e., TCS bit (T1CON<1> = 1, TSYNC bit (T1CON<2> = 0, and TECS<1:0> bits (T1CON<9:8>) are greater than ‘0b01) does not reflect the first count from an external T1CK input.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>
24. Module: Timer1
The TMR1 register of Timer1 in Asynchronous mode (i.e., TCS bit (T1CON<1> = 1, TSYNC bit (T1CON<2> = 0, and TECS<1:0> bits (T1CON<9:8>) are greater than ‘0b01), remains at initial set value for 5 external clock pulses after wake up from Sleep mode.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

25. Module: Timer1
Back-to-back writes to the TMR1 register are not allowed for four PBCLK2 cycles.

Work around
Wait for four PBCLK2 cycles before attempting a second write to the TMR1 register.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

26. Module: I/O
If the I/O function is configured for RTCC alarm output driver, it does not return to default/Reset input high–Z state on wake-up from Deep Sleep mode through MCLR.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
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</table>

27. Module: Deep Sleep
Deep-Sleep mode is non-functional.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

28. Module: RCON
The RCON register status bits, VBPOR, PORIO, PORCORE, and VBAT, are inconsistent and cannot be used.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

29. Module: Sleep
If the ON bit (PB5DIV<15>) = 0, and PBCLK5 is disabled, there is a 3 mA increase in Sleep I PD current.

Work around
Do not disable PBCLK5 before entering Sleep mode.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

30. Module: Sleep
There is a 170 µA increase in Sleep I PD current if USB pins D+ and D- are unused and left floating.

Work around
Add 50k pull-downs on D+ and D-, and tie VUSB3V3 to VDD.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

31. Module: PMP
The PMP Input Buffer ‘x’ Status Full bit, IB0F (PMSTAT<8>), and Output Buffer Underflow Status bit, OBUF (PMSTAT<6>), are set as soon as the PMP is turned ON in Slave mode, when TTLEN = 1.

Work around
After PMP initial initialization is complete, and before PMP and interrupts are enabled, clear these bits in user software.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
32. Module: PMP
CS is deasserting before RD in Slave mode. Slave mode is defeatured.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

33. Module: CTMU
Edge Sequencing mode, (EDGSEQEN bit (CTMUON<2>)), and Edge mode are not functional.

Work around
Use level modes.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

34. Module: CTMU
When the TGEN bit is set, manual current sourcing (i.e., setting the EDG1STAT bit) from the CTMU is not possible.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
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</tr>
</tbody>
</table>

35. Module: ICAP
Debug breakpoints are not supported when using Input Capture with DMA.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

36. Module: PWM
Leading edge blanking in XPRES mode, XPRES bit (PWMCONx<2>) = 1, is not functional.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
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</tr>
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</table>

37. Module: PWM
The PWM module does not relinquish control of the PWM pins even if they are not enabled, (i.e., PENH bit (IOCONx<15>) = 0 and PENL bit (IOCON<14>) = 0).

Work around
Disable corresponding unused user PWM channels by setting the appropriate PWMxMD bit in the PMD4 register = 1.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
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</table>

38. Module: PWM
Leading-edge Blanking (LEB) trigger is not applied at the correct time if dead time is enabled. The trigger is applied before the dead time when it should be applied after the dead time to coincide with the actual dead time delayed PWM signal transition.

Work around
Make the leading edge blanking time LEBDLYx<11:0> (i.e., LED<11:0> bits) equal to the desired leading edge blanking time, and the respective dead time value

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
### 39. Module: PWM

Multiple PWM Interrupts occur for single TRGIF, PWMLIF, and PWMHIF interrupt events. The ISR is re-executed multiple times if the PWM prescaler bits (PTCON<6:4>) (i.e., PCLKDIV<2:0>) or SCLKDIV<2:0> bits (i.e. STCON<6:4>) are greater than 5.

**Work around**

Insure that the PCLKDIV<2:0> bits and the STCON<2:0> bits are less than 5.

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
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</table>

### Affected Silicon Revisions

<table>
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<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
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</tbody>
</table>

### 40. Module: UART

A UART Transmit Interrupt (UTXISEL<1:0> bits (UxSTA<15:14>) = '0b00) is generated and asserted while the transmit buffer contains at least one empty space and the UART Receiver Interrupt Flag bit (URXISEL<1:0> bits (UxSTA<7:6>) = '0b00) is asserted while the receive buffer is not empty and non-functional.

**Work around**

None.

<table>
<thead>
<tr>
<th>A1</th>
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<tr>
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</table>

### Affected Silicon Revisions

<table>
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<tr>
<th>A1</th>
<th>A2</th>
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</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

### 41. Module: UART

A UART Transmit Interrupt (UTXISEL<1:0> bits = '0b01) is generated but does not remain asserted when all of the characters have been transmitted. Once the IFSx bit is cleared by the user, it does not remain asserted even while all characters have been transmitted. This behavior compounded with finite interrupt latency can create a race condition amongst subsequent TX interrupts.

**Work around**

To avoid the race condition, clear the UARTx IFS flag before writing a new value to the TX Buffer, UxTXREG, in the ISR.

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
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</table>

### Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

### 42. Module: UART

UART Transmit UTXISEL<1:0> bits = '0b10 Interrupt is generated but does not remain asserted while the transmit buffer is empty. Once the IFS bit is cleared by the user, it does not remain asserted even while transmit buffer is empty. This behavior compounded with finite interrupt latency can create a race condition amongst subsequent TX interrupts.

**Work around**

To avoid the race condition, clear the UARTx IFS flag before writing a new value to the TX Buffer, UxTXREG, in the ISR.

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tr>
<td>X</td>
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### Affected Silicon Revisions

<table>
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<tr>
<th>A1</th>
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<tbody>
<tr>
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<td>X</td>
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</tbody>
</table>

### 43. Module: UART

The UART Receive Interrupt Flag (URXISEL<1:0> bits = '0b01) is asserted only when the receive buffer equals one-half full and not when the receive buffer is greater than one-half full.

**Work around**

Before exiting the UART RX ISR, ensure all the contents of the RX Buffer have been read, by reading the contents of the RX Buffer in the ISR until the URXDA bit (UxSTA<0>) is cleared.

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
<tr>
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### Affected Silicon Revisions

<table>
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<tr>
<th>A1</th>
<th>A2</th>
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</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

### 44. Module: UART

The UART Receive Interrupt Flag bit (URXISEL<1:0> bits = '0b10) is asserted only when the receive buffer equals three-quarters full and not when the receive buffer is greater than three-quarters full.

**Work around**

Before exiting the UART RX ISR, ensure the entire contents of the RX Buffer have been read by reading the contents of RX Buffer in the ISR until the URXDA bit (UxSTA<10>) is cleared.

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
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<td>X</td>
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### Affected Silicon Revisions

<table>
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<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
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</tbody>
</table>
45. Module: Reserved
The issue, previously reported in a prior revision of this errata, is no longer relevant and was removed.

46. Module: CAN
The CAN Wake Interrupt Flag bit, WAKIF (CxINT<14>), is set even when the CAN module is disabled.

**Work around**
During CAN initialization, and before enabling the CAN peripheral, clear the WAKIF bit in user code.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
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<tbody>
<tr>
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</tbody>
</table>

47. Module: Deadman Timer (DMT)
The Deadman Timer module does not cause a Non-maskable Interrupt (NMI) on a BAD1, BAD2, or DMTEVENT.

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
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</tbody>
</table>

48. Module: Watchdog Timer (WDT)
Multiple valid key writes can be performed outside the Watchdog Timer window before a Reset occurs instead of the required single write.

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
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</tbody>
</table>

49. Module: ICSP
Regardless of other functions shared on the TDO pin, the TDO function becomes an active output and toggles while programming on any ICSP PGECx/PGEDx pair.

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

50. Module: ViH
ViH(MIN) does not meet the electrical specification of (0.65 * VDD), but is instead ViH(MIN) = (0.8 * VDD).

**Work around**
Although ViH is greater than VOH(MIN) = 2.4V, VOH(MIN) is a function of IOH(MAX). If the application does not load the ViH input source signal by more than IOH(MAX) by 50%, there should be no issues.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
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</tr>
</tbody>
</table>

51. Module: Cache
A Data Bus Error Exception can occur when prefetch cache is enabled, (PREFEN<1:0>) bits (CHECON<5:4> = '0b01).

**Work around**
Users must ensure that predictive prefetch cache is disabled by setting the PREFEN<1:0> bits = '0b00.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
<td></td>
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</tbody>
</table>

52. Module: BOR
On a BOR event, and when the BORSEL bit (DEVCFG2<29>) = 0, the POR Status bit (RCON<0>) may also be erroneously set.

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
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<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
53. Module: BOR

On a BOR event, \( V_{POR} < V_{DD} < V_{BOR} \), a Reset is not generated when the BOR threshold is reached. System clocks will stop with all I/O pins functions frozen in their present state until either \( V_{DD} \) falls to \( V_{POR} \) or \( V_{DD} \) returns to above \( V_{BOR} \). The user must assess if this \( V_{DD} \) brown-out condition and the resulting frozen I/O pin state has an adverse effect on their application (UART, PWM, I/O, OC, etc.).

**Work around 1**

Use an external Reset supervisor/monitor (see Figure 2). Some LDO regulators, as listed in Table 6, have an embedded reset supervisor included. The required minimum reset trip voltage of the supervisor should be at least \( (V_{BOR} + 0.5V) \) with the SMCLR bit (DEVCFG0<15>) = 0 and the BORSEL bit (DEVCFG2<29>) = 1 in the Configuration Words. This means that the minimum \( V_{DD} \) operating voltage of the application needs to be above the reset supervisor maximum trip voltage at [Reset Trip (max) + 0.2V], (i.e. Application \( V_{DD}(MIN) \approx (V_{BOR} + 0.5V + 0.2V) \). The reset supervisor should have an open drain output so as not to interfere with the MPLAB programming/debug tools. This workaround assures that MCLR will generate an internal POR and reset the I/O pins before the \( V_{BOR} \) trip point.

**Note:** For Motor Control applications utilizing the PWM module, only Work around 1 is recommended.

**Work around 2**

If the application can sustain frozen I/O states for ~2.1 ms (UART, CAN, I/O, etc.), the application must enable the Deep Sleep Watchdog Timer and Clock Fail Monitor, based on the details provided in Table 5 and Table 6. If implemented correctly, after ~2.1 ms, a valid internal reset state is entered and the I/O pins are set to the device default Reset state.

---

### FIGURE 2:  RESET SUPERVISOR CIRCUIT

![Reset Supervisor Circuit](image)

### TABLE 5: RESET SUPERVISOR/ VOLTAGE MONITOR

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Reset Trip</th>
<th>CPU MCLR Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIC803-26D2VC3</td>
<td>2.63v</td>
<td>Reset pin (Open Drain)</td>
</tr>
</tbody>
</table>

### TABLE 6: LDO REGULATORS WITH EMBEDDED RESET SUPERVISOR

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Topology</th>
<th>( V_{IN(MAX)} )</th>
<th>( V_{OUT} )</th>
<th>( I_{OUT} )</th>
<th>Reset Trip</th>
<th>CPU MCLR Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIC5239-3.3YM</td>
<td>LDO</td>
<td>30V</td>
<td>3.3V</td>
<td>500mA</td>
<td>3.3V-5%</td>
<td>FLG pin (Open Drain)</td>
</tr>
<tr>
<td>MIC5239-3.3YMM</td>
<td>LDO</td>
<td>30V</td>
<td>3.3V</td>
<td>500mA</td>
<td>3.3V-5%</td>
<td>FLG pin (Open Drain)</td>
</tr>
<tr>
<td>MCP1725-3302E/MC</td>
<td>LDO</td>
<td>6V</td>
<td>3.3V</td>
<td>500mA</td>
<td>3.3V-10%</td>
<td>PWRGD pin (Open Drain)</td>
</tr>
<tr>
<td>MCP1727-3302E/MF</td>
<td>LDO</td>
<td>6V</td>
<td>3.3V</td>
<td>1500mA</td>
<td>3.3V-10%</td>
<td>PWRGD pin (Open Drain)</td>
</tr>
</tbody>
</table>

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th></th>
<th>A1</th>
<th>A2</th>
<th>X</th>
</tr>
</thead>
</table>

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54. Module: SPI2

Reading the SPI2 SS2R PPS register will return indeterminate results. Therefore, also avoid using bit instruction of the form SS2Rbits.SQLR, as it is a read-modify-write command, which will corrupt the register value. Writes to the register or bit SET, CLR, or INV will function as expected.

Work around

Only use register write instruction forms to this register.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A2</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001402D):

**Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. **Module: Band Gap Temperature Sensor**

   The current revision of the data sheet erroneously included the Band Gap Temperature Sensor, which is not available in PIC32MK GP/MC devices. Therefore, **Table 36-43: Temperature Sensor Specifications** is invalid.

2. **Module: Deep Sleep Max Current**

   The Deep Sleep Max Current, as defined in parameter DC41 in **Table 36-8: DC Characteristics: Power-Down Current (IPD)** was incorrectly stated. The correct value is shown in the following table.

<table>
<thead>
<tr>
<th>DC CHARACTERISTICS</th>
<th>Standard Operating Conditions: 2.2V to 3.6V (unless otherwise stated)</th>
<th>Operating temperature (-40°C \leq T_A \leq +85°C) for Industrial (-40°C \leq T_A \leq +125°C) for Extended</th>
</tr>
</thead>
<tbody>
<tr>
<td>Param. No.</td>
<td>Typical</td>
<td>Maximum</td>
</tr>
<tr>
<td>DC41</td>
<td>6</td>
<td>40</td>
</tr>
</tbody>
</table>

3. **Module: CTMU Temperature Sensor Graph**

   The current revision of the data sheet erroneously included **Figure 37-5: Typical CTMU Temperature Sensor Voltage** in 37.0 “AC And DC Characteristics Graphs”.
4. Module: LPRC Accuracy Specification

The LPRC Minimum value, as defined in parameter F21 for the Extended temperature range in Table 36-18: AC Characteristics: Internal LPRC Accuracy was incorrectly stated. The correct value is shown in the following table.

<table>
<thead>
<tr>
<th>Param. No.</th>
<th>Characteristics</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>F21</td>
<td>LPRC</td>
<td>-8</td>
<td></td>
<td>+8</td>
<td>%</td>
<td>0°C ≤ TA ≤ +85°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-25</td>
<td></td>
<td>+25</td>
<td>%</td>
<td>-40°C ≤ TA ≤ +125°C</td>
</tr>
</tbody>
</table>
APPENDIX A: REVISION HISTORY

Rev A Document (3/2017)

Rev B Document (7/2017)
Updated silicon issue 45. to Reserved.

Rev C Document (9/2017)
Updated for Revision A2 silicon.
Added silicon issue 54. (SPI2).
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