The PIC32MZ Graphics (DA) family devices that you have received conform functionally to the current Device Data Sheet (DS60001361D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. If applicable, any silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC32MZ Graphics (DA) family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table (if applicable) apply to the current silicon revision (A1).

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip’s programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

Data Sheet clarifications and corrections (if applicable) start on page 13.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip’s programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

### Table 1: Silicon DevRev Values

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device ID(1)</th>
<th>Revision ID for Silicon Revision(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC32MZ1025DAA169</td>
<td>0x05F0C053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1025DAB169</td>
<td>0x05F0D053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1064DAA169</td>
<td>0x05F0F053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1064DAB169</td>
<td>0x05F10053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAA169</td>
<td>0x05F15053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAB169</td>
<td>0x05F16053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAA169</td>
<td>0x05F18053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAB169</td>
<td>0x05F19053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1025DAG169</td>
<td>0x05F4C053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1025DAH169</td>
<td>0x05F43053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1064DAG169</td>
<td>0x05F45053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1064DAH169</td>
<td>0x05F46053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAG169</td>
<td>0x05F4B053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAH169</td>
<td>0x05F4C053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAG169</td>
<td>0x05F4E053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAH169</td>
<td>0x05F4F053</td>
<td></td>
</tr>
</tbody>
</table>

Note 1: Refer to the “Memory Organization” and “Special Features” chapters in the current Device Data Sheet (DS60001361D) for detailed information on Device and Revision IDs for your specific device.
### TABLE 1: SILICON DEVREV VALUES (CONTINUED)

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device ID(1)</th>
<th>Revision ID for Silicon Revision(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC32MZ1025DAA176</td>
<td>0x05F78053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1025DAB176</td>
<td>0x05F79053</td>
<td>0x1</td>
</tr>
<tr>
<td>PIC32MZ1064DAA176</td>
<td>0x05F7B053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1064DAB176</td>
<td>0x05F7C053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAA176</td>
<td>0x05F81053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAB176</td>
<td>0x05F82053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAA176</td>
<td>0x05F84053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAB176</td>
<td>0x05F85053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1025DAG176</td>
<td>0x05FAE053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1025DAH176</td>
<td>0x05FAF053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1064DAG176</td>
<td>0x05FB053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1064DAH176</td>
<td>0x05FB2053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAG176</td>
<td>0x05FB7053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAH176</td>
<td>0x05FB8053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAG176</td>
<td>0x05FBA053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAH176</td>
<td>0x05FBB053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1025DAA288</td>
<td>0x05F5D053</td>
<td>0x1</td>
</tr>
<tr>
<td>PIC32MZ1025DAB288</td>
<td>0x05F5E053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1064DAA288</td>
<td>0x05F60053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1064DAB288</td>
<td>0x05F61053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAA288</td>
<td>0x05F66053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2025DAB288</td>
<td>0x05F67053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAA288</td>
<td>0x05F69053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2064DAB288</td>
<td>0x05F6A053</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Refer to the “Memory Organization” and “Special Features” chapters in the current Device Data Sheet (DS60001361D) for detailed information on Device and Revision IDs for your specific device.
## TABLE 2: SILICON ISSUE SUMMARY

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Item</th>
<th>Issue Summary</th>
<th>Affected Revisions&lt;sup&gt;(1)&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary Oscillator</td>
<td>Primary Oscillator Crystal</td>
<td>1</td>
<td>The Primary Oscillator (POsc) has been tested in a normal power-up sequence and supports specific crystal operation.</td>
<td>X</td>
</tr>
<tr>
<td>Secondary Oscillator</td>
<td>Secondary Oscillator Crystal</td>
<td>2</td>
<td>The Secondary Oscillator (SOsc) does not support crystal operation.</td>
<td>X</td>
</tr>
<tr>
<td>Reset</td>
<td>BOR</td>
<td>3</td>
<td>A system Reset is not generated on a BOR event (VPORIO&lt;VDIO&lt;VBORIO). This will stop system clocks with all the I/O pin functions frozen in the present state until either VDDIO falls to VPORIO or VDDIO&gt;VBORIO.</td>
<td>X</td>
</tr>
<tr>
<td>Reset</td>
<td>HVD Reset</td>
<td>4</td>
<td>A BOR event also sets the HVD1V8R (RCON&lt;29&gt;) bit.</td>
<td>X</td>
</tr>
<tr>
<td>Power-Saving PMD Bits</td>
<td>PMD Bits</td>
<td>5</td>
<td>Turning off the REFCLK modules through the PMD (PMD6&lt;11:8&gt;) bits causes unpredictable device behavior.</td>
<td>X</td>
</tr>
<tr>
<td>DMA</td>
<td>PMD Bits</td>
<td>6</td>
<td>Setting the PMD bit for DMA (PMD7&lt;4&gt;) does not disable clocks or DMA peripheral.</td>
<td>X</td>
</tr>
<tr>
<td>VBAT</td>
<td>—</td>
<td>7</td>
<td>VBAT is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>Deep Sleep</td>
<td>—</td>
<td>8</td>
<td>Deep Sleep mode is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>I²C</td>
<td>—</td>
<td>9</td>
<td>The I²C module does not function reliably under certain conditions.</td>
<td>X</td>
</tr>
<tr>
<td>ADC</td>
<td>Interrupts</td>
<td>10</td>
<td>ADC Group Early Interrupt is not functional (IRQ205).</td>
<td>X</td>
</tr>
<tr>
<td>ADC</td>
<td>Level Trigger</td>
<td>11</td>
<td>ADC level trigger will not perform burst conversions in debug mode.</td>
<td>X</td>
</tr>
<tr>
<td>ADC</td>
<td>DNL</td>
<td>12</td>
<td>In Differential mode, code 3072 is not within the specification.</td>
<td>X</td>
</tr>
<tr>
<td>ADC</td>
<td>Turbo Mode</td>
<td>13</td>
<td>Turbo mode is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>SDHC Clock</td>
<td>—</td>
<td>14</td>
<td>The SDHC module requires System PLL to be turned ON.</td>
<td>X</td>
</tr>
<tr>
<td>SDHC Clock Stability</td>
<td>—</td>
<td>15</td>
<td>The SDHC module may not function if the SDCD pin is not used.</td>
<td>X</td>
</tr>
<tr>
<td>SDHC Card Detect Status</td>
<td>—</td>
<td>16</td>
<td>Card detect status indication through the CDSLVL bit (SDHCSTAT1&lt;18&gt;) is inverted.</td>
<td>X</td>
</tr>
<tr>
<td>SDHC Write Protect Status</td>
<td>—</td>
<td>17</td>
<td>Write protect status indication through the WPSLVL bit (SDHCSTAT1&lt;19&gt;) is inverted.</td>
<td>X</td>
</tr>
<tr>
<td>SDHC Stop at Block Gap</td>
<td>—</td>
<td>18</td>
<td>The Stop at Block Gap feature of the SDHC module is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>HLVD</td>
<td>—</td>
<td>19</td>
<td>High/Low-Voltage Detect module is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>DDR2C</td>
<td>—</td>
<td>20</td>
<td>DDR2 is functional only between 0°C and 70°C.</td>
<td>X</td>
</tr>
<tr>
<td>DDR2C Internal VREF Circuit</td>
<td>—</td>
<td>21</td>
<td>Internal VREF circuit is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>SQI</td>
<td>XIP Mode</td>
<td>22</td>
<td>SQI XIP mode is not functional in cached memory space (KSEG2).</td>
<td>X</td>
</tr>
<tr>
<td>USB</td>
<td>Interrupt</td>
<td>23</td>
<td>USB General Event Interrupt (IRQ #132) is not persistent.</td>
<td>X</td>
</tr>
<tr>
<td>USB</td>
<td>Resume</td>
<td>24</td>
<td>The USB module does not support remote wake-up.</td>
<td>X</td>
</tr>
<tr>
<td>System Bus Writes</td>
<td>—</td>
<td>25</td>
<td>The EERP (SBTxECON&lt;16&gt;) bit is not functional.</td>
<td>X</td>
</tr>
<tr>
<td>Crypto</td>
<td>Flash Data Access</td>
<td>26</td>
<td>The Crypto module cannot access data from Flash.</td>
<td>X</td>
</tr>
</tbody>
</table>

<sup>Note 1:</sup> Only those issues indicated in the last column apply to the current silicon revision.
<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Item</th>
<th>Issue Summary</th>
<th>Affected Revisions(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART</td>
<td>Overflow</td>
<td>27.</td>
<td>Clearing the OERR bit (UxSTA&lt;1&gt;) clears the receiver buffer.</td>
<td>X</td>
</tr>
<tr>
<td>EBI</td>
<td>Chip Select</td>
<td>28.</td>
<td>For Asynchronous NOR Flash, EBI internal clock specification, TEBICLK (EB10) is not met.</td>
<td>X</td>
</tr>
<tr>
<td>CTMU</td>
<td>Triggers</td>
<td>29.</td>
<td>Edge Sequencing mode (EDGESEQEN(CTMUCON&lt;2&gt;)) and Edge modes are not functional.</td>
<td>X</td>
</tr>
<tr>
<td>CTMU</td>
<td>TGEN</td>
<td>30.</td>
<td>When the TGEN bit is set, manual current sourcing from CTMU is not possible.</td>
<td>X</td>
</tr>
<tr>
<td>Temperature Sensor</td>
<td>—</td>
<td>31.</td>
<td>The temperature sensor does not function.</td>
<td>X</td>
</tr>
<tr>
<td>ICSP</td>
<td>TDO</td>
<td>32.</td>
<td>While programming on any ICSP PGECx/PGEDx pair, the TDO pin will toggle.</td>
<td>X</td>
</tr>
<tr>
<td>PORTS</td>
<td>ViH Electrical Specification</td>
<td>33.</td>
<td>ViH specification of 0.65 * VDDIO is not met.</td>
<td>X</td>
</tr>
</tbody>
</table>

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.
Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A1).

1. Module: Primary Oscillator

   The POSC has been tested in a normal power-up sequence and supports specific crystal operation.

   **Work around 1**

   The Primary Oscillator (POSC) has been characterized to operate at 8 MHz and 12 MHz when the circuit shown in Figure 1 is implemented, and the operating conditions listed in Table 3 are met.

   ![Figure 1: POSC Crystal Circuit](image)

   **TABLE 3: CRYSTAL SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Crystal Frequency (See Note 1)</th>
<th>Series Resistor Rs</th>
<th>POSC Gain Setting POSCGAIN&lt;1:0&gt; (DEVCFG0&lt;20:19&gt;)</th>
<th>POSC Boost Setting POSCBOOST (DEVCFG0&lt;21&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 MHz</td>
<td>2 kΩ</td>
<td>`0b00 (GAIN_0)</td>
<td>`0b1</td>
</tr>
<tr>
<td>12 MHz</td>
<td>1 kΩ</td>
<td>`0b00 (GAIN_0)</td>
<td>`0b1</td>
</tr>
</tbody>
</table>

   **Note 1:** Using any other crystal frequency will require special component selection and characterization.

   **Note 2:** A parallel register (Rp) should not be used to increase the gain of the POSC.

   **Work around 2**

   Alternatively, use an external clock or Internal FRC Oscillator. Note that communication interfaces (DDR2, USB, etc.,) with tighter clock accuracy requirements will not function with the FRC as clock source.

   **Affected Silicon Revisions**

   | A1 | X |   |   |

2. Module: Secondary Oscillator

   A crystal oscillator cannot be used as the input to the Secondary Oscillator (SOSC) pins: SOSCI and SOSCO.

   **Work around**

   Use an external clock source (32,768 Hz) applied to the SOSCO pin with the FSOSCEN bit (DEVCFG1<6>) set to '0' (i.e., the SOSC is disabled through the Configuration Word) for a real-time clock base; otherwise, use the internal LPRC for non-precision requirements.

   **Affected Silicon Revisions**

   | A1 | X |   |   |

---
3. Module: Reset

A system Reset is not generated on a BOR event (VPORIO<VDDIO<VBORIO). This will stop system clocks with all the I/O pin functions frozen in the present state until either VDDIO falls to VPORIO or VDDIO>VBORIO.

Work around

Reset device using a MCLR pin through an external reset supervisor/monitor is shown in Figure 2. Set the SMCLR (DEVCFG2<15>) configuration bit to '0', which makes the MCLR to act as a POR Reset instead of a normal system reset.

Table 4 and Table 5 provide a list of external Reset supervisor and regulators with built in Reset supervisors that can be used.

When selecting an external supervisor other than the ones provided in Table 4 and Table 5, the following requirements must be taken into consideration:

- Minimum Reset trip voltage of the external supervisor should be VBORIO (Max)+0.5V.
- The external reset supervisor/LDO output going to MCLR should have an open drain output to not interfere with the MPLAB programming/debug tools.

When this work around is implemented, the minimum VDDIO operating voltage of the application needs to be above the reset supervisor maximum trip voltage + 0.2V, where 0.2V compensates for variation in the external reset supervisor voltage.

FIGURE 2: EXTERNAL RESET CIRCUIT

TABLE 4: RESET SUPERVISOR / VOLTAGE MONITOR

<table>
<thead>
<tr>
<th>PART#</th>
<th>V IN (Max.)</th>
<th>V OUT</th>
<th>IOUT</th>
<th>RESET TRIP VOLTAGE</th>
<th>MCLR SOURCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIC803-26D2VC3</td>
<td>30V</td>
<td>3.3V</td>
<td>500ma</td>
<td>3.3V-5%</td>
<td>FLG pin (Open Drain)</td>
</tr>
<tr>
<td>MIC803-3.3YM</td>
<td>30V</td>
<td>3.3V</td>
<td>500ma</td>
<td>3.3V-5%</td>
<td>FLG pin (Open Drain)</td>
</tr>
<tr>
<td>MCP1725-3302E/MC</td>
<td>6V</td>
<td>3.3V</td>
<td>500ma</td>
<td>3.3V-10%</td>
<td>PWRGD pin (Open Drain)</td>
</tr>
<tr>
<td>MCP1727-3302E/MF</td>
<td>6V</td>
<td>3.3V</td>
<td>1500ma</td>
<td>3.3V-10%</td>
<td>PWRGD pin (Open Drain)</td>
</tr>
</tbody>
</table>

TABLE 5: LDOs WITH EMBEDDED RESET SUPERVISOR

<table>
<thead>
<tr>
<th>PART#</th>
<th>Vin (Max.)</th>
<th>Vout</th>
<th>IOUT</th>
<th>RESET TRIP VOLTAGE</th>
<th>MCLR SOURCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIC5239-3.3YM</td>
<td>30V</td>
<td>3.3V</td>
<td>500ma</td>
<td>3.3V-5%</td>
<td>FLG pin (Open Drain)</td>
</tr>
<tr>
<td>MIC5239-3.3YMM</td>
<td>30V</td>
<td>3.3V</td>
<td>500ma</td>
<td>3.3V-5%</td>
<td>FLG pin (Open Drain)</td>
</tr>
<tr>
<td>MCP1725-3302E/MC</td>
<td>6V</td>
<td>3.3V</td>
<td>500ma</td>
<td>3.3V-10%</td>
<td>PWRGD pin (Open Drain)</td>
</tr>
<tr>
<td>MCP1727-3302E/MF</td>
<td>6V</td>
<td>3.3V</td>
<td>1500ma</td>
<td>3.3V-10%</td>
<td>PWRGD pin (Open Drain)</td>
</tr>
</tbody>
</table>

Affected Silicon Revisions

| A1 |     |     |     |     |
| X  |     |     |     |     |
4. Module: Reset

ABOR event also sets the HVD1V8R (RCON<29>) bit.

Work around

True high-voltage detect will set only the HVD1V8R (RCON<29>) bit. This bit should be ignored when it is set along with the BOR (RCON<1>) bit. Also, make sure to clear the HVD1V8R bit on exit from the BOR event, if set.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

5. Module: Power-Saving

Turning off the REFCLK modules through the PMD (PMD6<11:8>) bits causes unpredictable device behavior.

Work around

None. Do not disable the REFCLK modules through the PMD bits.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

6. Module: DMA

Setting the PMD bit for DMA (PMD7<4>) does not disable clocks or DMA peripheral.

Work around

Use the ON (DMACON<15>) bit to enable/disable DMA globally, or use CHEN (DCHxCON<7>) to enable/disable individual channels.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

7. Module: VBAT

The VBAT pin is not functional. Connect the VBAT pin to VDDIO.

Work around

None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

8. Module: Deep Sleep

Deep Sleep mode is not functional.

Work around

None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
9. **Module: I²C**

Indeterminate I²C module behavior may result when data rates > 100 kHz and/or continuous sequential data transfers > 500 bytes are used.

The potential false intermittent error signals can result in one of the following error conditions, which are listed in order of decreasing frequency:

- **False Error Condition 1:**
  False Master Bus Collision Detect (Master-mode only) – The error is indicated through the BCL bit (I2CxSTAT<10>).

- **False Error Condition 2:**
  Receive Overflow (Master or Slave modes) – The error is indicated through the I2COV bit (I2CxSTAT<20>).

- **False Error Condition 3:**
  Suspended I²C Module Operations (Master or Slave modes) – I²C transactions in progress are inadvertently suspended without error indications.

**Note:** All three false errors are recoverable in software.

**Work around 1**

- **False Error Condition 1:**
  Clear the Master Bus Collision Detect (BCL bit (I2CxSTAT<10>) after the bus returns to an Idle state. The software can monitor the S bit (I2CxSTAT<3>) and the P (I2CxSTAT<4>) bit to wait for an Idle bus. When the software services the bus collision Interrupt Service Routine and the I²C bus is free, the software can resume communication by asserting a new Start condition.

- **False Error Condition 2:**
  Clear the Receive Overflow Status flag I2COV bit (I2CxSTAT<20>), and then resume normal operation.

- **False Error Condition 3:**
  Initialize a Timer to slightly greater than the worst case I²C transaction cycle, (i.e., from Start-to-Stop, including the sum of all other application PC flow latencies, calls, interrupts, etc.). Exact timing is not required, rather just long enough so that a normal transaction is not interrupted. Prior to the beginning of each transaction, start the timer. Be sure to stop and reset the timer after completion of each successful I²C transaction. During the Timer interrupt (i.e., the I²C transaction has timed out), disable the I²C module by setting the ON bit (I2CxCON<15>) = 0. After disabling the module, wait 4 instruction cycles, after which time the I2CxSTAT register will automatically be cleared. Re-enable the I²C module by setting the ON bit = 1 and resume normal operation.

**Work around 2**

Instead of using the hardware I²C module, use a software “bit-bang” implementation.

**Affected Silicon Revisions**

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Note: All three false errors are recoverable in software.
10. Module: ADC
The ADC Group Early Interrupt (IRQ #205) feature is not functional.

**Work around**
Use individual ADC Early Interrupts (IRQ #119 through IRQ #203 and IRQ #206).

**Affected Silicon Revisions**
- A1
- X

11. Module: ADC
The ADC level trigger will not perform burst conversions in Debug mode.

**Work around**
Do not use Debug mode with the ADC level trigger.

**Affected Silicon Revisions**
- A1
- X

12. Module: ADC
In Differential mode, code 3072 has a DNL of +3.

**Work around**
None.

**Affected Silicon Revisions**
- A1
- X

13. Module: ADC
Turbo mode is not functional when two channels are linked for the purpose of increasing throughput.

**Work around**
None.

**Affected Silicon Revisions**
- A1
- X

14. Module: SDHC
The SDHC module requires the System PLL to be turned ON.

**Work around**
SPLL should be enabled before using the SD Host Controller (SDHC) module.

**Affected Silicon Revisions**
- A1
- X

15. Module: SDHC
The SDHC module may not function if the SDCD pin is not used.

**Work around 1**
Set CDSSEL (SDHCCON1<7>) to ‘1’ and CDTLVL (SDHCCON1<6>) to ‘0’.

**Work around 2**
Ensure that the SDCD pin is used and driven to a known state externally.

**Affected Silicon Revisions**
- A1
- X

16. Module: SDHC
Card-detect status indication through the CDSLVL bit (SDHCSTAT1<18>) is inverted.

**Work around 1**
Use ACMD42 to detect the card’s presence.

**Work around 2**
If SDCD is used for card detect, add a software work around to invert the CDSLVL (SDHCSTAT1<18>) state.

**Affected Silicon Revisions**
- A1
- X
17. Module: SDHC
Write-protect status indication through the WPSLVL bit (SDHCSTAT1<19>) is inverted.

Work around
If SDWP is used for Write-protect, add a software work around to invert WPSLVL (SDHCSTAT1<19>) state.

Affected Silicon Revisions

18. Module: SDHC
The Stop at Block Gap feature of the SDHC module is not functional.

Work around
None.

Affected Silicon Revisions

19. Module: HLVD
High/Low-Voltage Detect module is not functional.

Work around
None.

Affected Silicon Revisions

20. Module: DDR2C
DDR2 is functional only between 0°C and 70°C.

Work around
None.

Affected Silicon Revisions

21. Module: DDR2C
Internal VREF circuit (voltage divider) is not functional.

Work around
Use external voltage divider circuit on the VREF pin to track VDR1V8/2. Make sure to set INTVREFCON<1:0> (CFGMPPLL<7:6>) to 0'b00 before initializing DDR2.

Affected Silicon Revisions

22. Module: SQI
SQI eXecute-In-Place (XIP) mode is not functional in cached memory space (KSEG2).

Work around
Use KSEG3 (un-cached, starts at 0xF0000000) address space to access SQI Flash in XIP mode.

Affected Silicon Revisions

23. Module: USB
USB General Event Interrupt (IRQ #132) is not persistent as expected.

Work around
Handle USB general events in Non-persistent mode.

Affected Silicon Revisions

24. Module: USB
The USB module does not support remote wake-up through the USBRBIE bit (USBCRCON<1>).

Work around
None.

Affected Silicon Revisions
25. Module: System Bus
The ERRP (SBTxECON<16>) bit is not functional and should not be used.

Work around
None.

Affected Silicon Revisions

| A1 | X |

26. Module: Crypto
The Crypto module cannot access data from Flash due to pre-fetch cache corruption. Both workarounds listed below do not impact CPU performance when L1 cache is used by CPU.

Work around 1
Disable predictive prefetching for all addresses except CPU instructions and data. This can be achieved by NOT setting PREFEN<1:0> (PRECON<5:4>) to 0'b11.

Work around 2
Set Flash Wait states using the PFMWS<2:0> bits (PRECON<2:0>) to greater than four.

Affected Silicon Revisions

| A1 | X |

27. Module: UART
Clearing the receive buffer overrun error through the OERR bit (UxSTA<1>) clears the receive buffer. This condition occurs when the RUNOVF bit (UxMODE<16>) is set, and an overflow condition occurs.

Work around
When a receive buffer overrun error occurs, read the entire receive FIFO through the UxRXREG register before clearing the OERR (UxSTA<1>) bit.

Affected Silicon Revisions

| A1 | X |

28. Module: EBI
For Asynchronous NOR Flash, EBI internal clock specification, TEBICLK (EB10) is not met.

Work around
When asynchronous NOR is attached to EBI, the system frequency would have to be reduced to 180 MHz for it to properly function.

Affected Silicon Revisions

| A1 | X |

29. Module: CTMU
Edge Sequencing mode (EDGSEQEN(CTMU<CON<2>)) and Edge mode are not functional.

Work around
Use level modes.

Affected Silicon Revisions

| A1 | X |

30. Module: CTMU
When the TGEN bit is set, manual current sourcing (i.e. setting the EDG1STAT bit) from CTMU is not possible.

Work around
None.

Affected Silicon Revisions

| A1 | X |

31. Module: Temperature Sensor
The temperature sensor is not functional.

Work around
None.

Affected Silicon Revisions

| A1 | X |
32. Module: ICSP
   While programming/debugging the device through any PGECx/PGEDx pair, TDO will toggle.

   **Work around**
   None.

   **Affected Silicon Revisions**

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33. Module: PORTS
   VIH specification of 0.65 * VDDIO is not met. Use VIH specification of 0.8 * VDDIO.

   **Work around**
   None.

   **Affected Silicon Revisions**

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Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001361D):

**Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

No issues to report.

APPENDIX A: REVISION HISTORY

Rev A Document (3/2017)

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