This document describes known silicon errata for the KSZ8041 family of devices, which includes the following:

- KSZ8041NL / KSZ8041NLI / KSZ8041NL AM
- KSZ8041TL / KSZ8041TLI
- KSZ8041FTL / KSZ8041FTLI
- KSZ8041MLL
- KSZ8041RNL / KSZ8041RNLI

The silicon errata discussed in this document are for silicon with silicon revisions as listed in Table 1. The silicon revision can be determined by the device’s top marking as indicated in Figure 1. A summary of KSZ8041 silicon errata is provided in Table 2.

### TABLE 1: AFFECTED SILICON REVISIONS

<table>
<thead>
<tr>
<th>Part Numbers</th>
<th>Silicon Revision</th>
</tr>
</thead>
<tbody>
<tr>
<td>KSZ8041NL AM</td>
<td>A3</td>
</tr>
<tr>
<td>KSZ8041NL, KSZ8041NLI, KSZ8041TL, KSZ8041TLI,</td>
<td>A4</td>
</tr>
<tr>
<td>KSZ8041FTL, KSZ8041FTLI, KSZ8041FTLII, KSZ8041MLL</td>
<td></td>
</tr>
<tr>
<td>KSZ8041RNL, KSZ8041RNLI</td>
<td>A (different marking, but same engineering silicon revision as A4)</td>
</tr>
</tbody>
</table>

### FIGURE 1: TOP MARKING SILICON REVISION INDICATION

The markings in this position indicate the Silicon Revision.

**Note:** The purpose of Figure 1 is to detail the top markings of an example part and highlight the location of the silicon revision. Other top marking values may differ (lot codes, location of manufacture, etc.).
TABLE 2: SILICON ISSUE SUMMARY

<table>
<thead>
<tr>
<th>Item Number</th>
<th>Silicon Issue Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Receiver error in 100BASE-TX mode following software power down</td>
</tr>
<tr>
<td>2.</td>
<td>Pin Strapping failures due to 1.8V core power slow ramp-up</td>
</tr>
</tbody>
</table>

Silicon Errata Issues

Module 1: Receiver error in 100BASE-TX mode following software power down

DESCRIPTION
Some KSZ8041 devices may exhibit receiver errors after the software power down bit (register 0h, bit 11), is set and then cleared. The problem only occurs following software power down. There is no issue following power up or hardware reset.

END USER IMPLICATIONS
When the failure occurs:
• The RXER pin is asserted randomly
• The RXER counter (register 15h) increments
• The RXER interrupt bit (register 18h, bit 6) is set
• 100BASE-TX receive side exhibits errors (transmit side functions properly)
• 10BASE-T transmit and receive function properly
The only ways to exit the failure condition are:
• Cycle power off and on
• Set and clear the software power down bit (this method may resolve the issue, but is not guaranteed)

Work around
It is recommended to not use the software power-down feature.

PLAN
This errata will not be covered in a future revision.
Module 2:  Pin Strapping failures due to 1.8V core power slow ramp-up

DESCRIPTION
A small percentage (<1%) of devices can potentially encounter pin strapping failures with fast 3.3V supply rise times (<150us) or slow core rail rise times, due to a large bulk storage capacitor value (10uF or greater) for the 1.8V core.

END USER IMPLICATIONS
When this errata occurs, pin strap values may not be correctly latched.

Work around
Reduce the 1.8V core bulk storage capacitor from 10uF to 1.0uF and ensure the 3.3V supply rise time is 250us or greater.

PLAN
This errata is not planned to be corrected in a future revision.
APPENDIX A: DOCUMENT REVISION HISTORY

<table>
<thead>
<tr>
<th>Revision Level &amp; Date</th>
<th>Section/Figure/Entry</th>
<th>Correction</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS80000700A (05-05-16)</td>
<td>All</td>
<td>Initial release</td>
</tr>
</tbody>
</table>