PIC32MZ Embedded Connectivity with Floating Point Unit (EF) Family Silicon Errata and Data Sheet Clarification

The PIC32MZ Embedded Connectivity with Floating Point Unit (EF) family of devices that you have received conform functionally to the current Device Data Sheet (DS60001320D), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The silicon revision level can be identified using the current version of MPLAB® X IDE and Microchip’s programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB X IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB X IDE project.
3. Configure the MPLAB X IDE project for the appropriate device and hardware debugger.
4. Select Window > Dashboard, and then click the Refresh Debug Tool Status icon ( ).
5. The part number and the Device and Revision ID values appear in the Output window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various PIC32MZ EF Family silicon revisions are shown in Table 1.

### TABLE 1: SILICON DEVREV VALUES

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device ID(1)</th>
<th>Revision ID for Silicon Revision(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC32MZ0512EFE064</td>
<td>0x7201053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ0512EFF064</td>
<td>0x7206053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ0512EFK064</td>
<td>0x722E053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1024EFE064</td>
<td>0x7202053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1024EFF064</td>
<td>0x7207053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1024EFK064</td>
<td>0x722F053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1024EFG064</td>
<td>0x7203053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1024EFH064</td>
<td>0x7208053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ1024EFM064</td>
<td>0x7230053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ2048EFG064</td>
<td>0x7204053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ2048EFH064</td>
<td>0x7209053</td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ2048EFM064</td>
<td>0x7231053</td>
<td>A3</td>
</tr>
</tbody>
</table>

Note 1: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

Note 2: Refer to the “Memory Organization” and “Special Features” chapters in the current Device Data Sheet (DS60001320D) for detailed information on Device and Revision IDs for your specific device.
### TABLE 1: SILICON DEVREV VALUES (CONTINUED)

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device ID(1)</th>
<th>Revision ID for Silicon Revision(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>A1</td>
</tr>
<tr>
<td>PIC32MZ0512EFE100</td>
<td>0x720B053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ0512EFF100</td>
<td>0x7210053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ0512EFK100</td>
<td>0x7238053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFE100</td>
<td>0x720C053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFF100</td>
<td>0x7211053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFK100</td>
<td>0x7239053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFG100</td>
<td>0x720D053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFH100</td>
<td>0x7212053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFM100</td>
<td>0x723A053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2048EFG100</td>
<td>0x720E053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2048EFH100</td>
<td>0x7213053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2048EFM100</td>
<td>0x723B053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ0512EFE124</td>
<td>0x7215053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ0512EFF124</td>
<td>0x721A053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ0512EFK124</td>
<td>0x7242053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFE124</td>
<td>0x7216053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFF124</td>
<td>0x721B053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFK124</td>
<td>0x7243053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFG124</td>
<td>0x7217053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFH124</td>
<td>0x721C053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFM124</td>
<td>0x7244053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2048EFG124</td>
<td>0x7218053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2048EFH124</td>
<td>0x721D053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2048EFM124</td>
<td>0x7245053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ0512EFE144</td>
<td>0x721F053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ0512EFF144</td>
<td>0x7224053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ0512EFK144</td>
<td>0x724C053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFE144</td>
<td>0x7220053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFF144</td>
<td>0x7225053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFK144</td>
<td>0x724D053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFG144</td>
<td>0x7221053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFH144</td>
<td>0x7226053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ1024EFM144</td>
<td>0x724E053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2048EFG144</td>
<td>0x7222053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2048EFH144</td>
<td>0x7227053</td>
<td></td>
</tr>
<tr>
<td>PIC32MZ2048EFM144</td>
<td>0x724F053</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Refer to the “Memory Organization” and “Special Features” chapters in the current Device Data Sheet (DS60001320D) for detailed information on Device and Revision IDs for your specific device.
### TABLE 2: SILICON ISSUE SUMMARY

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Issue</th>
<th>Issue Summary</th>
<th>Affected Revisions$^{(1)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillator</td>
<td>Reference Clock</td>
<td>1.</td>
<td>The Reference Clock cannot divide input frequencies greater than 100 MHz.</td>
<td>X X</td>
</tr>
<tr>
<td>Oscillator</td>
<td>Primary Oscillator Crystal</td>
<td>2.</td>
<td>Revision A1 Silicon: A crystal oscillator cannot be used as an input to the Primary Oscillator (OSC1/OSC2 pins).</td>
<td>X X</td>
</tr>
<tr>
<td>Oscillator</td>
<td>FRC Tuning</td>
<td>3.</td>
<td>Revision A3 Silicon: The Primary Oscillator has been tested in a normal power-up sequence and supports specific crystal operation.</td>
<td>X X</td>
</tr>
<tr>
<td>Secondary Oscillator</td>
<td>Crystal Use</td>
<td>4.</td>
<td>The Secondary Oscillator (Sosc) does not support crystal operation.</td>
<td>X X</td>
</tr>
<tr>
<td>Power-Saving</td>
<td>PMD bits</td>
<td>5.</td>
<td>Turning off REFCLK through the PMD bits causes unpredictable device behavior.</td>
<td>X X</td>
</tr>
<tr>
<td>I^2C</td>
<td>—</td>
<td>6.</td>
<td>The I^2C module does not function reliably under certain conditions.</td>
<td>X X</td>
</tr>
<tr>
<td>UART</td>
<td>Auto-baud</td>
<td>7.</td>
<td>The Auto-baud feature does not function to set the baud rate.</td>
<td>X X</td>
</tr>
<tr>
<td>UART</td>
<td>Synchronization</td>
<td>8.</td>
<td>On a RX FIFO overflow, shift registers stop receiving data, which causes the UART to lose synchronization.</td>
<td>X X</td>
</tr>
<tr>
<td>USB</td>
<td>Suspend Mode</td>
<td>9.</td>
<td>The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to '1'.</td>
<td>X X</td>
</tr>
<tr>
<td>Power-Saving</td>
<td>Sleep Mode</td>
<td>10.</td>
<td>The device may not exit Sleep mode.</td>
<td>X X</td>
</tr>
<tr>
<td>ADC</td>
<td>Digital Filters</td>
<td>11.</td>
<td>Using multiple digital filters may result in data not being captured accurately.</td>
<td>X X</td>
</tr>
<tr>
<td>ADC</td>
<td>Level Trigger</td>
<td>12.</td>
<td>The ADC level trigger will not perform burst conversions in Debug mode.</td>
<td>X X</td>
</tr>
<tr>
<td>ADC</td>
<td>DNL</td>
<td>13.</td>
<td>In Differential mode, DNL for code 3072 is out of specification.</td>
<td>X X</td>
</tr>
<tr>
<td>ADC</td>
<td>Low-voltage Operation</td>
<td>14.</td>
<td>When the operating voltage (VDD/AVDD) is below 2.5V (i.e., charge pumps are ON), only one ADC core can be used.</td>
<td>X X</td>
</tr>
<tr>
<td>ADC</td>
<td>Turbo Mode</td>
<td>15.</td>
<td>Turbo mode is not functional.</td>
<td>X X</td>
</tr>
<tr>
<td>USB</td>
<td>Resume</td>
<td>16.</td>
<td>The USB module does not support remote wake-up.</td>
<td>X X</td>
</tr>
<tr>
<td>Oscillator</td>
<td>External Clock Mode</td>
<td>17.</td>
<td>The EC mode timing specifications for the Primary Oscillator (Posc) are not met.</td>
<td>X</td>
</tr>
<tr>
<td>Temperature Sensor</td>
<td>—</td>
<td>18.</td>
<td>The Temperature Sensor does not function.</td>
<td>X X</td>
</tr>
</tbody>
</table>

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.
Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A3).

1. Module: Oscillator

The Reference Module cannot divide input frequencies greater than 100 MHz. Therefore, SYSCLK cannot be divided if the SYSCLK operates at frequencies greater than 100 MHz.

Work around

Instead of using SYSCLK, use PBCLK1 as the input, which is limited to 100 MHz and is synchronized to SYSCLK.

Alternatively, do not divide the SYSCLK and allow the destination peripheral (i.e., SQI, SPI) to divide it as needed. To do this, set the ROTRIM<8:0> bits and the RODIV<14:0> bits to ‘0’.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th></th>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

2. Module: Oscillator

Revision A1 Silicon: A crystal oscillator cannot be used as an input to the Primary Oscillator (Posc) pins OSC1 and OSC2.

Revision A1 Silicon Work around

Use an external clock or the Internal FRC Oscillator.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th></th>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Revision A3 Silicon: The Posc has been tested in a normal power-up sequence and supports specific crystal operation.

Revision A3 Silicon Work around 1

The Primary Oscillator (Posc) has been characterized to operate at 8 MHz, 12 MHz, and 24 MHz when the circuit in Figure 1 is implemented, and the operating conditions listed in Table 3 are met.

**FIGURE 1: POSC CRYSTAL CIRCUIT**

**TABLE 3: CRYSTAL SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Crystal Frequency (see Note 1)</th>
<th>Series Resistor (Rs)</th>
<th>Posc Gain Setting POSCGAIN&lt;1:0&gt; (DEVCFG0&lt;20:19&gt;)</th>
<th>Posc Boost Setting POSCBOOST (DEVCFG0&lt;21&gt;)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 MHz</td>
<td>2 kΩ</td>
<td>'0b000 (GAIN_0)</td>
<td>'0b1 (ON)</td>
</tr>
<tr>
<td>12 MHz</td>
<td>1 kΩ</td>
<td>'0b000 (GAIN_0)</td>
<td>'0b1 (ON)</td>
</tr>
<tr>
<td>24 MHz</td>
<td>0 kΩ</td>
<td>'0b000 (GAIN_0)</td>
<td>'0b1 (ON)</td>
</tr>
</tbody>
</table>

Note: Using any other crystal frequency will require special component selection and characterization.

2: A parallel resistor (Rp) should not be used to increase the gain of the POSC.

Revision A3 Silicon Work around 2

Alternatively, use an external clock or the Internal FRC oscillator.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th></th>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
3. Module: Oscillator

The OSCTUN register only increases the frequency of the FRC, which results in the TUN<5:0> bits (OSCTUN<5:0>) functioning as follows:

- **TUN<5:0>:** FRC Oscillator Tuning bits
  - 111111 = Center frequency +4%
  - 111110 =
  - •
  - •
  - 000001 =
  - 000000 = Center frequency; Oscillator runs at nominal frequency (8 MHz)

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

4. Module: Secondary Oscillator

A crystal oscillator cannot be used as the input to the Secondary Oscillator (Sosc) pins SOSCI and SOSCO.

**Silicon Work around**
Use an external clock source (32,768 Hz) applied to the SOSCO pin with the FSOSCN bit (DEVCFG1<6>) set to ‘0’ (i.e., the Sosc is disabled through the Configuration Word) for a real-time clock base; otherwise, use the internal LPRC for non-precision requirements.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

5. Module: Power-Saving

Turning off the REFCLK modules through the PMD bits causes unpredictable behavior.

**Work around**
None. Do not disable the REFCLK modules through the PMD bits.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

6. Module: I²C

Indeterminate I²C module behavior may result when data rates > 100 kHz and/or continuous sequential data transfers > 500 bytes are used. The potential false intermittent error signals can result in one of the following error conditions, which are listed in order of decreasing frequency:

- **False Error Condition 1:**
  - False Master Bus Collision Detect (Master-mode only) – The error is indicated through the BCL bit (I2CxSTAT<10>).
- **False Error Condition 2:**
  - Receive Overflow (Master or Slave modes) – The error is indicated through the I2COV bit (I2CxSTAT<20>).
- **False Error Condition 3:**
  - Suspended I²C Module Operations (Master or Slave modes) – I²C transactions in progress are inadvertently suspended without error indications.

**Revision A1 Silicon Work around 1**

**False Error Condition 1:**
Clear the Master Bus Collision Detect (BCL bit (I2CxSTAT<10>), after the bus returns to an Idle state. The software can monitor the S bit (I2CxSTAT<3>) and the P bit (I2CxSTAT<4>) to wait for an Idle bus. When the software services the bus collision Interrupt Service Routine and the I²C bus is free, the software can resume communication by asserting a new Start condition.

**False Error Condition 2:**
Clear the Receive Overflow Status flag I2COV bit (I2CxSTAT<20>), and then resume normal operation.

**Note:** All three false error conditions are recoverable in software.
False Error Condition 3:
First, initialize a Timer to slightly greater than the worst case I2C transaction cycle, (i.e., from Start-to-Stop, including the sum of all other application PC flow latencies, calls, interrupts, etc.). Exact timing is not required, rather just long enough so that a normal transaction is not interrupted. Prior to the beginning of each transaction, start the timer. Be sure to stop and reset the timer after completion of each successful I2C transaction.

Then, during the Timer interrupt (meaning the I2C transaction has timed out), disable the I2C module by setting the ON bit (I2CxCON<15>) = 0. After disabling the module, wait 4 instruction cycles, after which time the I2CxSTAT register will automatically be cleared. Then, re-enable the I2C module by setting the ON bit = 1 and resume normal operation.

Revision A1 Silicon Work around 2
Instead of using the hardware I2C module, use a software “bit-bang” implementation.

Revision A3 Silicon Work around
The work arounds described for revision A1 silicon will also work for silicon revision A3, with the exception of I2C3, as I2C3 must use a software “bit-bang” implementation.

Affected Silicon Revisions

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>A3</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Module: UART
During a RX FIFO overflow condition, the shift register stops receiving data. This causes the UART to lose synchronization with the serial data stream. The only way to recover from this is to turn the UART OFF and ON until it synchronizes. This could require several OFF/ON sequences.

Work arounds

Work around 1:
Avoid the RX overrun condition by ensuring that the UARTx module has a high enough interrupt priority such that other peripheral interrupt processing latencies do not exceed the time to overrun the UART RX buffer based on the application baud rate. Alternately or in addition to, set the URXISEL bits in the UxSTA register to generate an earlier RX interrupt based on RX FIFO fill status to buy more time for interrupt latency processing requirements.

Work around 2:
If avoiding RX FIFO overruns is not possible, implement an ACK/NAK software handshake protocol to repeat lost packet transfers after restoring the UART synchronization.

Affected Silicon Revisions

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>A3</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Module: USB
The USB module will not function if the device enters Sleep mode and the USB PHY is turned off by setting the USBSSEN bit in the CFGCON register to ‘1’.

Work around
Keep the USB PHY operational in Sleep mode by setting the USBSSEN bit to ‘0’.

Affected Silicon Revisions

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>A3</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
10. Module: Power-Saving Modes
The device may not exit Sleep mode when Flash is powered down through the FSLEEP bit in the DEVCFG0/ADEVCFG0 Configuration register.

Work around
Enable Flash in Sleep mode by clearing the Flash Sleep Mode Configuration bit, FSLEEP, in the DEVCFG0/ADEVCFG0 Configuration register.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

11. Module: ADC
When using multiple digital filters, the filters may not capture data correctly when the assigned data sources are ready at the same time.

Work around
Only one digital filter may be used at a time.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

12. Module: ADC
The ADC level trigger will not perform burst conversions in Debug mode.

Work around
Do not use Debug mode with the ADC level trigger.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

13. Module: ADC
In Differential mode, code 3072 has a DNL of +3.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

14. Module: ADC
When the operating voltage (VDD/AVDD) is below 2.5V (i.e., charge pumps are ON), only one ADC core can be used.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

15. Module: ADC
Turbo mode is not functional when two channels are linked for the purpose of increasing throughput.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

16. Module: USB
The USB module does not support remote wake-up through the USBRIE bit (USBCRCON<1>).

Work around
None.

USB descriptors must inform the host that the device does not support remote wake-up.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
17. Module: Oscillator

The Primary Oscillator in EC mode only functions up to 24 MHz

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

18. Module: Temperature Sensor

The Temperature Sensor does not function.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001320D):

**Note:** Corrections in tables are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

### 1. Module: Resets

Deleted the General NMI (GNMI) bit from **Register 6-3**. This bit is not available for either triggering an NMI event or for reflecting the status of the NMIKEY bit (INTCON<31:24>), which is also removed.

**REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER**

<table>
<thead>
<tr>
<th>Bit Range</th>
<th>Bit 31/23/15/7</th>
<th>Bit 30/22/14/6</th>
<th>Bit 29/21/13/5</th>
<th>Bit 28/20/12/4</th>
<th>Bit 27/19/11/3</th>
<th>Bit 26/18/10/2</th>
<th>Bit 25/17/9/1</th>
<th>Bit 24/16/8/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>23:16</td>
<td>R/W-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>15:8</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td>7:0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
</tbody>
</table>

Legend:

- **R** = Readable bit  
- **W** = Writable bit  
- **U** = Unimplemented bit, read as ‘0’  
- **-n** = Value at POR  
- ‘1’ = Bit is set  
- ‘0’ = Bit is cleared  
- **x** = Bit is unknown

**bit 31-26 Unimplemented:** Read as ‘0’

- **bit 25 DMTO:** Deadman Timer Time-out Flag bit  
  - 1 = DMT time-out has occurred and caused a NMI  
  - 0 = DMT time-out has not occurred  
  Setting this bit will cause a DMT NMI event, and NMICNT will begin counting.

- **bit 24 WDTO:** Watchdog Timer Time-Out Flag bit  
  - 1 = WDT time-out has occurred and caused a NMI  
  - 0 = WDT time-out has not occurred  
  Setting this bit will cause a WDT NMI event, and NMICNT will begin counting.

- **bit 23 SWNMI:** Software NMI Trigger.  
  - 1 = An NMI will be generated  
  - 0 = An NMI will not be generated  

- **bit 22-18 Unimplemented:** Read as ‘0’

**Note 1:** When a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is triggered, the NMICNT bit will start decrementing. When the NMICNT bit reaches zero, the device is Reset. This NMI reset counter is only applicable to these two specific NMI events.

**Note:** The system unlock sequence must be performed before the SWRST bit can be written. Refer to Section 42. “Oscillators with Enhanced PLL” in the “PIC32 Family Reference Manual” for details.
REGISTER 6-3: RNMICON: NON-MASKABLE INTERRUPT (NMI) CONTROL REGISTER
(CONTINUED) (CONTINUED) (CONTINUED)

bit 17  CF: Clock Fail Detect bit
1 = FSCM has detected clock failure and caused an NMI
0 = FSCM has not detected clock failure
Setting this bit will cause a CF NMI event, but will not cause a clock switch to the BFRC.

bit 16  WDTS: Watchdog Timer Time-out in Sleep Mode Flag bit
1 = WDT time-out has occurred during Sleep mode and caused a wake-up from sleep
0 = WDT time-out has not occurred during Sleep mode
Setting this bit will cause a WDT NMI.

bit 15-0  NMICNT<15:0>: NMI Reset Counter Value bits
1111111111111111-0000000000000001 = Number of SYSCLK cycles before a device Reset occurs
0000000000000000 = No delay between NMI assertion and device Reset event

Note 1: When a Watchdog Timer NMI event (when not in Sleep mode) or a Deadman Timer NMI event is triggered, the NMICNT bit will start decrementing. When the NMICNT bit reaches zero, the device is Reset. This NMI reset counter is only applicable to these two specific NMI events.

Note: The system unlock sequence must be performed before the SWRST bit can be written. Refer to Section 42. “Oscillators with Enhanced PLL” in the “PIC32 Family Reference Manual” for details.
## Module: Interrupt Controller

Deleted the NMIKEY<7:0> bit from Register 7-1. The ability to trigger an NMI event through the NMIKEY field is not available, and the corresponding status bit GNMI (RNMICON<19>) is also not available.

### REGISTER 7-1: INTCON: INTERRUPT CONTROL REGISTER

<table>
<thead>
<tr>
<th>Bit Range</th>
<th>Bit 31/23/15/7</th>
<th>Bit 30/22/14/6</th>
<th>Bit 29/21/13/5</th>
<th>Bit 28/20/12/4</th>
<th>Bit 27/19/11/3</th>
<th>Bit 26/18/10/2</th>
<th>Bit 25/17/9/1</th>
<th>Bit 24/16/8/0</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
</tr>
<tr>
<td>23:16</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
<td>U-0 U-0 U-0 U-0</td>
</tr>
<tr>
<td>15:8</td>
<td>U-0 U-0 U-0 R/W-0</td>
<td>U-0 R/W-0 R/W-0 R/W-0</td>
<td>R/W-0 R/W-0 R/W-0 R/W-0</td>
<td>R/W-0 R/W-0 R/W-0 R/W-0</td>
<td>R/W-0 R/W-0 R/W-0 R/W-0</td>
<td>R/W-0 R/W-0 R/W-0 R/W-0</td>
<td>R/W-0 R/W-0 R/W-0 R/W-0</td>
<td>R/W-0 R/W-0 R/W-0 R/W-0</td>
</tr>
<tr>
<td>7:0</td>
<td>U-0 U-0 U-0 R/W-0</td>
<td>R/W-0 R/W-0 R/W-0 R/W-0</td>
<td>R/W-0 R/W-0 R/W-0 R/W-0</td>
<td>R/W-0 R/W-0 R/W-0 R/W-0</td>
<td>R/W-0 R/W-0 R/W-0 R/W-0</td>
<td>R/W-0 R/W-0 R/W-0 R/W-0</td>
<td>R/W-0 R/W-0 R/W-0 R/W-0</td>
<td>R/W-0 R/W-0 R/W-0 R/W-0</td>
</tr>
</tbody>
</table>

**Legend:**
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR ‘1’ = Bit is set ‘0’ = Bit is cleared x = Bit is unknown

bit 31-13 **Unimplemented:** Read as ‘0’

bit 12 **MVEC:** Multi Vector Configuration bit
- 1 = Interrupt controller configured for multi vectored mode
- 0 = Interrupt controller configured for single vectored mode

bit 11 **Unimplemented:** Read as ‘0’

bit 10-8 **TPC<2:0>:** Interrupt Proximity Timer Control bits
- 111 = Interrupts of group priority 7 or lower start the Interrupt Proximity timer
- 110 = Interrupts of group priority 6 or lower start the Interrupt Proximity timer
- 101 = Interrupts of group priority 5 or lower start the Interrupt Proximity timer
- 100 = Interrupts of group priority 4 or lower start the Interrupt Proximity timer
- 011 = Interrupts of group priority 3 or lower start the Interrupt Proximity timer
- 010 = Interrupts of group priority 2 or lower start the Interrupt Proximity timer
- 001 = Interrupts of group priority 1 start the Interrupt Proximity timer
- 000 = Disables Interrupt Proximity timer

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **INT4EP:** External Interrupt 4 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge

bit 3 **INT3EP:** External Interrupt 3 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge

bit 2 **INT2EP:** External Interrupt 2 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge

bit 1 **INT1EP:** External Interrupt 1 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge

bit 0 **INT0EP:** External Interrupt 0 Edge Polarity Control bit
- 1 = Rising edge
- 0 = Falling edge
3. Module: External Clock Timing

Requirements

The Fosc signal maximum frequency in parameter OS10 was incorrectly stated in the current data sheet. The following table shows the correct maximum value.

### TABLE 37-17: EXTERNAL CLOCK TIMING REQUIREMENTS

<table>
<thead>
<tr>
<th>AC CHARACTERISTICS</th>
<th>Standard Operating Conditions: 2.1V to 3.6V (unless otherwise stated)</th>
<th>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended</th>
</tr>
</thead>
<tbody>
<tr>
<td>Param. No.</td>
<td>Symbol</td>
<td>Characteristics</td>
</tr>
<tr>
<td>OS10</td>
<td>Fosc</td>
<td>External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)</td>
</tr>
</tbody>
</table>

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are characterized but are not tested.

2: This parameter is characterized, but not tested in manufacturing.

3: See parameter OS50 for PLL input frequency limitations.
APPENDIX A: REVISION HISTORY

Rev A Document (7/2015)
Initial release of this document issued for revision A1 silicon, which includes silicon issues
1. Module: (Oscillator),
2. Module: (Oscillator),
3. Module: (Oscillator),
4. Module: (Secondary Oscillator),
5. Module: (Power-Saving),
6. Module: (I2C),
7. Module: (UART),
8. Module: (UART),
9. Module: (USB), and
Power-Saving Modes.

Added silicon issues 11. Module: (ADC) and 12. Module: (ADC).
Updated silicon issues 2. Module: (Oscillator) and 10. Module: (Power-Saving Modes).

Rev C Document (7/2016)
Updated to include silicon revision A3.
Added data sheet clarifications 1. Module: (Resets) and 2. Module: (Interrupt Controller).

Rev D Document (9/2016)
Updated Figure 1 and Table 3 in silicon issue 2. Module: (Oscillator).
Added silicon issues 17. Module: (Oscillator) and 18. Module: (Temperature Sensor).
Added data sheet clarification 3. Module: (External Clock Timing Requirements).
Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continually improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, dsPIC, FlashFlex, flexPWR, Helda, JukeBlox, KeeLoq, KeeLoq logo, Kleer, LANCheck, LINK MD, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC32 logo, RightTouch, SpyNIC, SST, SST logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, ETHERSYNCH, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and QUIET-WIRE are registered trademarks ofMicrochip Technology Incorporated in the U.S.A.


SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2015-2016, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.
ISBN: 978-1-5224-0972-4

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company’s quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KeeLoq® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV

ISO/TS 16949
Worldwide Sales and Service

AMERICAS
Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support: http://www.microchip.com/support
Web Address: www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Austin, TX
Tel: 512-257-3370

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Novi, MI
Tel: 248-848-4000

Houston, TX
Tel: 281-894-5983

Indianapolis
Noblesville, IN
Tel: 317-773-8323
Fax: 317-773-5453

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

New York, NY
Tel: 631-435-6000

San Jose, CA
Tel: 408-735-9110

Canada - Toronto
Tel: 905-695-1980
Fax: 905-695-2078

ASIA/PACIFIC
Asia Pacific Office
Suits 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon

Hong Kong
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Beijing
Tel: 86-10-8569-7000
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Dongguan
Tel: 86-769-8702-9880

China - Guangzhou
Tel: 86-20-8755-8029

China - Hangzhou
Tel: 86-571-8792-8115
Fax: 86-571-8792-8116

China - Hong Kong SAR
Tel: 852-2943-5100
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8864-2200
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

ASIA/PACIFIC
China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-3019-1500

Japan - Osaka
Tel: 81-6-6152-7160
Fax: 81-6-6152-9310

Japan - Tokyo
Tel: 81-3-6880-3770
Fax: 81-3-6880-3771

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or 82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-5778-936
Fax: 886-3-5770-955

Taiwan - Kaohsiung
Tel: 886-7-213-7282

Taiwan - Taipei
Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE
Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4450-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Dusseldorf
Tel: 49-2129-376600

Germany - Karlsruhe
Tel: 49-721-625370

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Italy - Venice
Tel: 39-049-7625286

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Poland - Warsaw
Tel: 48-22-3325737

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

Sweden - Stockholm
Tel: 46-8-5090-4654

UK - Wokingham
Tel: 44-118-921-5800
Fax: 44-118-921-5820

06/23/16