This document describes known anomalies for all functional revisions of the USB331x device.

**TABLE 1: SILICON ISSUE SUMMARY**

<table>
<thead>
<tr>
<th>Hardware Functional Rev A</th>
<th>Hardware Functional Rev B</th>
<th>Hardware Functional Rev C</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Module 1: “HS J/K Amplitude”</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Module 2: “Scratch Register “Set” and “Clear” Does Not Function Correctly”</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Module 3: “Carkit Mode Interrupt Pin Non-Functional”</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Module 4: “VDD1.8 Current in Suspend Mode”</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Module 5: “RID Converter Cannot Detect 440K Resistor”</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Module 6: “Datasheet Correction: Power Sequencing (Variable I/O Devices Only)”</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Module 7: “Datasheet Correction: HS TX Boost Setting “01b””</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Module 8: “Intermittent Loss of USB Link in OMAP4 Host Applications”</td>
</tr>
</tbody>
</table>

Legend:  X = Applicable to the Functional Rev.

**Silicon Errata Issue**

**Module 1: HS J/K Amplitude**

**Description**
The nominal HS J/K Amplitude measures 2% low.

**End User Implications**
In extremely limited cases, the customer may have trouble meeting HS Eye compliance based on applications where flex cables, EMI chokes, ESD circuits, etc. are placed in the path of the USB lines.

**Solution**
Use the “hs_drive” bits in Internal Test Register 1 to increase the HS Eye current by 3.5%.

**Plan**
This anomaly has been fixed in functional revision B devices and newer devices.

**Module 2: Scratch Register “Set” and “Clear” Does Not Function Correctly**

**Description**
The Scratch register set and clear do not function correctly. However, the read and write operations work correctly.

**End User Implications**
The Link will not be able to use this register to debug register clear operations. This register is not used for USB operation and is only used for Link Hardware design and debug.

**Solution**
None needed for USB operation. The Link should avoid all sets and clears to the Scratch register during debug.
Plan
This will not be addressed in a future revision of the device.

Module 3: Carkit Mode Interrupt Pin Non-Functional

Description
When the USB331x operates in Carkit Mode, the DATA[3] interrupt pin is not functional. When an unmasked interrupt is generated, the interrupt will not be indicated on DATA[3].

End User Implications
The USB331x will not signal any interrupts to the Link when using the Carkit Mode. The switches and UART interface are still functional and their operation is not affected.

Solution
The USB331x provides a Headset Audio mode where the interrupts are visible on the ULPI bus. In the Headset Audio mode the ULPI interface is redefined to indicate the status of the interrupt signals. Please consult SMSC sales and Marketing for details on the Headset Audio mode.

There is no known workaround in the USB UART mode.

Plan
This will not be addressed in a future revision of the device.

Module 4: VDD1.8 Current in Suspend Mode

Description
The VBAT (VDD3.3) pin may draw up to 1.3mA of current from the VBAT source when all of the following conditions apply:
1. The VDD1.8 supply is removed.
2. The VBAT supply is ON.

In this mode the VBAT (VDD3.3) pin should draw ≤ 25 μA.

Table 2 details which USB331x power combination modes are affected by this anomaly:

<table>
<thead>
<tr>
<th>Power Combo</th>
<th>VBUS</th>
<th>VBAT/ VDD3.3</th>
<th>VDD1.8</th>
<th>Note</th>
<th>Affected by Anomaly</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>PHY is off</td>
<td>NO</td>
</tr>
<tr>
<td>2</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>PHY is off, USB cable connected. VBUS current will be approximately 1 μA.</td>
<td>NO</td>
</tr>
<tr>
<td>3</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ULPI registers can be read and maintain their contents as long as the RESETB pin is held high. The PHY can be placed in low power mode via the ULPI interface.</td>
<td>NO</td>
</tr>
<tr>
<td>4</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>Same as line 3 above, but the USB cable connection has been made. VBUS current will be approximately 1 μA.</td>
<td>NO</td>
</tr>
<tr>
<td>5</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>Normal operating mode of the PHY when a USB cable connection is not made.</td>
<td>NO</td>
</tr>
<tr>
<td>6</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>Normal operating mode of the PHY.</td>
<td>NO</td>
</tr>
<tr>
<td>7</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ULPI interface not functional.</td>
<td>YES</td>
</tr>
<tr>
<td>8</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>ULPI interface not functional.</td>
<td>YES</td>
</tr>
</tbody>
</table>
For power combinations where VBUS, VBAT, and VDD3.3 turn on together, Table 3 details the modes affected by this anomaly:

**TABLE 3: TWO RAIL POWER COMBINATIONS**

<table>
<thead>
<tr>
<th>Power Combo</th>
<th>VBUS, VBAT, VDD3.3</th>
<th>VDD1.8</th>
<th>Note</th>
<th>Affected by Anomaly</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OFF</td>
<td>OFF</td>
<td></td>
<td>NO</td>
</tr>
<tr>
<td>2</td>
<td>OFF</td>
<td>ON</td>
<td>ULPI registers can be read and maintain their contents as long as the RESETB pin is held high. The PHY can be placed in low power mode via the ULPI interface.</td>
<td>NO</td>
</tr>
<tr>
<td>3</td>
<td>ON</td>
<td>ON</td>
<td>Normal operating mode of the PHY.</td>
<td>NO</td>
</tr>
<tr>
<td>4</td>
<td>ON</td>
<td>OFF</td>
<td>ULPI interface not functional.</td>
<td>YES</td>
</tr>
</tbody>
</table>

**End User Implications**

Removing supply voltage from both VBAT and VDD1.8 produces a leakage current of 0 μA. If the customer elects to leave VBAT on while VDD1.8V is off, the USB331x may exhibit increased current draw (>25 μA) from the VBAT (VDD3.3) supply when in Suspend Mode. USB functionality is not affected.

**Solution**

- Leave the VDD1.8 supply ON whenever voltage is applied to VBAT. Standby current will be ≤ 25 μA.
- Supply voltage on VBAT from a PMIC and switch it off whenever VDD1.8 is switched off. Standby current will be 0 μA.
- Add a LDO regulator with enable between VBAT and the battery which can be switched off whenever VDD1.8 is switched off. Standby current will be 0 μA.
- Add a resistor divider between VDD3.3 and VDD1.8 supplies, as shown in Figure 1:

**FIGURE 1: RESISTOR DIVIDER CIRCUIT**

![Resistor Divider Circuit Diagram]

Where:

R1 = 210 kΩ 1%
R2 = 309 kΩ 1%

**Note:** If there are other devices attached to the 1.8V on the customer platform, those device impedances need to be taken into account.

Standby current will be ≤ 30 μA.

**Plan**

This anomaly has been fixed in functional revision C devices and newer devices.
Module 5:  RID Converter Cannot Detect 440K Resistor

**Description**
The RID Converter does not reliably detect a 440K resistor. An “ID Floating” condition may be reported to the Vendor RID Conversion register and the CarKit Interrupt Status register.

**End User Implications**
The USB331x will not reliably discern the difference between a 440K ohm resistor on the ID pin and a floating ID pin. Other RID converter conversion values are still functional and their operation is not affected.

**Solution**
None.

**Plan**
This will not be addressed in a future revision of the device.

Module 6:  Datasheet Correction: Power Sequencing (Variable I/O Devices Only)

**Description**
In the USB3315, USB3317, and USB3318 Rev 2.0 Datasheets, Note 5.3 is incorrect. In the USB3313D Datasheet, Note 5.2 is incorrect. These notes state “VDDIO must be powered to tri-state the ULPI interface in this configuration”. In practice, VDDIO must never be left ON while VDD18 is OFF.

**End User Implications**
Customers should ignore Datasheet Note 5.3 for the USB3315/USB3317/USB3318 products (Datasheet Note 5.2 for the USB3313). As stated in Table 3.1 of the datasheet, customers should never apply >0.7V to VDDIO when no voltage is supplied to VDD18. Similarly, Section 5.5.3 of the datasheet states that the “VDDIO supply should be powered up at the same time or after the VDD18 supply is turned on and stable”.

**Solution**
None.

**Plan**
A future revision of the USB3315/USB3317/USB3318 datasheets will remove Note 5.3. A future revision of the USB3313 datasheet will remove Note 5.2.

Module 7:  Datasheet Correction: HS TX Boost Setting “01b”

**Description**
In all Rev B and Rev C product datasheets, the HS TX Boost register defines a '01b' option which “Enables 3.7% decreased drive strength”. This option is now defeatured.

**End User Implications**
Customers should not set bits [6:5] in the HS TX Boost register to value '01b'. The other three options are still valid. This value is now “Reserved”.

**Solution**
None.

**Plan**
A future revision of the USB331x datasheets will remove this HS TX Boost option.

Module 8:  Intermittent Loss of USB Link in OMAP4 Host Applications

**Description**
This anomaly may apply to any host USB link when ALL of the following conditions apply:
1. The USB331x is a connected to a USB Host (EHCI or OTG controller) via ULPI and operates as a USB Host Transceiver.
2. The USB331x is moved from High Speed configuration to Full Speed by removing the HS terminations and the SuspendM == 1.
In some applications where the Texas Instruments OMAP4 is the USB Host and connects to the USB331x via
ULPI, the OMAP4 can periodically lose the connection with the downstream device when attempting to suspend
the USB connection. The root cause of this is that the OMAP EHCI controller can lock up when entering USB
Suspend, even if the OMAP properly puts the USB331x into Low Power Mode. In the ULPI suspend signaling
definition in the ULPI specification and in the majority of SoC’s, the command to suspend the USB Transceiver
and the command to change to the USB Transceiver’s Full Speed receivers arrives in a single register command.
The OMAP4 places a delay (3ms) between these commands because the OMAP4 is waiting for the downstream
USB device to assert its 1.5K pull-up on DP (indicating that the downstream device is in USB suspend). During
this 3ms delay, noise on the DP and DM USB signals can cause a significant number of RX CMDs and Receive
data packets to be transmitted by the USB331x. As a result, the OMAP EHCI controller may miss the status
update required to initiate the command to put the PHY into low power mode and place the OMAP4 EHCI con-
troller into the USB Suspend state.

In the OMAP EHCI controller, the Suspend bit becomes '0' by writing to the Resume bit, waiting for >20ms, and
then clearing the Resume bit to stop Resume signaling on bus. If the bus has resumed into HS-IDLE mode, then
the Suspend bit will be automatically cleared. Under the conditions of this anomaly, the Resume Bit does not clear
at all - it remains stuck at value '1'. This behavior is the signature of this anomaly.

**End User Implications**
The customer's application will not be able to recover from USB Suspend and will lose communication with the
downstream USB device.

**Solution**
1. The host SoC should command the USB331x to enable Full Speed Transceivers and enter Low Power Mode
   with a single command (TX CMD = 0x05h). Do not split these two steps into separate TX CMDs. The downstream
   USB device will always enter USB suspend when this work around is used.
   If the Function Control Register (04h-06h) is written immediately after the Port Suspend bit is set and the XcvrSe-
   lect bits are set back to 00, the noise will be eliminated:

   **Note:** The squelch threshold may need to be adjusted through the Varisense bits in the HS Compensation Reg-
   ister (31h) to ensure that the correct status update still occurs.

2. If port resume bit on the EHCI port is not cleared in the OMAP upon attempted entry to USB suspend, then the
   OMAP EHCI controller failed to enter suspend. If the USB331x was suspended successfully (clearing the Sus-
   pendM bit in the Function Control Register), then the OMAP must assert either:
   - STP to bring the USB331x out of Low Power Mode or:
   - Toggle RESETB on the USB331x

3. To reduce USB noise during the undefined state prior to entering Low Power Mode, assert the ChargerPullupEn-
   ableDP or ChargerPullupEnableDM bits. Only assert one of these two bits. In applications with very low noise on
   USB signals DP and DM, this can provide a robust workaround to this anomaly:
   - **ChargerPullupEnDP/DM (Bits 4 and 5 of register 39h)** - These bits connect a 125k pull up resistor to the
     3.3V supply of the PHY, or inject ~20uA of current onto the desired pin.

**Plan**
This will not be addressed in a future revision of the device.
APPENDIX A: DOCUMENT REVISION HISTORY

<table>
<thead>
<tr>
<th>Revision Level &amp; Date</th>
<th>Section/Figure/Entry</th>
<th>Correction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rev A (April 2015)</td>
<td></td>
<td>Initial release</td>
</tr>
</tbody>
</table>

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