The PIC16(L)F1824/1828 family devices that you have received conform functionally to the current Device Data Sheet (DS40001419E), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1824/1828 silicon.

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select Programmer > Reconnect.
   b) For MPLAB X IDE, select Window > Dashboard and click the Refresh Debug Tool Status icon ( ).
5. Depending on the development tool used, the part number and Device Revision ID value appear in the Output window.

The DEVREV values for the various PIC16(L)F1824/1828 silicon revisions are shown in Table 1.
### TABLE 2: SILICON ISSUE SUMMARY

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Item Number</th>
<th>Issue Summary</th>
<th>Affected Revisions (1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>ADC Conversion</td>
<td>1.1</td>
<td>ADC Conversion may not complete.</td>
<td>X</td>
</tr>
<tr>
<td>Oscillator</td>
<td>HS Oscillator</td>
<td>2.1</td>
<td>HS Oscillator min. VDD.</td>
<td>X</td>
</tr>
<tr>
<td>Oscillator</td>
<td>Clock Switching</td>
<td>2.2</td>
<td>Clock switching can cause a single corrupted instruction.</td>
<td>X X</td>
</tr>
<tr>
<td>Oscillator</td>
<td>Oscillator Start-up Timer</td>
<td>2.3</td>
<td>OSTS bit remains set.</td>
<td>X X X</td>
</tr>
<tr>
<td>Enhanced Capture Compare PWM (ECCP)</td>
<td>Enhanced PWM</td>
<td>3.1</td>
<td>PWM 0% duty cycle direction change.</td>
<td>X</td>
</tr>
<tr>
<td>Enhanced Capture Compare PWM (ECCP)</td>
<td>Enhanced PWM</td>
<td>3.2</td>
<td>PWM 0% duty cycle port steering.</td>
<td>X</td>
</tr>
<tr>
<td>Enhanced Capture Compare PWM (ECCP)</td>
<td>Capture Mode</td>
<td>3.3</td>
<td>TTL Input selection suppresses capture event (PIC16(L)F1828 devices only)</td>
<td>X X X X</td>
</tr>
<tr>
<td>Timer1</td>
<td>T1 Gate Toggle mode</td>
<td>4.1</td>
<td>T1 Gate flip-flop does not clear.</td>
<td>X</td>
</tr>
<tr>
<td>In-Circuit Serial Programming™ (ICSP™)</td>
<td>Low-Voltage Programming</td>
<td>5.1</td>
<td>Bulk Erase not available with LVP.</td>
<td>X</td>
</tr>
<tr>
<td>Clock Switching</td>
<td>OSTS Status Bit</td>
<td>6.1</td>
<td>Remains clear when 4xPLL enabled.</td>
<td>X X X X</td>
</tr>
<tr>
<td>BOR</td>
<td>Wake-up from Sleep</td>
<td>7.1</td>
<td>Device resets on wake-up from Sleep (LF devices only).</td>
<td>X X</td>
</tr>
<tr>
<td>Enhanced Universal Synchronous Asynchronous Receiver (EUSART)</td>
<td>16-Bit High-Speed Asynchronous mode</td>
<td>8.1</td>
<td>Works improperly at maximum rate.</td>
<td>X X X X</td>
</tr>
<tr>
<td>Enhanced Universal Synchronous Asynchronous Receiver (EUSART)</td>
<td>Auto-Baud Detect</td>
<td>8.2</td>
<td>Auto-Baud Detect may store incorrect count value in the SPBRG registers.</td>
<td>X X</td>
</tr>
<tr>
<td>PFM Self-Writes</td>
<td>PFM Self-Write</td>
<td>9.1</td>
<td>PFM Self-Write will not work depending on clock selection.</td>
<td>X</td>
</tr>
<tr>
<td>MSSP (Master Synchronous Serial Port)</td>
<td>SPI Master mode</td>
<td>10.1</td>
<td>Buffer Full (BF) bit or MSSP Interrupt Flag (SSPIF) bit becomes set half SCK cycle too early.</td>
<td>X X X X</td>
</tr>
</tbody>
</table>

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.
Silicon Errata Issues

**Note:** This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (A5).

1. Module: ADC

1.1 Analog-to-Digital Conversion

An ADC conversion may not complete under these conditions:

1. When Fosc is greater than 8 MHz and it is the clock source used for the ADC converter.
2. The ADC is operating from its dedicated internal FRC oscillator and the device is not in Sleep mode (any Fosc frequency).

When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the GO/DONE bit does not get cleared, and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

**Work around**

Method 1: Select the system clock, Fosc, as the ADC clock source and reduce the Fosc frequency to 8 MHz or less when performing ADC conversions.

Method 2: Select the dedicated FRC oscillator as the ADC conversion clock source and perform all conversions with the device in Sleep.

Method 3: This method is provided if the application cannot use Sleep mode and requires continuous operation at frequencies above 8 MHz. This method requires early termination of an ADC conversion. Provide a fixed time delay in software to stop the A-to-D conversion manually, after all 10 bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/DONE bit in software. The GO/DONE bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to Figure 1 for details.

**FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE**

Fosc = 32 MHz  
TCY = 4/32 MHz = 125 nsec  
TAD = 1 µsec, ADCS = Fosc/32

Stop the A/D conversion between 10.5 and 11 TAD cycles.

See the Analog-to-Digital Conversion TAD Cycles figure in the Analog-to-Digital Converter section of the data sheet.

See the ADC Clock Period (TAD) vs. Device Operating Frequencies table, in the Analog-to-Digital Converter section of the data sheet.
In Figure 1, 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of 8 TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

**Note:** The exact delay time will depend on the TAD divisor (ADCS) selection. The TCY counts shown in the timing diagram above apply to this example only. Refer to Table 3 for the required delay counts for other configurations.

**EXAMPLE 1:** CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF ADCON0, ADGO ; Start ADC conversion
 ; Provide 86 instruction cycle delay here
BCF ADCON0, ADGO ; Terminate the conversion manually
MOVF ADRESH, W ; Read conversion result
```

For other combinations of FOSC, TAD values and Instruction cycle delay counts, refer to Table 3.

**TABLE 3: INSTRUCTION CYCLE DELAY COUNTS BY TAD SELECTION**

<table>
<thead>
<tr>
<th>TAD</th>
<th>Instruction Cycle Delay Counts</th>
</tr>
</thead>
<tbody>
<tr>
<td>FOSC/64</td>
<td>172</td>
</tr>
<tr>
<td>FOSC/32</td>
<td>86</td>
</tr>
<tr>
<td>FOSC/16</td>
<td>43</td>
</tr>
</tbody>
</table>

**2. Module: Oscillator**

**2.1 HS Oscillator**

The HS oscillator requires a minimum voltage of 3.0 volts (at 65°C or less) to operate at 20 MHz.

**Work around**

None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**2.2 Clock Switching**

When switching clock sources between INTOSC clock source and an external clock source, one corrupted instruction may be executed after the switch occurs.

This issue does not affect Two-Speed Start-up or the Fail-Safe Clock Monitor operation.

**Work around**

When switching from an external oscillator clock source, first switch to 16 MHz HFINTOSC. Once running at 16 MHz HFINTOSC, configure IRCF to run at desired internal oscillator frequency.

When switching from an internal oscillator (INTOSC) to an external oscillator clock source, first switch to HFINTOSC High-Power mode (8 MHz or 16 MHz). Once running from HFINTOSC, switch to the external oscillator clock source.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2.3 Oscillator Start-up Timer

During the Two-Speed Start-up sequence, the Oscillator Start-up Timer is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as the primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer failing to restart:

• MCLR Reset
• Wake from Sleep
• Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators which take longer than the clock failure time-out period to start.

**Work around**
None.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

3. Module: Enhanced Capture Compare PWM (ECCP)

3.1 Enhanced PWM

When the PWM is configured for Full-Bridge mode and the duty cycle is set to 0%, writing the PxM<1:0> bits to change the direction has no effect on PxA and PxC outputs.

**Work around**
Increase the duty cycle to a value greater than 0% before changing directions.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3.2 Enhanced PWM

In PWM mode, when the duty cycle is set to 0% and the STRxSYNC bit is set, writing the STRxA, STRxB, STRxC and the STRxD bits to enable/disable steering to port pins has no effect on the outputs.

**Work around**
Increase the duty cycle to a value greater than 0% before enabling/disabling steering to port pins.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

3.3 Capture Mode

This issue applies to the PIC16(L)F1828 devices only.

When the input threshold control for RC6 is configured for TTL, the CCP4 capture input is ignored.

**Work around**
Use the Schmitt Trigger threshold level by setting the INVLC<6> bit.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

**Note:** All CCP Capture pins function at Schmitt Trigger logic levels. The INVLx registers apply only to PORT reads and Interrupt-on-Change.
4. Module: Timer1

4.1 Timer1 Gate Toggle mode

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal. To perform this function, the Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the gate signal. Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When working properly, clearing either the T1GTM bit or the TMR1ON bit would also clear the output value of this flip-flop, and hold it clear. This is done in order to control which edge is being measured. The issue that exists is that clearing the TMR1ON bit does not clear the output value of the flip-flop and hold it clear.

Work around
Clear the T1GTM bit in the T1GCON register to clear and hold clear the output value of the flip-flop.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

5. Module: In-Circuit Serial Programming™ (ICSP™)

5.1 Bulk Erase Feature not available with Low-Voltage Programming mode

A bulk erase of the program Flash memory or data memory cannot be executed in Low-Voltage Programming mode.

Work around

Method 1: If ICSP Low-Voltage Programming mode is required, use row erases to erase the program memory, as described in the Program/Verify mode section of the Programming Specification. Data memory must be over-written with the desired values.

Method 2: Use ICSP High-Voltage Programming mode if a bulk erase is required.

Note: Only the bulk erase feature will erase program or data memory if code or data protection is enabled. Method 2 must be used if code or data protection is enabled.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

6. Module: Clock Switching

6.1 OSTS Status Bit

When the 4xPLL is enabled, the Oscillator Start-up Time-out Status (OSTS) bit always remains clear.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
7. Module: BOR

7.1 BOR Reset

This issue affects only the PIC16LF1824/1828 devices. The device may undergo a BOR Reset when waking-up from Sleep and BOR is re-enabled. A BOR Reset may also occur the moment the software BOR is enabled.

Under certain voltage and temperature conditions and when either SBODEN or BOR_NSLEEP is selected, the devices may occasionally reset when waking-up from Sleep or BOR is enabled.

Work around

Method 1: In applications where BOR use is not critical, turn off the BOR in the Configuration Word.

Method 2: Set the FVREN bit of the FVRCON register. Maintain this bit on at all times.

Method 3: When BOR module is needed only during run-time, use the software-enabled BOR by setting the SBODEN option on the Configuration Word. BOR should be turned off by software before Sleep, then follow the below sequence for turning BOR on after wake-up:

a. Wake-up event occurs;
b. Turn on FVR (FVREN bit of the FVRCON register);
c. Wait until FVR_RDY bit is set;
d. Wait 15 µs after the FVR Ready bit is set;
e. Manually turn on the BOR.

Method 4: Use the software-enabled BOR as described in Method 3, but use the following sequence:

a. Switch to internal 32 kHz oscillator immediately before Sleep;
b. Upon wake-up, turn on FVR (FVREN bit of the FVRCON register);
c. Manually turn on the BOR;
d. Switch the clock back to the preferred clock source.

Note: When using the software BOR follow the steps in Methods 3 or 4 above when enabling BOR for the first time during program execution.

<table>
<thead>
<tr>
<th>Affected Silicon Revisions</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
</tr>
<tr>
<td>X</td>
</tr>
</tbody>
</table>
8. Module: Enhanced Universal
Synchronous Asynchronous
Receiver (EUSART)

8.1 16-Bit High-Speed Asynchronous Mode

The EUSART provides unexpected operation when the 16-Bit High-Speed Asynchronous mode is selected and the Baud Rate Generator Data register values are loaded with zero (0). We do not recommend using this configuration for EUSART communication. The configuration is shown below in the following table:

<table>
<thead>
<tr>
<th>Configuration Bits</th>
<th>BRG Data Registers</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYNC</td>
<td>BRG16</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

**Work around**

Ensure that the SPBRGH or the SPBRGL register is loaded with a non-zero value.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
8.2 Auto-Baud Detect

When using automatic baud detection (ABDEN), on occasion, an incorrect count value can be stored at the end of auto-baud detection in the SPBRGH:SPBRGL (SPBRG) registers. The SPBRG value may be off by several counts. This condition happens sporadically when the device clock frequency drifts to a frequency where the SPBRG value oscillates between two different values. The issue is present regardless of the baud rate Configuration bit settings.

Work around

When using auto-baud, it is a good practice to always verify the obtained value of SPBRG, to ensure it remains within the application specifications. Two recommended methods are shown below.

For additional auto-baud information, see Technical Brief TB3069, “Use of Auto-Baud for Reception of LIN Serial Communications Devices: Mid-Range and Enhanced Mid-Range”.

EXAMPLE 2: METHOD 1 – EUSART AUTO-BAUD DETECT WORK AROUND

In firmware, define default, minimum and maximum auto-baud (SPBRG) values according to the application requirements.

For example, if the application runs at 9600 baud at 16 MHz then, the default SPBRG value would be (assuming 16-bit/Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a +/-5% tolerance is required, so tolerance is 0x67 * 5% = 0x05.

```
#define SPBRG_16BIT *((int *)&SPBRG; // define location for 16-bit SPBRG value

const int DEFAULT_BAUD = 0x0067; // Default Auto-Baud value
const int TOL = 0x05; // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL; // Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL; // Maximum Auto-Baud Limit

ABDEN = 1; // Start Auto-Baud
while (ABDEN); // Wait until Auto-Baud completes

if((SPBRG_16BIT > MAX_BAUD)|| (SPBRG_16BIT < MIN_BAUD))
{
        SPBRG_16BIT = DEFAULT_BAUD; // if out of spec, use DEFAULT_BAUD
}
// if in spec, continue using the
// Auto-Baud value in SPBRG
```
EXAMPLE 3: METHOD 2 – EUSART AUTO-BAUD DETECT WORK AROUND

Similar to Method 1, define default, minimum and maximum auto-baud (SPBRG) values. In firmware, compute a running average of SPBRG. If the new SPBRG value falls outside the minimum or maximum limits, then use the current running average value (Average_Baud), otherwise use the auto-baud SPBRG value and calculate a new running average.

For example, if the application runs at 9600 baud at 16 MHz then, the default SPBRG value would be (assuming 16-bit/Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a +/-5% tolerance is required, so tolerance is 0x67 * 5% = 0x05.

```c
#define SPBRG_16BIT   (*((int *)&SPBRG); // define location for 16-bit SPBRG value
const int DEFAULT_BAUD = 0x0067;  // Default Auto-Baud value
const int TOL = 0x05;               // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL;  // Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL;  // Maximum Auto-Baud Limit

int Average_Baud; // Define Average_Baud variable
int Integrator; // Define Integrator variable

Average_Baud = DEFAULT_BAUD; // Set initial average Baud rate
Integrator = DEFAULT_BAUD*15; // The running 16 count average

ABDEN = 1; // Start Auto-Baud
while (ABDEN); // Wait until Auto-Baud completes

Integrator+ = SPBRG_16BIT;
Average_Baud = Integrator/16;
if((SPBRG_16BIT > MAX_BAUD)||(SPBRG_16BIT < MIN_BAUD))
{    // Check if value is within limits
    SPBRG_16BIT = Average_Baud; // If out of spec, use previous average
}
else // If in spec, calculate the running
{    // average but continue using the
    Integrator+ = SPBRG_16BIT;
    Average_Baud = Integrator/16;
    Integrator- = Average_Baud;
}

```

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
9. Module: PFM Self-Writes

9.1 PFM

Writes to the PFM will not execute if the device’s clock source is HS, ECH, or the Internal Oscillator is at either 8 MHz or 16 MHz. The DFM is unaffected.

Work around

To write to the PFM, the clock source must be one of the following settings: Internal Oscillator set to 4 MHz or lower, ECM, ECL, XT, External RC, LP or T1OSC.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>

10. Module: MSSP (Master Synchronous Serial Port)

10.1 SPI Master mode

When the MSSP is used in SPI Master mode and the CKE bit is clear (CKE = 0), the Buffer Full (BF) bit and the MSSP Interrupt Flag (SSPIF) bit becomes set half an SCK cycle early. If the user software immediately reacts to either of the bits being set, a write collision may occur as indicated by the WCOL bit being set.

Work around

To avoid a write collision one of the following methods should be used:

Method 1: Add a software delay of one SCK period after detecting the completed transfer (the BF bit or SSPIF bit becomes set) and prior to writing to the SSPBUF register. Verify the WCOL bit is clear after writing to SSPBUF. If the WCOL bit is set, clear the bit in software and rewrite the SSPBUF register.

Method 2: As part of the MSSP initialization procedure, set the CKE bit (CKE = 1).

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>A1</th>
<th>A3</th>
<th>A4</th>
<th>A5</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001419E):

<table>
<thead>
<tr>
<th>Note:</th>
<th>Corrections are shown in bold. Where possible, the original bold text formatting has been removed for clarity.</th>
</tr>
</thead>
<tbody>
<tr>
<td>None.</td>
<td></td>
</tr>
</tbody>
</table>
APPENDIX A: DOCUMENT
REVISION HISTORY

Rev A Document (06/2010)
Initial release of this document.

Rev B Document (07/2010)
Revised Module 1.1; Added Module 6.1; Other minor corrections.

Updated errata to new format; Added Revision A3; Added Module 7.

Added Module 8, BOR.

Rev E Document (02/2012)
Updated Table 1; Added Modules 2.2, 2.3 and 2.4; Added Module 9, EUSART; Other minor corrections. Data Sheet Clarifications: Added Module 1, Oscillator.

Rev F Document (04/2012)
Added Silicon Revision A4.

Rev G Document (08/2012)
Added Module 9.1

Rev H Document (12/2012)
Removed Module 5.1 ADC (Error Parameters). Added Silicon Revision A5.

Rev J Document (01/2014)
Added Module 3.3; Other minor corrections.

Rev K Document (12/2014)
Added Module 10, MSSP; Other minor corrections.
Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip’s code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MicroCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks
The Microchip name and logo, the Microchip logo, dsPIC, FlashFlex, flexPWR, JukeBlox, KEELOQ, KEELOQ logo, Kleer, LANCheck, MediaLB, MOST, MOST logo, MPLAB, OptoLyzer, PIC, PICSTART, PIC32 logo, RightTouch, SpyNIC, SST, SST Logo, SuperFlash and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

The Embedded Control Solutions Company and mTouch are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, BodyCom, chipKIT, chipKIT logo, CodeGuard, dsPICDEM, dsPICDEM.net, ECAN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, KleerNet, KleerNet logo, MiWi, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscent Code Generation, PICDEM, PICDEM.net, PICkit, PICtail, RightTouch logo, REAL ICE, SQI, Serial Quad I/O, Total Endurance, TSHARC, USBCheck, VanSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2010-2014, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV
ISO/TS 16949

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company’s quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip’s quality system for the design and manufacture of development systems is ISO 9001:2000 certified.
## Worldwide Sales and Service

**AMERICAS**  
Corporate Office  
2355 West Chandler Blvd.  
Chandler, AZ 85224-6199  
Tel: 480-792-7200  
Fax: 480-792-7277  
Technical Support:  
http://www.microchip.com/support  
Web Address:  
www.microchip.com

**Atlanta**  
Duluth, GA  
Tel: 678-957-9614  
Fax: 678-957-1455

**Austin, TX**  
Tel: 512-257-3370

**Boston**  
Westborough, MA  
Tel: 508-367-6200  
Fax: 508-367-6202

**Chicago**  
Itasca, IL  
Tel: 630-285-0087  
Fax: 630-285-0088

**Cleveland**  
Independence, OH  
Tel: 216-447-0464  
Fax: 216-447-0643

**Dallas**  
Addison, TX  
Tel: 972-818-7423  
Fax: 972-818-2924

**Detroit**  
Novi, MI  
Tel: 248-848-4000

**Houston, TX**  
Tel: 281-894-5983

**Indianapolis**  
Noblesville, IN  
Tel: 317-773-8323  
Fax: 317-773-5453

**Los Angeles**  
Mission Viejo, CA  
Tel: 949-462-9523  
Fax: 949-462-9608

**New York, NY**  
Tel: 631-435-6000

**San Jose, CA**  
Tel: 408-735-9110

**Canada - Toronto**  
Tel: 905-673-0699  
Fax: 905-673-6509

**ASIA/PACIFIC**  
Asia Pacific Office  
Suites 3707-14, 37th Floor  
Tower 6, The Gateway  
Harbour City, Kowloon  
Hong Kong  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**Australia - Sydney**  
Tel: 61-2-9668-6733  
Fax: 61-2-9668-6755

**China - Beijing**  
Tel: 86-10-8569-7000  
Fax: 86-10-8528-2104

**China - Chengdu**  
Tel: 86-28-8665-5511  
Fax: 86-28-8665-7889

**China - Chongqing**  
Tel: 86-23-8980-9588

**China - Hangzhou**  
Tel: 86-571-8792-8115  
Fax: 86-571-8792-8116

**China - Hong Kong SAR**  
Tel: 852-2943-5100  
Fax: 852-2401-3431

**China - Nanjing**  
Tel: 86-25-8792-8116

**China - Shanghai**  
Tel: 86-21-5407-5533  
Fax: 86-21-5407-5066

**China - Shenyang**  
Tel: 86-24-2334-2829  
Fax: 86-24-2334-2393

**China - Shenzhen**  
Tel: 86-755-8664-2200  
Fax: 86-755-8203-1760

**China - Wuhan**  
Tel: 86-27-5980-5300  
Fax: 86-27-5980-5118

**China - Xian**  
Tel: 86-29-8833-7252  
Fax: 86-29-8833-7256

**China - Xiamen**  
Tel: 86-592-2388138  
Fax: 86-592-2388130

**China - Zhuhai**  
Tel: 86-756-3210040  
Fax: 86-756-3210049

**ASIA/PACIFIC**  
India - Bangalore  
Tel: 91-80-3090-4444  
Fax: 91-80-3090-4123

**India - New Delhi**  
Tel: 91-11-4160-8631  
Fax: 91-11-4160-8632

**India - Pune**  
Tel: 91-20-3019-1500

**Japan - Osaka**  
Tel: 81-6-6152-7160  
Fax: 81-6-6152-9310

**Japan - Tokyo**  
Tel: 81-3-6880-3770  
Fax: 81-3-6880-3771

**Korea - Daegu**  
Tel: 82-53-744-4301  
Fax: 82-53-744-4302

**Korea - Seoul**  
Tel: 82-2-554-7200  
Fax: 82-2-558-5932 or 82-2-558-5934

**Malaysia - Kuala Lumpur**  
Tel: 60-3-6201-9857  
Fax: 60-3-6201-9859

**Malaysia - Penang**  
Tel: 60-4-227-8870  
Fax: 60-4-227-4068

**Philippines - Manila**  
Tel: 63-2-634-9065  
Fax: 63-2-634-9069

**Singapore**  
Tel: 65-6334-8870  
Fax: 65-6334-8850

**Taiwan - Hsin Chu**  
Tel: 886-3-5778-366  
Fax: 886-3-5770-955

**Taiwan - Kaohsiung**  
Tel: 886-7-213-7830

**Taiwan - Taipei**  
Tel: 886-2-2508-6800  
Fax: 886-2-2508-0102

**Thailand - Bangkok**  
Tel: 66-2-694-1351  
Fax: 66-2-694-1350

**EUROPE**  
Austria - Wels  
Tel: 43-7242-2244-39  
Fax: 43-7242-2244-393

**Denmark - Copenhagen**  
Tel: 45-4450-2828  
Fax: 45-4485-2829

**France - Paris**  
Tel: 33-1-69-53-63-20  
Fax: 33-1-69-30-90-79

**Germany - Dusseldorf**  
Tel: 49-2129-3766400

**Germany - Munich**  
Tel: 49-89-627-144-0  
Fax: 49-89-627-144-44

**Germany - Pforzheim**  
Tel: 49-7231-424750

**Italy - Milan**  
Tel: 39-0331-742611  
Fax: 39-0331-466781

**Italy - Venice**  
Tel: 39-049-7625286

**Netherlands - Drunen**  
Tel: 31-416-690399  
Fax: 31-416-690340

**Poland - Warsaw**  
Tel: 48-22-3325737

**Spain - Madrid**  
Tel: 34-91-708-08-90  
Fax: 34-91-708-08-91

**Sweden - Stockholm**  
Tel: 46-8-5090-4654

**UK - Wokingham**  
Tel: 44-118-921-5800  
Fax: 44-118-921-5820

03/25/14