The PIC18F26K20/46K20 family devices that you have received conform functionally to the current Device Data Sheet (DS41303H), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F26K20/46K20 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (B6).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip’s programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:
1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select Programmer > Reconnect.
   b) For MPLAB X IDE, select Window > Dashboard and click the Refresh Debug Tool Status icon ( ).
5. Depending on the development tool used, the part number and Device Revision ID value appear in the Output window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F26K20/46K20 silicon revisions are shown in Table 1.

### TABLE 1: SILICON DEVREV VALUES

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Device ID(1) (11-bit)</th>
<th>Revision ID for Silicon Revision(2) (5-bit)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>B2</td>
</tr>
<tr>
<td>PIC18F26K20</td>
<td>100h</td>
<td>0x09</td>
</tr>
<tr>
<td>PIC18F46K20</td>
<td>101h</td>
<td>0x09</td>
</tr>
</tbody>
</table>

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID:DEVREV”.

2: Refer to the “PIC18F2XXK20/4XXK20 Flash Programming Specification” (DS41297) for detailed information on Device and Revision IDs for your specific device.
# TABLE 2: SILICON ISSUE SUMMARY

<table>
<thead>
<tr>
<th>Module</th>
<th>Feature</th>
<th>Item Number</th>
<th>Issue Summary</th>
<th>Affected Revisions(1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECCP</td>
<td>Full-Bridge</td>
<td>1.</td>
<td>Dead-band time is 4/Fosc instead of 1/Fosc.</td>
<td>X X X X X</td>
</tr>
<tr>
<td>ECCP</td>
<td>Full-Bridge</td>
<td>2.</td>
<td>Compromised dead band.</td>
<td>X X X X X</td>
</tr>
<tr>
<td>MSSP SPI</td>
<td>SPI Clock</td>
<td>3.</td>
<td>Improper start in Timer2/2 Clock mode.</td>
<td>X X X X X</td>
</tr>
<tr>
<td>MSSP SPI</td>
<td>SPI Master</td>
<td>4.</td>
<td>Improper sampling of last bit.</td>
<td>X X X X X</td>
</tr>
<tr>
<td>MSSP (Master I²C Mode)</td>
<td>I²C Master</td>
<td>5.</td>
<td>Improper handling of Stop event.</td>
<td>X X X X X</td>
</tr>
<tr>
<td>EUSART</td>
<td>OERR Flag</td>
<td>6.</td>
<td>Clearing SPEN bit does not clear OERR flag.</td>
<td>X X X X X</td>
</tr>
<tr>
<td>EUSART</td>
<td>BAUDCON</td>
<td>7.</td>
<td>RCIDL may improperly stay low.</td>
<td>X X X X X</td>
</tr>
<tr>
<td>System Clocks</td>
<td>HFINTOSC</td>
<td>8.</td>
<td>Frequency instability.</td>
<td>X</td>
</tr>
<tr>
<td>Data EEPROM Memory</td>
<td>Endurance</td>
<td>9.</td>
<td>Endurance limited to 10K cycles.</td>
<td>X X X X X</td>
</tr>
<tr>
<td>Program Flash Memory</td>
<td>Endurance</td>
<td>10.</td>
<td>Endurance limited to 1K cycles.</td>
<td>X X X X X</td>
</tr>
<tr>
<td>PORTB Interrupt-on-Change</td>
<td>Interrupt-on-change</td>
<td>11.</td>
<td>False interrupt when setting interrupt enable.</td>
<td>X X X X X</td>
</tr>
<tr>
<td>ADC</td>
<td>ADC Conversion</td>
<td>12.</td>
<td>ADC conversion may be limited to half scale.</td>
<td>X X</td>
</tr>
<tr>
<td>Interrupt-on-Change</td>
<td>Interrupt-on-change interrupt when in Sleep</td>
<td>13.</td>
<td>False interrupt when waking from Sleep.</td>
<td>X X X X X</td>
</tr>
<tr>
<td>Capture/Compare/PWM</td>
<td>Capture mode</td>
<td>14.</td>
<td>Weak pull-up disabled in Capture mode on CCP2</td>
<td>X X X X X</td>
</tr>
<tr>
<td>Low-Voltage Detect</td>
<td>LVD in Sleep</td>
<td>15.</td>
<td>LVD erroneously triggers upon wake-up from Sleep if band gap is disabled in Sleep mode.</td>
<td>X X X X X</td>
</tr>
<tr>
<td>Resets (BOR)</td>
<td>Brown-out Reset</td>
<td>16.</td>
<td>An unexpected Reset may occur if the Brown-out Reset module (BOR) is disabled, and then re-enabled.</td>
<td>X X X X X</td>
</tr>
<tr>
<td>Wake-up from Low-Power Sleep mode</td>
<td>Wake-up sources</td>
<td>17.</td>
<td>Device may not wake-up under specific conditions.</td>
<td>X X X X X</td>
</tr>
</tbody>
</table>

**Note 1:** Only those issues indicated in the last column apply to the current silicon revision.
Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (B6).

1. Module: ECCP

Changing direction in Full-Bridge mode inserts a dead-band time of \(4/\text{Fosc} \times \text{TMR2 prescale}\) instead of \(1/\text{Fosc} \times \text{TMR2 prescale}\) as specified in the data sheet.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

2. Module: ECCP

ECCP – In Full-Bridge mode when \(\text{PR2} = \text{CCPR1L}\) and \(\text{DC1B[1:0]} \neq '00'\) and the direction is changed, then the dead time before the modulated output starts is compromised. The modulated signal improperly starts immediately with the direction change and stays on for \(\text{Tosc} \times \text{TMR2Prescale} \times \text{DC1B[1:0]}\).

Work around
Avoid changing direction when the duty cycle is within three Least Significant steps of 100% duty cycle. Instead, clear the \(\text{DC1B[1:0]}\) bits before the direction change and then set them to the desired value after the direction change is complete.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

3. Module: MSSP SPI

When the SPI clock is configured for Timer2/2 (SSPCON1<3:0> = 0011) and the CKE bit of the SSPSTAT register is ‘1’, then the first SDO data bit and SCK non-idle edge occur simultaneously. Also, the first SCK non-Idle level may be short.

Work around
Use clock mode other than Timer2/2.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

4. Module: MSSP SPI

In SPI Master mode, when the CKE bit of the SSPSTAT register is cleared and the SMP bit of the SSPSTAT register is set, then the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

Work around
None.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

5. Module: MSSP (Master \(^2\text{C Mode})

In Master \(^2\text{C Receive mode, if a Stop condition occurs in the middle of an address or data reception, then the SCL clock stream will continue endlessly and the RCEN bit of the SSPCON2 register will remain set improperly. When a Start condition occurs after the improper Stop condition, then nine additional clocks will be generated followed by the RCEN bit going low.

Work around
Use low-impedance pull-ups on the SDA line to reduce the possibility of noise glitches, which may trigger an improper Stop event. Use a time-out event timer to detect the unexpected Stop condition and resulting stuck RCEN bit. Clear stuck RCEN bit by clearing SSPEN bit of SSPCON1.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
6. Module: EUSART

The OERR flag of the RCSTA register is reset only by clearing the CREN bit of the RCSTA register or by a device Reset. Clearing the SPEN bit of the RCSTA register does not clear the OERR flag.

**Work around**

Clear the OERR flag by clearing the CREN bit instead of clearing the SPEN bit.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
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<td>X</td>
</tr>
</tbody>
</table>

7. Module: EUSART

In Asynchronous Receive mode when the RX input goes low after an Idle period and stays low for less than 1/16th bit period, then that event will be correctly detected as an invalid Start bit. If the RX input goes low a second time, less than one full bit time after the leading edge of the first invalid Start time, then the low transition of the RCIDL Status bit will be improperly delayed by one full bit time following that second edge. If the second pulse is also an invalid Start bit then the RCIDL will remain low indefinitely until either a valid Start bit occurs or the EUSART is reset.

**Work around**

When monitoring the RCIDL bit, measure the length of time between the RCIDL going low and the RCIF flag going high. If this time is greater than one character time, then restore the RCIDL bit by resetting the EUSART receiver. The EUSART receiver is reset when either the SPEN bit or CREN bit of the RCSTA register is cleared.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

8. Module: System Clocks

HFINTOSC output frequency may have up to 1% short term frequency instability beyond the maximum and minimum limits shown in the data sheet.

**Work around**

Use the HS, XT or EC clock modes.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

9. Module: Data EEPROM Memory

The write/erase endurance of data EEPROM memory is limited to 10K cycles.

**Work around**

Use the error correction method that stores data in multiple locations.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

10. Module: Program Flash Memory

The write/erase endurance of the PFM is limited to 1K cycles when VDD is above 3V. Endurance degrades when VDD is below 3V.

**Work around**

For data tables in Program Flash Memory use the error correction method that stores data in multiple locations.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

11. Module: PORTB Interrupt-on-Change

Setting a PORTB interrupt-on-change enable bit of the IOCB register while the corresponding PORTB input is high will cause an RBIF interrupt.

**Work around**

Set the IOCB bits to the desired configuration then read PORTB to clear the mismatch latches. Finally, clear the RBIF bit before setting the RBIE bit.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
12. Module: ADC

After extended stress the Most Significant bit (MSb) of the ADC conversion result can become stuck at ‘0’. Conversions resulting in code 511 or less are still accurate, but conversions that should result in codes greater than 511 are instead pinned at 511.

The potential for failures is a function of several factors:

- The potential for failures increases over the life of the part. No failures have ever been seen for accelerated stress estimated to be equivalent to 34 years at room temperature. The failure rate after accelerated stress estimated to be equivalent to 146 years at room temperature can be as high as 10% for VDD = 1.8V. The time to failure will decrease as the operating temperature increases.

- The potential for failures is highest at low VDD and decreases as VDD increases.

**Work around**

1. Restrict the input voltage to less than 1/2 of the ADC voltage reference so that the expected result is always a code less than or equal to 511.

2. Use manual acquisition time (ACQT<2:0> = 000) and put the part to Sleep after each conversion.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

13. Module: Interrupt-on-Change

When any interrupt-on-change is enabled and the corresponding input is high, then waking from Sleep by a source other than interrupt-on-change may cause the RBIF interrupt flag bit to become set improperly.

**Work around**

1. Use the INTx interrupts in lieu of interrupt-on-change.

Or

2. Store the state of the PORTB inputs before entering Sleep. Upon waking, if an RBIF is detected, then compare the PORTB levels with those stored. If they are the same, then clear and ignore the RBIF interrupt.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

14. Module: Capture/Compare/PWM

14.1 CCP2

The weak pull-up (if enabled) on the selected CCP2 pin will be disabled when CCP2 is set up for Capture mode.

**Work around**

Use an external resistor as the pull-up.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

15. Module: Low-Voltage Detect

If Low-Voltage Detect is enabled, the band gap is disabled in Sleep, and the part is put to Sleep for a short period of time, the LVD will trigger immediately upon waking-up from Sleep.

**Work around**

Do not disable the band gap in Sleep when using the LVD.

**Affected Silicon Revisions**

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
16. Module: Resets (BOR)

An unexpected Reset may occur if the Brown-out Reset module (BOR) is disabled, and then re-enabled when the Fixed Voltage Reference is not enabled (CVRCON2<7> = 0). This issue affects BOR modes: BOREN<1:0> = 10 and BOREN<1:0> = 01. In both of these modes, if the BOR module is re-enabled while the device is active, unexpected Resets may be generated.

Work around

If BOR is required, and power consumption is not an issue, use BOREN<1:0> = 11. For BOREN<1:0> = 10 mode, either switch to BOREN<1:0> = 11 mode or enable the FVR (CVRCON2<7> = 1) and verify that the FVR is stable (CVRCON2<6> = 1) prior to entering Sleep. If power consumption is an issue and low power is desired, do not use BOREN<1:0> = 10 mode. Instead, use BOREN<1:0> = 01 and follow the steps below when entering and exiting Sleep.

1. Disable BOR by clearing SBOREN(RCON<6> = 0) and the FVR (CVRCON2<7> = 0).
2. Enter Sleep mode (if desired). Sleep();
3. After exiting Sleep mode (if entered) enable the FVR (CVRCON2<7> = 1).
4. Wait for the Fixed Voltage Reference to stabilize (typically 25 us).
   while(!CVRCON2bits.FVRST);
5. Re-enable BOR by setting SBOREN (RCON<6> = 1).

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

17. Module: Wake-up from Low-Power Sleep mode

The device may not wake from Sleep when both of the following conditions are met:

1. The device is in Sleep mode for < 1 ms;
2. On waking, the device executes a SLEEP instruction within 100 μs.

Under these conditions, the oscillator may stop before completing execution of the SLEEP instruction. The device will enter Sleep mode but will not wake-up on any enabled wake-up event, including the Watchdog Timer.

Work around

1. Disable High-Speed Start-up
   Disabling High-Speed Start-up in the Configuration Word will delay the device executing code on wake-up by 250 μs, nominally, allowing the oscillator to stabilize.

   The wake-up time from Sleep will increase by about 250 μs, nominally.

2. BOR Enabled during Sleep
   Configuring the device for hardware only BOR or software-controlled BOR and enabling SBOREN, the voltage reference is on during Sleep. The device will wake-up and the oscillator will be stable. This will add 20 μA (nominal) to the Sleep current.

3. Enable the FVR during Sleep
   In the same manner as the BOR, the FVR will keep the voltage reference on during Sleep, causing the oscillator to be stable on wake-up.

4. Avoid executing SLEEP within 100 μs of any wake-up event
   This can be achieved by adding more instructions (NOP) before executing the SLEEP instruction. This minimizes the probability of the SLEEP instruction only partially executing.

Affected Silicon Revisions

<table>
<thead>
<tr>
<th>B2</th>
<th>B3</th>
<th>B5</th>
<th>B6</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41303H):

**Note:** Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. **Module: Product Identification System**

   The temperature range values have been corrected.

**PRODUCT IDENTIFICATION SYSTEM**

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>X</th>
<th>XX</th>
<th>XXX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>Tape and Reel</td>
<td>Temperature Range</td>
<td>Package</td>
</tr>
<tr>
<td>PIC18F26K20; PIC18F46K20; DSTEMP; PIC18F26K20; DSTEMP; PIC16F887; PIC18F45K20; PIC18F46K20.</td>
<td>Blank = Standard packaging (tube or tray)</td>
<td>T = Tape and Reel(1)</td>
<td>PT = TQFP (Thin Quad Flatpack)</td>
</tr>
<tr>
<td>Blank = Standard packaging (tube or tray)</td>
<td>T = Tape and Reel(1)</td>
<td>PT = TQFP (Thin Quad Flatpack)</td>
<td>QTP, SOTP, Code or Special Requirements (blank otherwise)</td>
</tr>
</tbody>
</table>

**Examples:**

a) PIC18F45K20 - E/P 301 = Industrial temp., PDIP package, QTP pattern #301.
b) PIC18F26K20 - I/SO = Industrial temp., SOIC package.
c) PIC16F887 - E/P = Extended temp., PDIP package.
d) PIC18F46K20 - I/PT = Industrial temp., TQFP package, tape and reel.

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.
APPENDIX A: DOCUMENT REVISION HISTORY

**Rev A Document (9/2008)**
Initial release of this document.

Updated Errata to new format.
Added Module 5, MSSP Master I^{2}C Mode; Added Module 6, EUSART; Added Module 12, ADC.
Clarifications/Corrections to the Data Sheet:
Removed Modules 1-3.

Revised Table 1: Silicon DEVREV Values.
Clarifications/Corrections to the Data Sheet: Added Module 1: Electrical Specifications; Added Module 2: Electrical Specifications; Added Module 3 MSSP: Register 17-3 SSPADD; Added Module 4 MSSP: Section 17.4.2 Operation; Added Module 5 MSSP: Figure 17-16 MSSP Block Diagram; Added Module 6 MSSP: Sections 17.4.7.1, 17.4.8, 17.4.9, 17.4.17.1, 17.4.17.2, 17.4.17.3: SSPADD, changing <6:0> to <7:0>.

Silicon Errata Issues: Added Module 13; Updated Table 2.
Data Sheet Clarifications:
Removed Modules 1-6.

Removed ADC Work around #2 and changed #3 to #2 (Module 12).

**Rev F Document (2/2012)**
Updated errata to new format; Added Module 14, Capture/Compare/PWM.

Added MPLAB X IDE; Added Silicon Revision B6.

Added Module 15, Low-Voltage Detect and Module 16, Reset (BOR).
Data Sheet Clarifications: Added Module 1, Electrical Characteristics.

**Rev J Document (9/2015)**
Data Sheet Clarifications:
Removed Module 1, Electrical Specifications. Added Module 1, Product Identification System.

Added Module 17. Wake-up from Low-Power Sleep Mode to the Silicon Errata Issues section. Other minor corrections.
Note the following details of the code protection feature on Microchip devices:

• Microchip products meet the specification contained in their particular Microchip Data Sheet.

• Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

• There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

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