MRF89XA
Data Sheet
Ultra Low-Power, Integrated ISM Band
Sub-GHz Transceiver
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Features
- Fully integrated ultra low-power, sub-GHz transceiver
- Wide band - Half-duplex transceiver
- Supports proprietary sub-GHz wireless protocols
- Simple, 4-wire SPI-compatible interface
- CMOS/TTL-compatible I/Os
- On-chip oscillator circuit
- Dedicated clock output
- Supports power-saving modes
- Operating voltage: 2.1V-3.6V
- Low-Current Consumption, Typically:
  - 3 mA in RX mode
  - 25 mA @ +10 dBm in TX mode
  - 0.1 μA (Typical) and 2 μA (Maximum) in Sleep mode
- Supports Industrial Temperature
- Small, 32-pin TQFN package; complies with ETSI EN 300 220 and FCC part 15

RF/Analog Features
- Supports ISM band sub-GHz frequency ranges: 863-870, 902-928 and 950-960 MHz
- Modulation technique: Supports FSK and OOK
- Supports high data rates: Up to 200 kbps, NRZ coding
- Reception sensitivity: Down to -107 dBm at 25 kb/s in FSK, -113 dBm at 2 kb/s in OOK
- RF output power: +12.5 dBm programmable in eight steps
- Wide Received Signal Strength Indicator (RSSI), dynamic range: 70 dB from RX noise floor
- Signal-ended RF input/output
- On-chip frequency synthesizer
- Supports PLL loop filter with lock detect
- Integrated Power Amplifier (PA) and Low Noise Amplifiers (LNA)
- Channel filters
- On-chip IF gain and mixers
- Integrated low phase noise VCO

Baseband Features
- Packet handling feature with data whitening and automatic CRC generation
- Incoming sync word (pattern) recognition
- Built-in bit synchronizer for incoming data, and clock synchronization and recovery
- 64-byte Transmit/Receive FIFO with preload in Standby mode
- Supports Manchester Encoding/Decoding Techniques

Typical Applications
- Home/industrial/building automation
- Remote wireless control
- Wireless PC peripherals
- Remote keyless entry
- Wireless sensor networks
- Vehicle sensor monitoring
- Telemetry
- Data logging systems
- Wireless alarm
- Remote automatic meter reading
- Security systems for home/industrial environments
- Automobile immobilizers
- Sports and performance monitoring
- Wireless toy controls
- Medical applications

General Description
The MRF89XA is a single chip FSK/OOK transceiver capable of operating in the 863-870 MHz and 902-928 MHz license-free ISM frequency bands, as well as the 950-960 MHz frequency band. The low-cost MRF89XA is optimized for very low-power consumption (3 mA in Receiver mode). It incorporates a baseband modem with data rates up to 200 kb/s. Data handling features include a 64-byte FIFO, packet handling, automatic CRC generation and data whitening. Its highly integrated architecture allows for minimum external component count while still maintaining design flexibility. All major RF communication parameters are programmable and most of them may be dynamically set. It complies with European (ETSI EN 300-220 V2.1.1) and North American (FCC Part 15.247 and 15.249) regulatory standards.
Pin Diagram

The following diagram shows the top view pin arrangement of the 32-pin QFN package.

FIGURE 1: MRF89XA 32-PIN QFN PIN DIAGRAM

Note 1: Pin 33 (GND) is located on the underside of the IC package.
2: It is recommended to connect Pin 32 NC to GND.
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1.0 OVERVIEW

Microchip Technology's MRF89XA is a fully integrated, half-duplex, sub-GHz transceiver. This low-power, single chip RF FSK and OOK baseband transceiver supports:

- Super Heterodyne Architecture
- Multi-Channel, Multi-Band Synthesizer with Phase Lock Loop (PLL) for easy RF Design
- Power Amplifier (PA)
- Low Noise Amplifier (LNA)
- I/Q Two Stage Down Converter Mixers
- I/Q Demodulator, FSK/OOK
- Baseband Filters and Amplifiers

The simplified functional block diagram of MRF89XA is shown in Figure 1-1.

The MRF89XA is a good choice for low-cost, high-volume, low data rate (<256 kbps), two-way short range wireless applications. This is a single chip FSK and OOK transceiver capable of operation in the 863-870 MHz and 902-928 MHz license-free ISM frequency bands, as well as the 950-960 MHz frequency band.

The low-cost MRF89XA is optimized for very low-power consumption (3 mA in Receiver mode). It incorporates a baseband modem with data rates up to 200 kb/s in FSK and 32 kb/s in OOK. Data handling features include a 64-byte FIFO, packet handling, automatic CRC generation and data whitening. The device also supports Manchester coding techniques. Its highly integrated architecture allows for minimum external component count while still maintaining design flexibility. All major RF communication parameters are programmable and most of them may be dynamically set.

The MRF89XA complies with European (ETSI EN 300-220 V2.1.1) and North American (FCC Part 15.247 and 15.249) regulatory standards, and therefore, can be used for all applications looking for FCC, IC, or ETSI certification in the ISM band and licensed bands also.

The MRF89XA supports a stable sensitivity and linearity characteristics for a wide supply range and is internally regulated. The frequency synthesizer of the MRF89XA is a fully integrated integer-N type PLL. The PLL circuit requires only five external components for the PLL loop filter and the VCO tank circuit. The PLL and low phase noise provides for excellent adjacent channel rejection capability, Bit Error Rate (BER) and larger communication coverage along with higher output power.

The crystal oscillator provided on the MRF89XA device provides the reference clock for the PLL. In order to minimize the total system cost, a communication link in most of the applications can be created using a low-cost, generic 12.8 MHz crystal, a bypass filter and an affordable microcontroller. The MRF89XA provides a clock signal for the microcontroller and avoids the need for a second crystal on the circuit board. The transceiver can be interfaced with many popular Microchip PIC® microcontrollers via a 4-wire SPI, interrupt (IRO), PLL lock and clock out. The interface between the microcontroller and MRF89XA is shown in Figure 1-1.

The MRF89XA supports the following digital data processing features:

- PLL and I/Q VCO Configuration
- Receiver Signal Strength Indicator
- Sync Word Recognition
- Packet Handler
- Interrupt and Flags
- Different Operating Modes (Continuous, Buffer and Packet)
- Data Filtering/Whitening/Encoding
- Baseband Power Amplifier
- TX/RX Data Buffer

The role is to interface the data to/from the modulator/demodulator and the microcontroller access points (SPI, IRQ and DATA pins). It also controls all the Configuration registers. The receiver's Baseband Bandwidth (BBBW) can be programmed to accommodate various deviations and data rates requirements.

The high-resolution PLL allows:

- The usage of multiple channels in any of the bands
- The rapid settling time allows for faster frequency hopping, bypassing multi-path fading and interference to achieve robust wireless links

An optional Bit Synchronizer (BitSync) is provided, to supply a synchronous clock and data stream to a companion microcontroller in Continuous mode, or to fill the FIFO with glitch-free data in Buffered mode. The transceiver is integrated with different power-saving modes and an internal wake-up time to keep track of the activities, which reduces the overall current consumption and extends the battery life. The small size and low-power consumption of the MRF89XA makes it ideal for various short range radio applications.
FIGURE 1-1: MRF89XA SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

- Antenna
- Saw Filter
- Matching Circuitry Block
- Loop Filter Block
- Tank Circuit Block
- RF Block
- PARS
- RFIO
- RF Parts
- Baseband Amplifier/Filter/Limiter
- Data Processing Unit
- Power Management
- Memory
- Control Interface
- Crystal Frequency = 12.8 MHz

MRF89XA

PIC® MCU
- CSDATA
- CSION
- SDI
- SDO
- SCK
- IRO0
- IR01
- DATA
- PLOCK
- CLKOUT
- OSC1
- I/O
- I/O
- SDO
- SDI
- SCK
- INT0
- INT1
- I/O
- I/O
- I/O

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2.0 HARDWARE DESCRIPTION

The MRF89XA is an integrated, single chip, low-power ISM band sub-GHz transceiver. A simplified architectural block diagram of the MRF89XA is shown in Figure 2-1. The frequency synthesizer is clocked by an external 12.8 crystal, and frequency ranges from 863-870 MHz, 902-928 MHz and 950-960 MHz.

The MRF89XA receiver employs a super-heterodyne architecture. Here, the first IF is 1/9th of the RF frequency (approximately 100 MHz). The second down conversion down converts the I and Q signals to baseband in the case of the FSK receiver (Zero IF) and to a low-IF (IF2) for the OOK receiver. After the second down-conversion stage, the received signal is channel select filtered and amplified to a level adequate for demodulation. Both FSK and OOK demodulation are available. Image rejection is achieved by the SAW filter.

The baseband I and Q signals at the transmitter side are digitally generated by a DDS whose Digital-to-Analog Converters (DAC) followed by two anti-aliasing low-pass filters transform the digital signal into analog In-Phase (I) and Quadrature (Q) components whose frequency is the selected Frequency Deviation (Fdev). The transmitter supports both FSK and OOK modes of operation. The transmitter has a typical output power of +12.5 dBm. An internal transmit/receive switch combines the transmitter and receiver circuits into a single-ended RFIO pin. This pin is connected to the impedance matching circuitry (Balun) and to the external antenna with power amplifier pin, if required. The device operates in the low-voltage range of 2.1V to 3.6V, and in Sleep mode, it operates at a very low-current state, typically 0.1 µA.

The quality of the data is validated using the RSSI and bit synchronizer blocks built into the transceiver. Data is buffered in 64-byte transmitter registers and receiver FIFOs. The frequency synthesizer allows the use of a low-accuracy, low-cost crystal. CLKOUT can be used to clock the external controller. The transceiver is controlled via a 4-wire Serial Peripheral Interface (SPI), interrupt (IRO0 and IRO1), PLOCK, DATA and Chip Select pins for SPI.

The MRF89XA supports the following feature blocks:
- Data Filtering and Whitening
- Bit Synchronization
- 64-Byte Transmit and Receive FIFO Buffer
- General Configuration Registers

These features reduce the processing load, which allows the use of simple, low-cost 8-bit microcontrollers for data processing.
FIGURE 2-1: MRF89XA BLOCK DIAGRAM

- Reception Block
  - LNA
  - First Stage Mixers
  - IF Gain
  - Second Stage Mixers
- Transmission Block
  - PA
  - Second Stage Mixers
  - First Stage Mixers
  - Modulation (DDS, DACs, Interpolation Filters)
  - PLL Block (Comparator, VCO, Filter, Dividers)
- Frequency Synthesis Block
  - Supply Block
  - Crystal
  - Loop Filter
- Reception Block
  - RSSI
  - Digital Demodulator
  - Control Interface
  - Supply
- Transmission Block
  - LO1 TX
  - LO2 TX
  - Phase Shift to Frequency Shift Conversion (FSK mode)
- PLL Block
  - LO1 TX
  - LO1 RX
  - LO2 TX
  - LO2 RX
- Supply Block
  - Supply
  - Crystal
  - Loop Filter
- Control Interface
  - SPI
  - DATA
  - CLKOUT
  - PLOCK
## TABLE 2-1: PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TEST5</td>
<td>Digital I/O</td>
<td>Test Pin. Connect to Ground.</td>
</tr>
<tr>
<td>2</td>
<td>TEST1</td>
<td>Digital I/O</td>
<td>Test Pin. Connect to Ground.</td>
</tr>
<tr>
<td>3</td>
<td>VCORS</td>
<td>Analog Output</td>
<td>Regulated voltage supply of the VCO.</td>
</tr>
<tr>
<td>4</td>
<td>VCOTM</td>
<td>Analog I/O</td>
<td>VCO tank.</td>
</tr>
<tr>
<td>5</td>
<td>VCOTP</td>
<td>Analog I/O</td>
<td>VCO tank.</td>
</tr>
<tr>
<td>6</td>
<td>PLLM</td>
<td>Analog I/O</td>
<td>PLL loop filter.</td>
</tr>
<tr>
<td>7</td>
<td>PLLP</td>
<td>Analog I/O</td>
<td>PLL loop filter.</td>
</tr>
<tr>
<td>8</td>
<td>TEST6</td>
<td>Digital I/O</td>
<td>Test Pin. Connect to Ground.</td>
</tr>
<tr>
<td>9</td>
<td>TEST7</td>
<td>Digital I/O</td>
<td>Test Pin. Connect to Ground.</td>
</tr>
<tr>
<td>10</td>
<td>OSC1</td>
<td>Analog Input</td>
<td>Crystal connection.</td>
</tr>
<tr>
<td>11</td>
<td>OSC2</td>
<td>Analog Input</td>
<td>Crystal connection.</td>
</tr>
<tr>
<td>12</td>
<td>TEST0</td>
<td>Digital Input</td>
<td>Test Pin. Connect to Ground.</td>
</tr>
<tr>
<td>13</td>
<td>TEST8</td>
<td>Digital I/O</td>
<td>Test Pin. Used for POR (allow pin to float; do not connect signal).</td>
</tr>
<tr>
<td>14</td>
<td>CSCON</td>
<td>Digital Input</td>
<td>SPI Configure Chip Select.</td>
</tr>
<tr>
<td>15</td>
<td>CSDATA</td>
<td>Digital Input</td>
<td>SPI Data Chip Select.</td>
</tr>
<tr>
<td>16</td>
<td>SDO</td>
<td>Digital Output</td>
<td>Serial data output interface from MRF89XA.</td>
</tr>
<tr>
<td>17</td>
<td>SDI</td>
<td>Digital Input</td>
<td>Serial data input interface to MRF89XA.</td>
</tr>
<tr>
<td>18</td>
<td>SCK</td>
<td>Digital Input</td>
<td>Serial clock interface.</td>
</tr>
<tr>
<td>19</td>
<td>CLKOUT</td>
<td>Digital Output</td>
<td>Clock output.</td>
</tr>
<tr>
<td>20</td>
<td>DATA</td>
<td>Digital I/O</td>
<td>NRZ data input and output (Continuous mode).</td>
</tr>
<tr>
<td>21</td>
<td>IRQ0</td>
<td>Digital Output</td>
<td>Interrupt request output (‘0’).</td>
</tr>
<tr>
<td>22</td>
<td>IRQ1</td>
<td>Digital Output</td>
<td>Interrupt request output (‘1’).</td>
</tr>
<tr>
<td>23</td>
<td>PLOCK</td>
<td>Digital Output</td>
<td>PLL lock detection output.</td>
</tr>
<tr>
<td>24</td>
<td>TEST2</td>
<td>Digital I/O</td>
<td>Test Pin. Connect to Ground.</td>
</tr>
<tr>
<td>25</td>
<td>TEST3</td>
<td>Digital I/O</td>
<td>Test Pin. Connect to Ground.</td>
</tr>
<tr>
<td>26</td>
<td>VDD</td>
<td>Power</td>
<td>Supply voltage.</td>
</tr>
<tr>
<td>27</td>
<td>AVRS</td>
<td>Analog Output</td>
<td>Regulated supply of the analog circuitry.</td>
</tr>
<tr>
<td>28</td>
<td>DVRS</td>
<td>Analog Output</td>
<td>Regulated supply of the digital circuitry.</td>
</tr>
<tr>
<td>29</td>
<td>PARS</td>
<td>Analog Output</td>
<td>Regulated supply of the PA.</td>
</tr>
<tr>
<td>30</td>
<td>TEST4</td>
<td>Digital I/O</td>
<td>Connect to GND.</td>
</tr>
<tr>
<td>31</td>
<td>RFIO</td>
<td>Analog I/O</td>
<td>RF input/output.</td>
</tr>
<tr>
<td>32</td>
<td>NC</td>
<td>—</td>
<td>No Connection. Connect to Ground.</td>
</tr>
<tr>
<td>33</td>
<td>Vss</td>
<td>Ground</td>
<td>Exposed Pad. Connect to Ground.</td>
</tr>
</tbody>
</table>
2.1 Memory Map for MRF89XA Configuration/Control/Status Registers

The memory in the MRF89XA transceiver is implemented as static RAM and is accessible via the SPI port. Each memory location functionally addresses the command, control, status or data/FIFO fields as shown in Table 2-2 and Table 2-3. The control registers provide control, status and configuration information. The device address for the transceiver is done by indexing the base address in the RAM memory. The registers operate fundamentally on parameters common to transmit and receive modes, Interrupt registers, receiver parameters, Sync pattern, transmitter parameters, crystal oscillator parameters and packet handler parameters. The FIFO serves as a temporary buffer for data transmission and reception.

TABLE 2-2: CONFIGURATION/CONTROL/STATUS REGISTER DESCRIPTION

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>0</td>
<td>GCONREG</td>
<td>General Configuration Register</td>
<td>Transceiver mode, frequency band selection, VCO trimming, PLL frequency dividers selection</td>
</tr>
<tr>
<td>2.</td>
<td>1</td>
<td>DMODREG</td>
<td>Data and Modulation Configuration Register</td>
<td>Modulation type, Data mode, OOK threshold type, IF gain</td>
</tr>
<tr>
<td>3.</td>
<td>2</td>
<td>FDEVREG</td>
<td>Frequency Deviation Control Register</td>
<td>Frequency deviation in FSK Transmit mode</td>
</tr>
<tr>
<td>4.</td>
<td>3</td>
<td>BRSEFREG</td>
<td>Bit Rate Set Register</td>
<td>Operational bit rate</td>
</tr>
<tr>
<td>5.</td>
<td>4</td>
<td>FLTHREG</td>
<td>Floor Threshold Control Register</td>
<td>Floor threshold in OOK Receive mode</td>
</tr>
<tr>
<td>6.</td>
<td>5</td>
<td>FIFOEREG</td>
<td>FIFO Configuration Register</td>
<td>FIFO size and threshold</td>
</tr>
<tr>
<td>7.</td>
<td>6</td>
<td>R1CNRSTREG</td>
<td>R1 Counter Set Register</td>
<td>Value input for R1 counter</td>
</tr>
<tr>
<td>8.</td>
<td>7</td>
<td>P1CNRSTREG</td>
<td>P1 Counter Set Register</td>
<td>Value input for P1 counter</td>
</tr>
<tr>
<td>9.</td>
<td>8</td>
<td>S1CNRSTREG</td>
<td>S1 Counter Set Register</td>
<td>Value input for S1 counter</td>
</tr>
<tr>
<td>10.</td>
<td>9</td>
<td>R2CNRSTREG</td>
<td>R2 Counter Set Register</td>
<td>Value input for R2 counter</td>
</tr>
<tr>
<td>11.</td>
<td>10</td>
<td>P2CNRSTREG</td>
<td>P2 Counter Set Register</td>
<td>Value input for P2 counter</td>
</tr>
<tr>
<td>12.</td>
<td>11</td>
<td>S2CNRSTREG</td>
<td>S2 Counter Set Register</td>
<td>Value input for S2 counter</td>
</tr>
<tr>
<td>13.</td>
<td>12</td>
<td>PACONREG</td>
<td>Power Amplifier Control Register</td>
<td>PA regulator output voltage</td>
</tr>
</tbody>
</table>

Interrupt Parameters Configuration Registers: Size – 3 Bytes, Start Address – 13

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>14.</td>
<td>13</td>
<td>FTPRXIREG</td>
<td>FIFO, Transmit and Receive Interrupt Request Configuration Register</td>
<td>Interrupt request (‘0’ and ‘1’) in Receive mode, interrupt request (‘1’) in Transmit mode, interrupt request for FIFO full, empty and overrun</td>
</tr>
<tr>
<td>15.</td>
<td>14</td>
<td>FTPRIREG</td>
<td>FIFO Transmit PLL and RSSI Interrupt Configuration Register</td>
<td>FIFO fill method, FIFO fill, interrupt request for TX start and end, interrupt request for RSSI, PLL lock enable and status</td>
</tr>
<tr>
<td>16.</td>
<td>15</td>
<td>RSTHIREG</td>
<td>RSSI Threshold Interrupt Request Configuration Register</td>
<td>RSSI threshold for interrupt</td>
</tr>
</tbody>
</table>
### Receiver Parameters Configuration Registers: Size – 6 Bytes, Start Address – 16

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>17.</td>
<td>16</td>
<td>FILCONREG</td>
<td>Filter Configuration Register</td>
<td>Passive filter bandwidth selection, sets the receiver bandwidth (Butterworth filter),</td>
</tr>
<tr>
<td>18.</td>
<td>17</td>
<td>PFCONREG</td>
<td>Polyphase Filter Configuration Register</td>
<td>Selects the central frequency of the polyphase filter</td>
</tr>
<tr>
<td>19.</td>
<td>18</td>
<td>SYNCREG</td>
<td>Sync Control Register</td>
<td>Enables polyphase filter (in OOK receive mode, bit synchronizer control, Sync word recognition, Sync word size, Sync word error</td>
</tr>
<tr>
<td>20.</td>
<td>19</td>
<td>RESVREG</td>
<td>Reserved Register</td>
<td>Reserved for future use</td>
</tr>
<tr>
<td>21.</td>
<td>20</td>
<td>RSTSREG</td>
<td>RSSI Status Read Register</td>
<td>RSSI output</td>
</tr>
<tr>
<td>22.</td>
<td>21</td>
<td>OOKCREG</td>
<td>OOK Configuration Register</td>
<td>RSSI threshold size in OOK demodulator, RSSI threshold period in OOK demodulator, cut-off frequency of the OOK threshold in demodulator</td>
</tr>
</tbody>
</table>

### Sync Word Parameters Configuration Registers: Size – 4 Bytes, Start Address – 22

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>23.</td>
<td>22</td>
<td>SYNCV31REG</td>
<td>Sync Value 1&lt;sup&gt;st&lt;/sup&gt; Byte Configuration Register</td>
<td>Configuring 1&lt;sup&gt;st&lt;/sup&gt; byte of the 32-bit Sync word</td>
</tr>
<tr>
<td>24.</td>
<td>23</td>
<td>SYNCV23REG</td>
<td>Sync Value 2&lt;sup&gt;nd&lt;/sup&gt; Byte Configuration Register</td>
<td>Configuring 2&lt;sup&gt;nd&lt;/sup&gt; byte of the 32-bit Sync word</td>
</tr>
<tr>
<td>25.</td>
<td>24</td>
<td>SYNCV15REG</td>
<td>Sync Value 3&lt;sup&gt;rd&lt;/sup&gt; Byte Configuration Register</td>
<td>Configuring 3&lt;sup&gt;rd&lt;/sup&gt; byte of the 32-bit Sync word</td>
</tr>
<tr>
<td>26.</td>
<td>25</td>
<td>SYNCV07REG</td>
<td>Sync Value 4&lt;sup&gt;th&lt;/sup&gt; Byte Configuration Register</td>
<td>Configuring 4&lt;sup&gt;th&lt;/sup&gt; byte of the 32-bit Sync word</td>
</tr>
</tbody>
</table>

### Transmitter Parameters Configuration Registers: Size – 1 Byte, Start Address – 26

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>27.</td>
<td>26</td>
<td>TXPARCREG</td>
<td>Transmit Parameters Configuration Register</td>
<td>Transmit interpolation cut-off frequency, power output</td>
</tr>
</tbody>
</table>

### Oscillator Parameters Configuration Registers: Size – 1 Byte, Start Address – 27

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>28.</td>
<td>27</td>
<td>CLKOUTREG</td>
<td>Clock Output Control Register</td>
<td>Clock-out control, frequency</td>
</tr>
</tbody>
</table>
### TABLE 2-2: CONFIGURATION/CONTROL/STATUS REGISTER DESCRIPTION (CONTINUED)

Packet Handling Parameters Configuration Registers: Size – 4 Bytes, Start Address – 28

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>29.</td>
<td>28</td>
<td>PLOADREG</td>
<td>Payload Configuration Register</td>
<td>Enable Manchester encoding/decoding, payload length</td>
</tr>
<tr>
<td>30.</td>
<td>29</td>
<td>NADDSREG</td>
<td>Node Address Set Register</td>
<td>Node's local address for filtering of received packets</td>
</tr>
<tr>
<td>31.</td>
<td>30</td>
<td>PKTCREG</td>
<td>Packet Configuration Register</td>
<td>Packet format, size of the preamble, whitening, CRC on/off, address filtering of received packets, CRC status</td>
</tr>
<tr>
<td>32.</td>
<td>31</td>
<td>FCRCREG</td>
<td>FIFO CRC Configuration Register</td>
<td>FIFO auto-clear (if CRC failed), FIFO access</td>
</tr>
<tr>
<td>Register Function/Parameter Type</td>
<td>Register Address</td>
<td>Register Name</td>
<td>Bit 7</td>
<td>Bit 6</td>
</tr>
<tr>
<td>---------------------------------</td>
<td>------------------</td>
<td>-------------------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>General</td>
<td>0</td>
<td>GCONREG</td>
<td>CMOD2</td>
<td>CMOD1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>DMODREG</td>
<td>MODSEL1</td>
<td>MODSEL0</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>FDEVREG</td>
<td>FDVAL7</td>
<td>FDVAL6</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>BRSREG</td>
<td>Reserved</td>
<td>BRVAL6</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>FLTHREG</td>
<td>FTOVAL7</td>
<td>FTOVAL6</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>FIFOCREG</td>
<td>FSIZE1</td>
<td>FSIZE0</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>R1CNTSREG</td>
<td>R1CVAL7</td>
<td>R1CVAL6</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>P1CNTSREG</td>
<td>P1CVAL7</td>
<td>P1CVAL6</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>S1CNTSREG</td>
<td>S1CVAL7</td>
<td>S1CVAL6</td>
</tr>
<tr>
<td></td>
<td>9</td>
<td>R2CNTSREG</td>
<td>R2CVAL7</td>
<td>R2CVAL6</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>P2CNTSREG</td>
<td>P2CVAL7</td>
<td>P2CVAL6</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>S2CNTSREG</td>
<td>S2CVAL7</td>
<td>S2CVAL6</td>
</tr>
<tr>
<td></td>
<td>12</td>
<td>PACONREG</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>13</td>
<td>FTXRXIREG</td>
<td>IRQ0RXS1</td>
<td>IRQ0RXS0</td>
</tr>
<tr>
<td></td>
<td>14</td>
<td>FTPRIREG</td>
<td>FIFOF</td>
<td>FIFOF</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td>RSTHIREG</td>
<td>RTIVAL7</td>
<td>RTIVAL6</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td>FILCONREG</td>
<td>PASFILV3</td>
<td>PASFILV2</td>
</tr>
<tr>
<td></td>
<td>17</td>
<td>PFCONREG</td>
<td>PLOCDFV3</td>
<td>PLOCDFV2</td>
</tr>
<tr>
<td></td>
<td>18</td>
<td>SYNCREG</td>
<td>POLFILVEN</td>
<td>BSYNCEN</td>
</tr>
<tr>
<td></td>
<td>19</td>
<td>RESVREG</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>RSTSREG</td>
<td>RSSIVAL7</td>
<td>RSSIVAL6</td>
</tr>
<tr>
<td></td>
<td>21</td>
<td>OOKCREG</td>
<td>OOKTHSV5</td>
<td>OOKTHSV4</td>
</tr>
<tr>
<td></td>
<td>22</td>
<td>SYNVX31REG</td>
<td>SYNCB1V7</td>
<td>SYNCB1V6</td>
</tr>
<tr>
<td></td>
<td>23</td>
<td>SYNVX23REG</td>
<td>SYNCB2V7</td>
<td>SYNCB2V6</td>
</tr>
<tr>
<td></td>
<td>24</td>
<td>SYNVX15REG</td>
<td>SYNCB3V7</td>
<td>SYNCB3V6</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>SYNVX07REG</td>
<td>SYNCB4V7</td>
<td>SYNCB4V6</td>
</tr>
<tr>
<td></td>
<td>26</td>
<td>TXPARCREG</td>
<td>TXIPOLFV3</td>
<td>TXIPOLFV2</td>
</tr>
<tr>
<td></td>
<td>27</td>
<td>CLKOUGTFREG</td>
<td>CLCKCNTNL</td>
<td>CLKOFREQ5</td>
</tr>
<tr>
<td></td>
<td>28</td>
<td>PLOADREG</td>
<td>MCHSTREN</td>
<td>PLDPLEN6</td>
</tr>
<tr>
<td></td>
<td>29</td>
<td>NANDDERG</td>
<td>NLADDR7</td>
<td>NLADDR6</td>
</tr>
<tr>
<td></td>
<td>30</td>
<td>PKTCREG</td>
<td>PKTLENF</td>
<td>PRESIZE1</td>
</tr>
<tr>
<td></td>
<td>31</td>
<td>FCRCREG</td>
<td>ACFCRC</td>
<td>FRWAXS</td>
</tr>
</tbody>
</table>
3.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

- Ambient temperature under bias: -40°C to +85°C
- Storage temperature: -55°C to +125°C
- Lead temperature (soldering, max 10s): +260°C
- Voltage on VDD with respect to VSS: -0.3V to 6V
- Voltage on any combined digital and analog pin with respect to VSS (except RFIO and VDD): -0.3V to (VDD + 0.3V)
- Voltage on open-collector outputs (RFIO)(†): -0.3V to 3.7V
- Input current into pin (except VDD and VSS): -25 mA to 25 mA
- Electrostatic discharge with human body model: 1000V

Note 1: At maximum, voltage on RFIO cannot be higher than 6V.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
3.1 ESD Notice

The MRF89XA is a high-performance radio frequency device. It satisfies:

- Class II of the JEDEC standard JESD22-A114-B (Human Body Model) of 2 KV, except on all of the RF pins where it satisfies Class 1A.
- Class III of the JEDEC standard JESD22-C101C (Charged Device Model) on all pins.

It should thus be handled with all the necessary ESD precautions to avoid any permanent damage.

### TABLE 3-1: RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient Operating Temperature</td>
<td>-40</td>
<td>—</td>
<td>+85</td>
<td>°C</td>
<td>—</td>
</tr>
<tr>
<td>Supply Voltage for RF, Analog and Digital Circuits</td>
<td>2.1</td>
<td>—</td>
<td>3.6</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>Supply Voltage for Digital I/O</td>
<td>2.1</td>
<td>—</td>
<td>3.6</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>Input High Voltage (VIH)</td>
<td>0.5 * VDD</td>
<td>—</td>
<td>VDD + 0.3</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>Input Low Voltage (VIL)</td>
<td>-0.3V</td>
<td>—</td>
<td>0.2 * VDD</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>DC Voltage on Open Collector Outputs (RFIO)¹(²)</td>
<td>VDD – 1.5</td>
<td>—</td>
<td>VDD + 1.5</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>AC Peak Voltage on Open Collector Outputs (IO)¹(²)</td>
<td>VDD – 1.5</td>
<td>—</td>
<td>VDD + 1.5</td>
<td>V</td>
<td>—</td>
</tr>
</tbody>
</table>

**Note 1:** At minimum, VDD – 1.5V should not be lower than 1.8V.

**Note 2:** At maximum, VDD + 1.5V should not be higher than 3.7V.

### TABLE 3-2: CURRENT CONSUMPTION³

<table>
<thead>
<tr>
<th>Chip Mode</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sleep</td>
<td>—</td>
<td>0.1</td>
<td>2</td>
<td>µA</td>
<td>Sleep clock disabled, all blocks disabled</td>
</tr>
<tr>
<td>Idle</td>
<td>—</td>
<td>65</td>
<td>80</td>
<td>µA</td>
<td>Oscillator and baseband enabled²(²)</td>
</tr>
<tr>
<td>Frequency Synth</td>
<td>—</td>
<td>1.3</td>
<td>1.7</td>
<td>mA</td>
<td>Frequency synthesizer running</td>
</tr>
<tr>
<td>TX</td>
<td>—</td>
<td>25</td>
<td>30</td>
<td>mA</td>
<td>Output power = +10 dBm</td>
</tr>
<tr>
<td>TX</td>
<td>—</td>
<td>16</td>
<td>21</td>
<td>mA</td>
<td>Output power = +1 dBm¹(²)</td>
</tr>
<tr>
<td>RX</td>
<td>—</td>
<td>3.0</td>
<td>3.5</td>
<td>mA</td>
<td>—</td>
</tr>
</tbody>
</table>

**Note 1:** Guaranteed by design and characterization.

**Note 2:** Crystal CLOAD = 10 pF, C0 = 2.5 pF, RM = 15 Ohms.

**Note 3:** Measurement Conditions: Temp = 25°C, VDD = 3.3V, crystal frequency = 12.8 MHz, carrier frequency = 869 or 915 MHz, modulation FSK, data rate = 25 kb/s, FDEV = 50 kHz, fc = 100 kHz, unless otherwise specified.
### TABLE 3-3: DIGITAL I/O PIN INPUT SPECIFICATIONS\(^{(1)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>—</td>
<td>—</td>
<td>0.2 * VDD</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>0.8 * VDD</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Low Leakage Current(^{(2)})</td>
<td>-0.5</td>
<td>—</td>
<td>0.5</td>
<td>µA</td>
<td>VIH = 0V</td>
</tr>
<tr>
<td>IIH</td>
<td>Input High Leakage Current</td>
<td>-0.5</td>
<td>—</td>
<td>0.5</td>
<td>µA</td>
<td>VIH = VDD, VDD = 3.7</td>
</tr>
<tr>
<td>VOL</td>
<td>Digital Low Output Voltage</td>
<td>—</td>
<td>—</td>
<td>0.1 * VDD</td>
<td>—</td>
<td>IOL = 1 mA</td>
</tr>
<tr>
<td>VOH</td>
<td>Digital Low Output</td>
<td>0.9 * VDD</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>IOH = -1 mA</td>
</tr>
</tbody>
</table>

**Note 1:** Measurement Conditions: TA = 25°C, VDD = 3.3V, crystal frequency = 12.8 MHz, unless otherwise specified.

**Note 2:** Negative current is defined as the current sourced by the pin.

**Note 3:** On Pin 10 (OSC1) and 11 (OSC2), maximum voltages of 1.8V can be applied.

### TABLE 3-4: PLL PARAMETERS AC CHARACTERISTICS\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Ranges</td>
<td>863</td>
<td>—</td>
<td>870</td>
<td>MHz</td>
<td>Programmable but requires specific BOM</td>
</tr>
<tr>
<td></td>
<td>902</td>
<td>—</td>
<td>928</td>
<td>MHz</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>950</td>
<td>—</td>
<td>960</td>
<td>MHz</td>
<td>—</td>
</tr>
<tr>
<td>Bit Rate (FSK)</td>
<td>1.56</td>
<td>—</td>
<td>200</td>
<td>kb/s</td>
<td>NRZ</td>
</tr>
<tr>
<td>Bit Rate (OOK)</td>
<td>1.56</td>
<td>—</td>
<td>32</td>
<td>kb/s</td>
<td>NRZ</td>
</tr>
<tr>
<td>Frequency Deviation (FSK)</td>
<td>33</td>
<td>50</td>
<td>200</td>
<td>kHz</td>
<td>—</td>
</tr>
<tr>
<td>Crystal Oscillator Frequency</td>
<td>9</td>
<td>12.8</td>
<td>15</td>
<td>MHz</td>
<td>—</td>
</tr>
<tr>
<td>Frequency Synthesizer Step</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>kHz</td>
<td>Variable, depending on the frequency</td>
</tr>
<tr>
<td>Oscillator Wake-up Time</td>
<td>—</td>
<td>1.5</td>
<td>5</td>
<td>ms</td>
<td>From Sleep mode(^{(1)})</td>
</tr>
<tr>
<td>Frequency Synthesizer Wake-up Time; at most, 10 kHz away from the Target</td>
<td>—</td>
<td>500</td>
<td>800</td>
<td>µs</td>
<td>From Stand-by mode</td>
</tr>
<tr>
<td>Frequency Synthesizer Hop Time; at most, 10 kHz away from the Target</td>
<td>—</td>
<td>180</td>
<td>—</td>
<td>µs</td>
<td>200 kHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>200</td>
<td>—</td>
<td>µs</td>
<td>1 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>250</td>
<td>—</td>
<td>µs</td>
<td>5 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>260</td>
<td>—</td>
<td>µs</td>
<td>7 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>290</td>
<td>—</td>
<td>µs</td>
<td>12 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>320</td>
<td>—</td>
<td>µs</td>
<td>20 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>340</td>
<td>—</td>
<td>µs</td>
<td>27 MHz step</td>
</tr>
</tbody>
</table>

**Note 1:** Guaranteed by design and characterization
TABLE 3-5: RECEIVER AC CHARACTERISTICS (1)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity (FSK)</td>
<td></td>
<td>-107</td>
<td></td>
<td>dBm</td>
<td>869 MHz, BR = 25 kb/s, Fdev = 50 kHz, fc = 100 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-103</td>
<td></td>
<td>dBm</td>
<td>869 MHz, BR = 66.7 kb/s, Fdev = 100 kHz, fc = 200 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-105</td>
<td></td>
<td>dBm</td>
<td>915 MHz, BR = 25 kb/s, Fdev = 50 kHz, fc = 100 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-101</td>
<td></td>
<td>dBm</td>
<td>915 MHz, BR = 66.7 kb/s, Fdev = 100 kHz, fc = 200 kHz</td>
</tr>
<tr>
<td>Sensitivity (OOK)</td>
<td></td>
<td>-113</td>
<td></td>
<td>dBm</td>
<td>869 MHz, 2kb/s NRZ, fc – fo = 50 kHz, fo = 50 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-106</td>
<td></td>
<td>dBm</td>
<td>869 MHz, 16.7 kb/s NRZ, fc – fo = 100 kHz, fo = 100 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-111</td>
<td></td>
<td>dBm</td>
<td>915 MHz, 2 kb/s NRZ, fc – fo = 50 kHz, fo = 50 kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-105</td>
<td></td>
<td>dBm</td>
<td>915 MHz, 16.7 kb/s NRZ, fc – fo = 100 kHz, fo = 100 kHz</td>
</tr>
<tr>
<td>Co-Channel Rejection</td>
<td></td>
<td>-12</td>
<td></td>
<td>dBc</td>
<td>Modulation as wanted signal</td>
</tr>
<tr>
<td>Adjacent Channel Rejection</td>
<td></td>
<td>27</td>
<td></td>
<td>dB</td>
<td>Offset = 300 kHz, unwanted tone is not modulated</td>
</tr>
<tr>
<td></td>
<td></td>
<td>52</td>
<td></td>
<td>dB</td>
<td>Offset = 600 kHz, unwanted tone is not modulated</td>
</tr>
<tr>
<td></td>
<td></td>
<td>57</td>
<td></td>
<td>dB</td>
<td>Offset = 1.2 MHz, unwanted tone is not modulated</td>
</tr>
<tr>
<td>Blocking Immunity</td>
<td></td>
<td>-48</td>
<td></td>
<td>dBm</td>
<td>Offset = 1 MHz, unmodulated</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-37</td>
<td></td>
<td>dBm</td>
<td>Offset = 2 MHz, unmodulated, no SAW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-33</td>
<td></td>
<td>dBm</td>
<td>Offset = 10 MHz, unmodulated, no SAW</td>
</tr>
<tr>
<td>Receiver Bandwidth in FSK Mode (2)</td>
<td>50</td>
<td></td>
<td>250</td>
<td>kHz</td>
<td>Single side BW, Polyphase Off</td>
</tr>
<tr>
<td>Receiver Bandwidth in OOK Mode (2)</td>
<td>50</td>
<td></td>
<td>400</td>
<td>kHz</td>
<td>Single side BW, Polyphase On</td>
</tr>
<tr>
<td>Input Third Order Intercept Point</td>
<td></td>
<td>-28</td>
<td></td>
<td>dBm</td>
<td>Interferers at 1 MHz and 1.950 MHz offset</td>
</tr>
<tr>
<td>Receiver Wake-up Time</td>
<td></td>
<td>280</td>
<td>500</td>
<td>µs</td>
<td>From FS to RX ready</td>
</tr>
<tr>
<td>Receiver Wake-up Time</td>
<td></td>
<td>600</td>
<td>900</td>
<td>µs</td>
<td>From Stand-by to RX ready</td>
</tr>
<tr>
<td>Receiver Hop Time from RX Ready</td>
<td></td>
<td>400</td>
<td></td>
<td>µs</td>
<td>200 kHz step</td>
</tr>
<tr>
<td>Ready to RX Ready with a Frequency</td>
<td></td>
<td>400</td>
<td></td>
<td>µs</td>
<td>1 MHz step</td>
</tr>
<tr>
<td>Hop Time</td>
<td></td>
<td>460</td>
<td></td>
<td>µs</td>
<td>5 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>480</td>
<td></td>
<td>µs</td>
<td>7 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>520</td>
<td></td>
<td>µs</td>
<td>12 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>550</td>
<td></td>
<td>µs</td>
<td>20 MHz step</td>
</tr>
<tr>
<td>RSSI Sampling Time</td>
<td></td>
<td></td>
<td>1/Fdev</td>
<td>s</td>
<td>From RX ready</td>
</tr>
<tr>
<td>RSSI Dynamic Range</td>
<td></td>
<td>70</td>
<td></td>
<td>dB</td>
<td>Ranging from sensitivity</td>
</tr>
</tbody>
</table>

**Note 1:** Guaranteed by design and characterization.

**Note 2:** This reflects the whole receiver bandwidth, as described by conditions for active and passive filters.
### TABLE 3-6: TRANSMITTER AC CHARACTERISTICS\(^{(1)}\)

<table>
<thead>
<tr>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Output Power, Programmable with 8 Steps of typ. 3 dB</td>
<td></td>
<td>+12.5</td>
<td></td>
<td>dBm</td>
<td>Maximum power setting.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-8.5</td>
<td></td>
<td>dBm</td>
<td>Minimum power setting.</td>
</tr>
<tr>
<td>Phase Noise</td>
<td></td>
<td>-112</td>
<td></td>
<td>dBc/Hz</td>
<td>Measured with a 600 kHz offset at the transmitter output.</td>
</tr>
<tr>
<td>Transmitted Spurious</td>
<td></td>
<td></td>
<td>-47</td>
<td>dBc</td>
<td>At any offset between 200 kHz and 600 kHz, unmodulated carrier, Fdev = 50 kHz.</td>
</tr>
<tr>
<td>Transmitter Wake-up Time</td>
<td></td>
<td>120</td>
<td>500</td>
<td>µs</td>
<td>From FS to TX ready.</td>
</tr>
<tr>
<td>Transmitter Wake-up Time</td>
<td></td>
<td>600</td>
<td>900</td>
<td>µs</td>
<td>From standby to TX ready.</td>
</tr>
</tbody>
</table>

**Note 1:** Guaranteed by design and characterization.

### 3.2 Timing Specification and Diagram

### TABLE 3-7: SPI TIMING SPECIFICATION\(^{(1,2,3)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPI Configure Clock Frequency</td>
<td></td>
<td></td>
<td>6</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>SPI Data Clock Frequency</td>
<td></td>
<td></td>
<td>1</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>Data Hold and Setup Time</td>
<td>2</td>
<td></td>
<td></td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>SDI Setup Time for SPI Configure</td>
<td>250</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SDI Setup Time for SPI Data</td>
<td>312</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CSCON Low to SCK Rising Edge; SCK Falling Edge to /CSCON High</td>
<td>500</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CSADATA Low to SCK Rising Edge; SCK Falling Edge to /CSADATA High</td>
<td>625</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CSCON Rising to Falling Edge</td>
<td>500</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>CSDATA Rising to Falling Edge</td>
<td>625</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Typical Values: TA = 25°C, VDD = 3.3V, crystal frequency = 12.8 MHz, unless otherwise specified.

2: Negative current is defined as the current sourced by the pin.

3: On Pin 10 (OSC1) and 11 (OSC2), maximum voltages of 1.8V can be applied.
APPENDIX A: REVISION HISTORY

Revision A (January 2010)

This is the initial released version of this document.
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________________________________________________________________________

2. How does this document meet your hardware and software development needs?

________________________________________________________________________

3. Do you find the organization of this document easy to follow? If not, why?

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________________________________________________________________________

5. What deletions from the document could be made without affecting the overall usefulness?

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6. Is there any incorrect or misleading information (what and where)?

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7. How would you improve this document?

________________________________________________________________________

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>X</th>
<th>/XX</th>
<th>XXX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature Range</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pattern</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Example:
- a) MRF89XA-I/MQ: Industrial temperature, QFN package.
- b) MRF89XAT-I/MQ: Industrial temperature, QFN package, tape and reel.

Device: MRF89XA: Ultra Low-Power, Integrated ISM Band Sub-GHz Transceiver

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Package: MQ = QFN (Quad Flat, No Lead)
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