MRF89XA
Data Sheet

Ultra Low-Power, Integrated ISM Band
Sub-GHz Transceiver
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Ultra Low-Power, Integrated ISM Band Sub-GHz Transceiver

Features

- Fully integrated ultra low-power, sub-GHz transceiver
- Wide-band half-duplex transceiver
- Supports proprietary sub-GHz wireless protocols
- Simple 4-wire SPI-compatible interface
- CMOS/TTL-compatible I/Os
- On-chip oscillator circuit
- Dedicated clock output
- Supports power-saving modes
- Operating voltage: 2.1-3.6V
- Low-current consumption, typically:
  - 3 mA in RX mode
  - 25 mA @ +10 dBm in TX mode
  - 0.1 μA (Typical) and 2 μA (Maximum) in Sleep mode
- Supports Industrial temperature range (-40ºC to +85ºC)
- Complies with ETSI EN 300-220 and FCC part 15
- Small, 32-pin TQFN package

RF/Analog Features

- Supports ISM band sub-GHz frequency ranges: 863–870, 902–928 and 950–960 MHz
- Modulation technique: Supports FSK and OOK
- Supports high data rates: Up to 200 kbps, NRZ coding
- Reception sensitivity: Down to -107 dBm at 25 kbps in FSK, -113 dBm at 2 kbps in OOK
- RF output power: +12.5 dBm programmable in eight steps
- Wide Received Signal Strength Indicator (RSSI), dynamic range: 70 dB from RX noise floor
- Signal-ended RF input/output
- On-chip frequency synthesizer
- Supports PLL loop filter with lock detect
- Integrated Power Amplifier (PA) and Low Noise Amplifiers (LNA)
- Channel filters
- On-chip IF gain and mixers
- Integrated low-phase noise VCO

Baseband Features

- Packet handling feature with data whitening and automatic CRC generation
- Incoming sync word (pattern) recognition
- Built-in bit synchronizer for incoming data, and clock synchronization and recovery
- 64-byte transmit/receive FIFO with preload in Stand-by mode
- Supports Manchester encoding/decoding techniques

Typical Applications

- Home/industrial/building automation
- Remote wireless control
- Wireless PC peripherals
- Remote keyless entry
- Wireless sensor networks
- Vehicle sensor monitoring
- Telemetry
- Data logging systems
- Wireless alarm
- Remote automatic meter reading
- Security systems for home/industrial environments
- Automobile immobilizers
- Sports and performance monitoring
- Wireless toy controls
- Medical applications

General Description

The MRF89XA is a single chip, multi-channel FSK/OOK transceiver capable of operating in the 863-870 MHz and 902-928 MHz license-free ISM frequency bands, as well as the 950-960 MHz frequency band. The low-cost MRF89XA is optimized for very low-power consumption. It incorporates a baseband modem with data rates up to 200 kbps. Data handling features include a 64-byte FIFO, packet handling, automatic CRC generation and data whitening.

Its highly integrated architecture allows for minimum external component count while still maintaining design flexibility.
All critical RF and baseband functions are integrated in the MRF89XA, which minimizes the external component count and reducing design time. The RF communication parameters are made programmable and most of them may be dynamically set. A microcontroller, RF SAW filter, 12.8 MHz crystal and a few passive components are required to create a complete, reliable radio function. The MRF89XA uses several low-power mechanisms to reduce overall current consumption and extend battery life. Its small size and low-power consumption makes the MRF89XA ideal for a wide variety of short range radio applications. The MRF89XA complies with European (ETSI EN 300-220) and United States (FCC Part 15.247 and 15.249) regulatory standards.

**FIGURE 1: MRF89XA 32-PIN QFN PIN DIAGRAM**

32-Pin QFN

MRF89XA

**Note 1:** Pin 33 (GND) is located on the underside of the IC package.

**Note 2:** It is recommended to connect Pin 32 (NC) to GND.
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1.0 OVERVIEW

Microchip’s MRF89XA is a fully integrated, half-duplex, sub-GHz transceiver. This low-power, single chip FSK and OOK baseband transceiver supports:

- Superheterodyne architecture
- Multi-channel, multi-band synthesizer with Phase Locked Loop (PLL) for easy RF design
- Power Amplifier (PA)
- Low Noise Amplifier (LNA)
- I/Q two stage down converter mixers
- I/Q demodulator, FSK/OOK
- Baseband filters and amplifiers

The simplified block diagram of the MRF89XA is illustrated in Figure 1-1.

The MRF89XA is a good option for low-cost, high-volume, low data rate (<200 kbps), and two-way short range wireless applications. This device is a single chip FSK and OOK transceiver capable of operating in the 863-870 MHz and 902-928 MHz license-free ISM frequency bands, and the 950-960 MHz frequency band.

The low-cost MRF89XA is optimized for very low-power consumption (3 mA in Receive mode). It incorporates a baseband modem with data rates up to 200 kbps in FSK and 32 kbps in OOK. Data handling features include a 64-byte FIFO, packet handling, automatic CRC generation and data whitening. The device also supports Manchester coding techniques. Its highly integrated architecture allows for minimum external component count while maintaining design flexibility. All major RF communication parameters are programmable and most of them may be dynamically set.

The MRF89XA supports a stable sensitivity and linearity characteristics for a wide supply range and is internally regulated. The frequency synthesizer of the MRF89XA is a fully integrated integer-N type PLL. The oscillator circuit provided on the MRF89XA device provides the reference clock for the PLL. The frequency synthesizer requires only five external components which includes PLL loop filter and the VCO tank circuit. Low-phase noise provides for excellent adjacent channel rejection capability, Bit Error Rate (BER) and longer communication range.

The high-resolution PLL allows:
- Usage of multiple channels in any of the bands
- Rapid settling time, which allows for faster frequency hopping

A communication link in most applications can be created using a low-cost 12.8 MHz crystal, a SAW filter and a low-cost microcontroller. The MRF89XA provides a clock signal for the microcontroller. The transceiver can be interfaced with many popular Microchip PIC® microcontrollers through a 4-wire Serial Peripheral Interface (SPI), interrupts (IRQ0 and IRQ1), PLL lock and clock out. The interface between the microcontroller and MRF89XA (a typical MRF89XA RF node) is illustrated in Figure 1-2.

The MRF89XA supports the following digital data processing features:
- Received Signal Strength Indicator (RSSI)
- Sync word recognition
- Packet handling
- Interrupt and flags
- Different operating Modes (Continuous, Buffer and Packet)
- Data filtering/whitening/encoding
- Baseband power amplifier
- 64-byte TX/RX FIFO

The role of the digital processing unit is to interface the data to/from the modulator/demodulator and the microcontroller access points (SPI, IRQ and DATA pins). It also controls all of the Configuration registers. The receiver’s Baseband Bandwidth (BBBW) can be programmed to accommodate various deviations and data rates requirements.

An optional Bit Synchronizer (BitSync) is provided, to supply a synchronous clock and data stream to a companion microcontroller in Continuous mode, or to fill the FIFO with glitch-free data in Buffered mode. The transceiver is integrated with different power-saving modes and a software wake-up time through the host microcontroller to keep track of the activities, which reduces the overall current consumption and extends the battery life. The small size and low-power consumption of the MRF89XA makes it ideal for various short range radio applications.

The MRF89XA complies with European (ETSI EN 300-220) and United States (FCC Part 15.247 and 15.249) regulatory standards.
FIGURE 1-1: MRF89XA SIMPLIFIED BLOCK DIAGRAM

- **LNA**: Low Noise Amplifier
- **First Stage Mixers**: Converts RF to IF
- **Second Stage Mixers**: Further converts IF to baseband
- **Modulation (DDS, DACs, Interpolation Filters)**: Generates the baseband signal
- **Filtering/Amplification**: Enhances the signal
- **RSSI**: Receiver Signal Strength Indicator
- **PLL Block (Comparator, VCO, Filter, Dividers)**: Provides the necessary frequency stability
- **Supply Block**: Provides power to the device
- **Transition Block**: Transmits the signal
- **Reception Block**: Receives the signal
- **Digital Demodulator**: Converts the signal to digital form
- **OOK Demodulator**: For ON-OFF Keying modulation
- **FSK Demodulator**: For Frequency Shift Keying modulation
- **Post-Demodulator**: Further processing of the demodulated signal
- **FIFO**: First-In, First-Out buffer
- **SYNC Word**: Provides synchronization information
- **Control Interface**: For control and management
- **Data Path**: PATH FOR DATA TRANSMISSION
- **Supply Crystal Loop Filter**: Filters the supply for stable operation
- **DVRS**: For general biasing
- **PARS**: Phase-Array Reference Synthesis
FIGURE 1-2: MRF89XA TO MICROCONTROLLER INTERFACE (NODE) BLOCK DIAGRAM

Note: The interface between the MRF89XA and the MCU depends on the Data mode of operation. For more information, refer to Section 3.8, Data Processing.
2.0 HARDWARE DESCRIPTION

The MRF89XA is an integrated, single chip, low-power ISM band sub-GHz transceiver. A detailed block diagram of the MRF89XA is illustrated in Figure 2-1. The frequency synthesizer is clocked by an external 12.8 MHz crystal, and frequency ranges from 863-870 MHz, 902-928 MHz and 950-960 MHz are possible.

The MRF89XA receiver employs a superheterodyne architecture. The first IF is one-ninth of the RF frequency (approximately 100 MHz). The second down conversion, down converts the I and Q signals to baseband in the case of the FSK receiver (zero-IF) and to a low-IF (IF2) for the OOK receiver. After the second down-conversion stage, the received signal is channel select filtered and amplified to a level adequate for demodulation. Both FSK and OOK demodulation are available. Image rejection is achieved using a SAW filter.

The baseband I and Q signals at the transmitter side are digitally generated by a Direct Digital Synthesis (DDS) whose Digital-to-Analog Converters (DAC) are followed by two anti-aliasing low-pass filters that transform the digital signal into analog In-Phase (I) and Quadrature (Q) components with frequency as the selected Frequency Deviation ($f_{\text{dev}}$). The transmitter supports both FSK and OOK modes of operation. The transmitter has a typical output power of +12.5 dBm. An internal transmit/receive switch combines the transmitter and receiver circuits into a single-ended RFIO pin (pin 31). The RFIO pin is connected through the impedance matching circuitry to an external antenna. The device operates in the low-voltage range of 2.1-3.6V, and in Sleep mode, it operates at a very low-current state, typically 0.1 µA.

The frequency synthesizer is based on an integer-N PLL having PLL bandwidth of 15 kHz. Two programmable frequency dividers in the feedback loop of the PLL and one programmable divider on the reference oscillator allow the LO frequency to be adjusted. The reference frequency is generated by a crystal oscillator running at 12.8 MHz.

The MRF89XA is controlled by a digital block that includes registers to store the configuration settings of the radio. These registers are accessed by a host microcontroller through a Serial Peripheral Interface (SPI). The quality of the data is validated using the RSSI and bit synchronizer blocks built into the transceiver. Data is buffered in a 64-byte transmitter or receiver FIFO. The transceiver is controlled through a 4-wire SPI, interrupts (IRQ0 and IRQ1), PLOCK, DATA and Chip Select pins for SPI are illustrated in Figure 2-1. On-chip regulators provide stable supply voltages to sensitive blocks and allow the MRF89XA to be used with supply voltages from 2.1-3.6V. Most blocks are supplied with a voltage below 1.4V.

The MRF89XA supports the following feature blocks:

- Data filtering and whitening
- Bit synchronization
- 64-byte transmit/receive FIFO buffer
- General configuration registers

These features reduce the processing load, which allows the use of simple, low-cost, 8-bit microcontrollers for data processing.
FIGURE 2-1: DETAILED BLOCK DIAGRAM OF THE MRF89XA
<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Pin Name</th>
<th>Pin Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TEST5</td>
<td>Digital I/O</td>
<td>Test Pin. Connected to Ground during normal operation.</td>
</tr>
<tr>
<td>2</td>
<td>TEST1</td>
<td>Digital I/O</td>
<td>Test Pin. Connected to Ground during normal operation.</td>
</tr>
<tr>
<td>3</td>
<td>VCORS</td>
<td>Analog Output</td>
<td>Regulated voltage supply of the VCO (0.85V).</td>
</tr>
<tr>
<td>4</td>
<td>VCOTN</td>
<td>Analog I/O</td>
<td>VCO tank.</td>
</tr>
<tr>
<td>5</td>
<td>VCOTP</td>
<td>Analog I/O</td>
<td>VCO tank.</td>
</tr>
<tr>
<td>6</td>
<td>PLLN</td>
<td>Analog I/O</td>
<td>PLL loop filter.</td>
</tr>
<tr>
<td>7</td>
<td>PLLP</td>
<td>Analog I/O</td>
<td>PLL loop filter.</td>
</tr>
<tr>
<td>8</td>
<td>TEST6</td>
<td>Digital I/O</td>
<td>Test Pin. Connected to Ground during normal operation.</td>
</tr>
<tr>
<td>9</td>
<td>TEST7</td>
<td>Digital I/O</td>
<td>Test Pin. Connected to Ground during normal operation.</td>
</tr>
<tr>
<td>10</td>
<td>OSC1</td>
<td>Analog Input</td>
<td>Crystal connection.</td>
</tr>
<tr>
<td>11</td>
<td>OSC2</td>
<td>Analog Input</td>
<td>Crystal connection.</td>
</tr>
<tr>
<td>12</td>
<td>TEST0</td>
<td>Digital Input</td>
<td>Test Pin. Connected to Ground during normal operation.</td>
</tr>
<tr>
<td>13</td>
<td>TEST8</td>
<td>Digital I/O</td>
<td>Test Pin. Allow pin to float; do not connect signal during normal operation.</td>
</tr>
<tr>
<td>14</td>
<td>CSCON</td>
<td>Digital Input</td>
<td>SPI Configure Chip Select.</td>
</tr>
<tr>
<td>15</td>
<td>CSDAT</td>
<td>Digital Input</td>
<td>SPI Data Chip Select.</td>
</tr>
<tr>
<td>16</td>
<td>SDO</td>
<td>Digital Output</td>
<td>Serial data output interface from MRF89XA.</td>
</tr>
<tr>
<td>17</td>
<td>SDI</td>
<td>Digital Input</td>
<td>Serial data input interface to MRF89XA.</td>
</tr>
<tr>
<td>18</td>
<td>SCK</td>
<td>Digital Input</td>
<td>Serial clock interface.</td>
</tr>
<tr>
<td>19</td>
<td>CLKOUT</td>
<td>Digital Output</td>
<td>Clock output. Output clock at reference frequency divided by a programmable factor. Refer to the Clock Output Control Register (Register 2-28) for more information.</td>
</tr>
<tr>
<td>20</td>
<td>DATA</td>
<td>Digital I/O</td>
<td>NRZ data input and output (Continuous mode).</td>
</tr>
<tr>
<td>21</td>
<td>IRQ0</td>
<td>Digital Output</td>
<td>Interrupt request output.</td>
</tr>
<tr>
<td>22</td>
<td>IRQ1</td>
<td>Digital Output</td>
<td>Interrupt request output.</td>
</tr>
<tr>
<td>23</td>
<td>PLOCK</td>
<td>Digital Output</td>
<td>PLL lock detection output. Refer to the FIFO Transmit PLL and RSSI Interrupt Request Configuration Register (Register 2-15) for more information.</td>
</tr>
<tr>
<td>24</td>
<td>TEST2</td>
<td>Digital I/O</td>
<td>Test Pin. Connected to Ground during normal operation.</td>
</tr>
<tr>
<td>25</td>
<td>TEST3</td>
<td>Digital I/O</td>
<td>Test Pin. Connected to Ground during normal operation.</td>
</tr>
<tr>
<td>26</td>
<td>Vdd</td>
<td>Power</td>
<td>Supply voltage.</td>
</tr>
<tr>
<td>27</td>
<td>AVRS</td>
<td>Analog Output</td>
<td>Regulated supply of the analog circuitry (1.0V).</td>
</tr>
<tr>
<td>28</td>
<td>DVRS</td>
<td>Analog Output</td>
<td>Regulated supply of the digital circuitry (1.0V).</td>
</tr>
<tr>
<td>29</td>
<td>PARS</td>
<td>Analog Output</td>
<td>Regulated supply of the PA (1.8V).</td>
</tr>
<tr>
<td>30</td>
<td>TEST4</td>
<td>Digital I/O</td>
<td>Test Pin. Connected to Ground during normal operation.</td>
</tr>
<tr>
<td>31</td>
<td>RFIO</td>
<td>Analog I/O</td>
<td>RF input/output (for more information, see Section 2.3, RFIO Pin).</td>
</tr>
<tr>
<td>32</td>
<td>NC</td>
<td>—</td>
<td>No Connection. Connected to Ground during normal operation.</td>
</tr>
<tr>
<td>33</td>
<td>Vss</td>
<td>Ground</td>
<td>Exposed Pad. Connected to Ground during normal operation.</td>
</tr>
</tbody>
</table>
2.1 Power Supply and Ground Block Pins

To provide stable sensitivity and linearity characteristics over a wide supply range, the MRF89XA is internally voltage regulated. This internal regulated power supply block structure is illustrated in Figure 2-2.

The power supply bypassing is essential for better handling of signal surges and noise in the power line. To ensure correct operation of the regulator circuit, the decoupling capacitor connection (shown in Figure 2-2) is recommended. These decoupling components are recommended for any design. The power supply block generates four regulated supplies for the analog, digital, VCO and the PLL blocks to reduce the voltages for their specific requirements. However, Power-on Reset (POR), Configuration registers and the SPI use the VDD supply given to the MRF89XA.

The large value decoupling capacitors should be placed at the PCB power input. The smaller value decoupling capacitors should be placed at every power point of the device and at bias points for the RF port. Poor bypassing can lead to conducted interference, which can cause noise and spurious signals to couple into the RF sections, thereby significantly reducing the performance.

It is recommended that the VDD pin have two bypass capacitors to ensure sufficient bypass and decoupling. However, based on the selected carrier frequency, the bypass capacitor values vary. The trace length (VDD pin to bypass capacitors) should be made as short as possible.

FIGURE 2-2: POWER SUPPLY BLOCK DIAGRAM

TABLE 2-2: POWER SUPPLY PIN DETAILS

<table>
<thead>
<tr>
<th>Blocks</th>
<th>Biasing Through</th>
<th>Associated Pins</th>
<th>Regulated Voltage (in Volts)</th>
</tr>
</thead>
<tbody>
<tr>
<td>POR, SPI and Configuration Registers</td>
<td>VDD</td>
<td>VDD</td>
<td>2.1–3.6</td>
</tr>
<tr>
<td>Regulated Supply (VINTS)</td>
<td>VDD</td>
<td>VDD</td>
<td>1.4</td>
</tr>
<tr>
<td>Analog</td>
<td>VINTS</td>
<td>AVRS</td>
<td>1.0</td>
</tr>
<tr>
<td>Digital</td>
<td>VINTS</td>
<td>DVRS</td>
<td>1.0</td>
</tr>
<tr>
<td>VCO</td>
<td>VINTS</td>
<td>VCORS</td>
<td>0.85</td>
</tr>
<tr>
<td>PA</td>
<td>VDD</td>
<td>PARS</td>
<td>1.8</td>
</tr>
</tbody>
</table>
2.2 Reset Pin

The device enters the Reset mode if any of the following events take place:

- Power-on Reset (POR)
- Manual Reset

The POR happens when the MRF89XA is switched on using VDD. The POR cycle takes at least 10 ms to execute any communication operations on the SPI bus.

An external hardware or manual Reset of the MRF89XA can be performed by asserting the TEST8 pin (pin 13) to high for 100 µs and then releasing the pin. After releasing the pin, it takes more than 5 ms for the transceiver to be ready for any operations. The pin is driven with an open-drain output, therefore, is pulled high while the device is in POR. The device will not accept commands during the Reset period. For more information, refer to Section 3.1.2, Manual Reset.

2.3 RFIO Pin

The receiver and the transmitter share the same RFIO pin (pin 31). Figure 2-3 illustrates the configuration of the common RF front-end.

- In Transmit mode, the PA and the PA regulator are ON with voltage on the PARS pin (pin 29) equal to the nominal voltage of the regulator (about 1.8V). The external RF choke inductance is used to bias the PA.
- In Receive mode, the PA and PA regulator are OFF and PARS is tied to ground. The external RF choke inductor is used for biasing and matching the LNA (this is basically implemented as a common gate amplifier).

2.4 Filters and Amplifiers Block

2.4.1 INTERPOLATION FILTER

After digital-to-analog conversion during transmission, both I and Q signals are smoothed by interpolation filters. These low-pass filters the digitally generated signal, and prevents the alias signals from entering the modulators.

2.4.2 POWER AMPLIFIER

The Power Amplifier (PA) integrated in the MRF89XA operates under a regulated voltage supply of 1.8V. The external RF choke inductor is biased by an internal regulator output made available on the PARS pin (pin 29). Therefore, the PA output power is consistent over the power supply range. This is important for applications which allows both predictable RF performance and battery life.

An open collector output requires biasing using an inductor as an RF choke. For the recommended PA bias and matching circuit details see Section 4.4.2, Suggested PA Biasing And Matching.

2.4.3 LOW NOISE AMPLIFIER (WITH FIRST MIXER)

In Receive mode, the RFIO pin (pin 31) is connected to a fixed gain, common-gate, Low Noise Amplifier (LNA). The performance of this amplifier is such that the Noise Figure (NF) of the receiver is estimated to be approximately 7 dB.

The LNA has approximately 50Ω impedance, which functions well with the proposed antenna (PCB/Monopole) during signal transmission. The LNA is followed by an internal RF band-pass filter.
2.4.4 IF GAIN AND SECOND I/Q MIXER

Following the LNA and first down-conversion, there is an IF amplifier whose gain can be programmed from 13.5-0 dB in 4.5 dB steps, through the register DMODREG. For more information, refer to Section 2.14.2, DATA AND MODULATION CONFIGURATION REGISTER DETAILS. The default setting corresponds to 0 dB gain, but lower values can be used to increase the RSSI dynamic range.

2.4.5 CHANNEL FILTERS

The second mixer stages are followed by the channel select filters. The channel select filters have a strong influence on the noise bandwidth and selectivity of the receiver and therefore, its sensitivity. Each channel select filter features a passive second-order RC filter, with a programmable bandwidth and the “fine” channel selection is performed by an active, third-order, Butterworth filter, which acts as a low-pass filter for the zero-IF configuration (FSK), or a complex polyphase filter for the low-IF (OOK) configuration. For more information on configuring passive and active filters see Section 3.4.4, Channel Filters.

2.5 Frequency Synthesizer Block

The frequency synthesizer of the MRF89XA is a fully integrated integer-N type PLL. The crystal oscillator provides the reference frequency for the PLL. The PLL circuit requires only a minimum of five external components for the PLL loop filter and the VCO tank circuit.

Figure 2-4 illustrates a block schematic of the MRF89XA PLL. Here the crystal reference frequency and the software controlled dividers R, P and S blocks determine the output frequency of the PLL. The VCO tank inductors are connected on an external differential input. Similarly, the loop filter is also located externally.

2.5.1 REFERENCE OSCILLATOR PINS

(OSC1/OSC2)

The MRF89XA has an internal, integrated oscillator circuit and the OSC1 and OSC2 pins are used to connect to an external crystal resonator. The crystal oscillator provides the reference frequency for the PLL. The crystal oscillator circuit, with the required loading capacitors, provides a 12.8 MHz reference signal for the PLL. The PLL then generates the local oscillator frequency. It is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. The crystal oscillator load capacitance is typically 15 pF, which allows the crystal oscillator circuit to accept a wide range of crystals.

Choosing a higher tolerance crystal results in a lower TX to RX frequency offset and the ability to select a smaller deviation in baseband bandwidth. Therefore, the recommended crystal accuracy should be \( \leq 40 \) ppm. The guidelines for selecting the appropriate crystal with specifications are explained in Section 4.6, Crystal Specification and Selection Guidelines.

Note: Crystal frequency error will directly translate to carrier frequency \( (f_c) \), bit rate and frequency deviation error.
2.5.2 CLKOUT OUTPUT PIN (CLKOUT)
The transceiver can provide a clock signal through the CLKOUT pin (pin 19) to the microcontroller for accurate timing, thereby eliminating the need for a second crystal. This results in reducing the component count. The CLKOUT is a sub-multiple of the reference frequency and is programmable.
The two main functions of the CLKOUT output are:
• To provide a clock output for a host microcontroller, thus saving the cost of an additional oscillator.
• To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

Note: To minimize the current consumption of the MRF89XA, ensure that the CLKOUT signal is disabled when unused.

CLKOUT can be made available in any operation mode, except Sleep mode, and is automatically enabled at power-up.

2.5.3 PHASE-LOCKED LOOP ARCHITECTURE
The Integer-N Phase-Locked Loop (PLL) circuitry determines the operating frequency of the device. The PLL maintains accuracy using the crystal-controlled reference oscillator and provides maximum flexibility in performance to the designers.
The high resolution of the PLL allows the use of multiple channels in any of the bands. The on-chip PLL is capable of performing manual and automatic calibration to compensate for the changes in temperature or operating voltage.

Note: Ensuring a symmetrical layout of the VCO inductors will further improve PLL spectral purity.

The output signal of the VCO is used as the input to the local oscillator (LO) generator stage, as illustrated in Figure 2-5. The VCO frequency is subdivided and used in a series of up/down conversions for transmission/reception.

FIGURE 2-5: LO VCO OUTPUT GENERATOR
2.6  MRF89XA Operating Modes
(Includes Power-Saving Mode)

This section summarizes the settings for each operating modes of the MRF89XA to save power that are based on the operations and available functionality. The timing requirements for switching between modes described in Section 5.3, Switching Times and Procedures.

2.6.1  MODES OF OPERATION

Table 2-3 lists the different operating modes of the MRF89XA, which can be used to save power.

2.6.2  DIGITAL PIN CONFIGURATION VS. CHIP MODE

Table 2-4 lists the state of the digital I/Os in each of the above described modes of operation, regardless of the data operating mode (Continuous, Buffered, or Packet).

### TABLE 2-3: OPERATING MODES

<table>
<thead>
<tr>
<th>Mode</th>
<th>CMOD&lt;2:0&gt; bits (GCONREG&lt;7:5&gt;</th>
<th>Active Blocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sleep</td>
<td>000</td>
<td>SPI, POR.</td>
</tr>
<tr>
<td>Stand-by</td>
<td>001</td>
<td>SPI, POR, Top regulator, digital regulator, XO, CLKOUT (if activated through CLKOREG).</td>
</tr>
<tr>
<td>FS</td>
<td>010</td>
<td>Same as Stand-by + VCO regulator, all PLL and LO generation blocks.</td>
</tr>
<tr>
<td>Receive</td>
<td>011</td>
<td>Same as FS mode + LNA, first mixer, IF amplifier, second mixer set, channel filters, baseband amplifiers and limiters, RSSI, OOK or FSK demodulator, BitSync and all digital features if enabled.</td>
</tr>
<tr>
<td>Transmit</td>
<td>100</td>
<td>Same as FS mode + DDS, Interpolation filters, all up-conversion mixers, PA driver, PA and external PARS pin (pin 29) output for the PA choke.</td>
</tr>
</tbody>
</table>

### TABLE 2-4: PIN CONFIGURATION VS. CHIP MODE

<table>
<thead>
<tr>
<th>Chip Mode Pin</th>
<th>Sleep Mode</th>
<th>Stand-by Mode</th>
<th>FS Mode</th>
<th>Receive Mode</th>
<th>Transmit Mode</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSCON</td>
<td>Input</td>
<td>Input</td>
<td>Input</td>
<td>Input</td>
<td>Input</td>
<td>CSCON has priority over CSDAT.</td>
</tr>
<tr>
<td>CSDAT</td>
<td>Input</td>
<td>Input</td>
<td>Input</td>
<td>Input</td>
<td>Input</td>
<td>—</td>
</tr>
<tr>
<td>SDO(4)</td>
<td>Output</td>
<td>Output</td>
<td>Output</td>
<td>Output</td>
<td>Output</td>
<td>Output only if CSCON or CSDAT = 0.</td>
</tr>
<tr>
<td>SDI</td>
<td>Input</td>
<td>Input</td>
<td>Input</td>
<td>Input</td>
<td>Input</td>
<td>—</td>
</tr>
<tr>
<td>SCK</td>
<td>Input</td>
<td>Input</td>
<td>Input</td>
<td>Input</td>
<td>Input</td>
<td>—</td>
</tr>
<tr>
<td>IRQ0(3)</td>
<td>High-Z</td>
<td>Output(1)</td>
<td>Output(1)</td>
<td>Output</td>
<td>Output</td>
<td>—</td>
</tr>
<tr>
<td>IRQ1(3)</td>
<td>High-Z</td>
<td>Output(1)</td>
<td>Output(1)</td>
<td>Output</td>
<td>Output</td>
<td>—</td>
</tr>
<tr>
<td>DATA</td>
<td>Input</td>
<td>Input</td>
<td>Input</td>
<td>Output</td>
<td>Input</td>
<td>—</td>
</tr>
<tr>
<td>CLKOUT</td>
<td>High-Z</td>
<td>Output</td>
<td>Output</td>
<td>Output</td>
<td>Output</td>
<td>—</td>
</tr>
<tr>
<td>PLOCK</td>
<td>High-Z</td>
<td>Output(2)</td>
<td>Output(2)</td>
<td>Output</td>
<td>Output(2)</td>
<td>—</td>
</tr>
</tbody>
</table>

Note 1:  High-Z if Continuous mode is activated; otherwise, Output.
2:  Output if LENPLL = 1; otherwise, High-Z.
3:  Valid logic states must be applied to inputs at all times to avoid unwanted leakage currents. Suggestions for designers,
   • Use external pull down resistor.
   • Tristate the Microcontroller interrupt pin to output when setting the MRF89XA to sleep. Then reverse when waking it up. Since the Microcontroller is in control, this should be easy to do and not require an external pull down resistor.
4:  The SDO pin defaults to a high impedance (High-Z) state when any of the CS pins are high (the MRF89XA is not selected).
2.7 Interrupt (IRQ0 and IRQ1) Pins

The Interrupt Requests (IRQ0 and IRQ1) pins 21 and 22, provide an interrupt signal to the host microcontroller from the MRF89XA. Interrupt requests are generated for the host microcontroller by pulling the IRQ0 (pin 21) or IRQ1 (pin 22) pins low or high based on the events and configuration settings of these interrupts. Interrupts must be enabled and unmasked before the IRQ pins are active. For detailed functional description of interrupts, see Section 3.8, Data Processing.

2.8 DATA Pin

After OOK or FSK demodulation, the baseband signal is available to the user on the DATA pin (pin 20), when Continuous mode is selected. Therefore, in Continuous mode, the NRZ data to or from the modulator or demodulator respectively is directly accessed by the host microcontroller on the bidirectional DATA pin. The SPI Data, FIFO and packet handler are therefore inactive. In Buffered and Packet modes, the data is retrieved from the FIFO through the SPI.

During transmission, the DATA pin is configured as DATA (Data Out) and with internal Transmit mode disabled; this manually modulates the data from the external host microcontroller. If the Transmit mode is enabled, this pin can be tied “high” or can be left unconnected.

During reception, the DATA pin is configured as DATA (Data In); this pin receives the data in conjunction with DCLK. DATA pin (unused in packed mode) should be pulled-up to VDD through a 100 kΩ resistor.

2.9 Transmitter

The transmitter chain is based on the same doubleconversion architecture and uses the same intermediate frequencies as the receiver chain. The main blocks include:

- A digital waveform generator that provides the I and Q base-band signals. This block includes digital-to-analog converters and anti-aliasing low-pass filters.
- A compound image-rejection mixer to up-convert the baseband signal to the first IF at one-ninth of the carrier frequency (f0), and a second image-rejection mixer to up-convert the IF signal to the RF frequency transmitter driver and power amplifier stages to drive the antenna port.
2.9.1 TRANSMITTER ARCHITECTURE

Figure 2-6 illustrates the transmitter architecture block diagram. The baseband I and Q signals are digitally generated by a DDS whose Digital-to-Analog Converters (DAC) followed by two anti-aliasing low-pass filters transform the digital signal into analog in-phase (I) and quadrature (Q) components whose frequency is the selected frequency deviation, set using the FDVAL<7:0> bits from FDEVREG<7:0>.

In FSK mode, the relative phase of I and Q is switched by the input data between -90° and +90° with continuous phase. The modulation is therefore performed at this initial stage, because the information contained in the phase difference will be converted into a frequency shift when the I and Q signals are up-converted in the first mixer stage. This first up-conversion stage is duplicated to enhance image rejection. The FSK convention is such that:

\[
\text{DATA} = 1 \rightarrow f_{rf} + f_{dev}
\]
\[
\text{DATA} = 0 \rightarrow f_{rf} - f_{dev}
\]

In OOK mode, the phase difference between the I and Q channels is kept constant (independent of the transmitted data). Thus, the first stage of up-conversion creates a fixed frequency signal at the low IF = f_{dev} (this explains why the transmitted OOK spectrum is offset by f_{dev}). OOK Modulation is accomplished by switching the PA and PA regulator stages ON and OFF. By convention:

\[
\text{DATA} = 1 \rightarrow P\text{Aon}
\]
\[
\text{DATA} = 0 \rightarrow P\text{Aoff}
\]

After the interpolation filters, a set of four mixers combines the I and Q signals and converts them into a pair of complex signals at the second intermediate frequency, equal to one-eighth of the LO frequency, or one-ninth of the RF frequency. These two new I and Q signals are then combined and up-converted to the final RF frequency by two quadrature mixers fed by the LO signal. The signal is pre-amplified, and then the transmitter output is driven by a final power amplifier stage. The I and Q signal details are illustrated in Figure 2-7.

FIGURE 2-7: I(t), Q(t) Signals Overview

In OOK mode, the phase difference between the I and Q channels is kept constant (independent of the transmitted data). Thus, the first stage of up-conversion creates a fixed frequency signal at the low IF = f_{dev} (this explains why the transmitted OOK spectrum is offset by f_{dev}). OOK Modulation is accomplished by switching the PA and PA regulator stages ON and OFF. By convention:

\[
\text{DATA} = 1 \rightarrow P\text{Aon}
\]
\[
\text{DATA} = 0 \rightarrow P\text{Aoff}
\]

After the interpolation filters, a set of four mixers combines the I and Q signals and converts them into a pair of complex signals at the second intermediate frequency, equal to one-eighth of the LO frequency, or one-ninth of the RF frequency. These two new I and Q signals are then combined and up-converted to the final RF frequency by two quadrature mixers fed by the LO signal. The signal is pre-amplified, and then the transmitter output is driven by a final power amplifier stage. The I and Q signal details are illustrated in Figure 2-7.
2.10 Receiver

The receiver is based on a superheterodyne architecture and comprises the following major blocks:

- An LNA that provides low-noise RF gain followed by an RF band-pass filter.
- A first mixer, which down-converts the RF signal to an intermediate frequency equal to one-ninth of the carrier frequency (f_{rf} 100 MHz for 915 MHz signals).
- A variable gain first-IF preamplifier followed by two second mixers, which down-convert the first IF signal to I and Q signals at a low frequency (zero-IF for FSK, low-IF for OOK).
- A two-stage IF filter followed by an amplifier chain are available for both I and Q channels. Limiters at the end of each chain drive the I and Q inputs to the FSK demodulator function. An RSSI signal is also derived from the I and Q IF amplifiers to drive the OOK detector. The second filter stage in each channel can be configured as either a third-order Butterworth low-pass filter for FSK operation or an image reject polyphase band-pass filter for OOK operation.
- An FSK arctangent type demodulator driven from the I and Q limiter outputs, and an OOK demodulator driven by the RSSI signal. Either detector can drive a data and clock recovery function that provides matched filter enhancement of the demodulated data.

2.10.1 RECEIVER ARCHITECTURE

Figure 2-8 illustrates the receiver architecture block diagram. The first IF is one-ninth of the RF frequency (approximately 100 MHz). The second down-conversion down-converts the I and Q signals to baseband in the case of the FSK receiver (zero-IF) and to a low-IF (IF2) for the OOK receiver.

After the second down-conversion stage, the received signal is channel-select filtered and amplified to a level adequate for demodulation. Both FSK and OOK demodulation are available. Finally, an optional bit synchronizer (BitSync) is provided to supply a synchronous clock and data stream to a companion microcontroller in Continuous mode, or to fill the FIFO buffers with glitch-free data in Buffered mode.

**Note:** Image rejection is achieved using a SAW filter on the RF input.

---

**FIGURE 2-8: RECEIVER ARCHITECTURE BLOCK DIAGRAM**

![Receiver Architecture Block Diagram](image-url)
FIGURE 2-9: FSK RECEIVER SETTING

Approx. 100 MHz

First down-conversion

Second down-conversion

IF2 ≠ 0 in FSK mode

IF1

LO2 RX

Image Frequency

LO1 RX Channel

Frequency

FIGURE 2-10: OOK RECEIVER SETTING

IF2 < 0 in FSK mode equal to $f_o$

Approx. 100 MHz

First down-conversion

Second down-conversion

Image Frequency

LO1 RX Channel

Frequency
2.11 Serial Peripheral Interface (SPI)

The MRF89XA communicates with the host microcontroller through a 4-wire SPI port as a slave device. An SPI-compatible serial interface allows the user to select, command and monitor the status of the MRF89XA through the host microcontroller. All the registers are addressed through the specific addresses to control, configure and read status bytes.

The SPI in the MRF89XA consists of the following two sub-blocks, as illustrated in Figure 2-11.

- SPI CONFIG: This sub-block is used in all data operation modes to read and write the configuration registers which control all the parameters of the chip (operating mode, frequency and bit rate).
- SPI DATA: This sub-block is used in Buffered and Packet mode to write and read data bytes to and from the FIFO. (FIFO Interrupts can be used to manage the FIFO content).

Both of these SPIs are configured in Slave mode while the host microcontroller is configured as the master. They have separate selection pins (CSCON and CSDAT) but share the remaining pins:

- SCK (SPI Clock): Clock signal provided by the host microcontroller
- SDI (SPI Input): Data Input signal provided by the host microcontroller
- SDO (SPI Output): Data Output signal provided by the MRF89XA

As listed in Table 2-5, only one interface can be selected at a time with CSCON having the priority:

<table>
<thead>
<tr>
<th>CSDAT</th>
<th>CSCON</th>
<th>SPI</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>CONFIG</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>DATA</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>CONFIG</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>None</td>
</tr>
</tbody>
</table>

All the parameters can be programmed and set through the SPI module. Any of these auxiliary functions can be disabled when it is not required. After power-on, all parameters are set to default values. The programmed values are retained during Sleep mode. The interface supports the read out of a status register, which provides detailed information about the status of the transceiver and the received data.

The MRF89XA supports SPI mode 0,0, which requires the SCK to remain idle in a low state. The CS pins, CSCON and CSDAT based on the mode (pin 14 and 15), must be held low to enable communication between the host microcontroller and the MRF89XA. The device’s timing specification details are listed in Table 5-7. The SDO pin defaults to a high impedance (hi-Z) state when any of the CS pins are high (the MRF89XA is not selected). This pin has a tri-state buffer and uses a bus hold logic.

As the device uses byte writes, any of the Chip Select (CS) pins should be pulled low for 8 bits. Data bits on the SDI pin (pin 17) are shifted into the device upon the rising edge of the clock on the SCK pin (pin 18) whenever the CS pins are low. The maximum clock frequency for the SPI clock for CONFIG mode is 6 MHz. However, maximum SPI Clock for DATA mode (to read/write FIFO) is 1 MHz. Data is received by the transceiver through the SDI pin and is clocked on the rising edge of SCK. The MRF89XA sends the data through the SDO pin and is clocked out on the falling edge of SCK. The Most Significant bit (MSb) is sent first in any data.

The SPI sequence diagrams are illustrated in Figure 2-12 through Figure 2-15.
2.11.1 SPI CONFIG

Write Register - To write a value into a Configuration register, the timing diagram illustrated in Figure 2-12 should be followed by the host microcontroller. The new value of the register is effective from the rising edge of CSCON.

Note: When writing more than one register successively, it is not compulsory to toggle CSCON back high between two write sequences. The bytes are alternatively considered as address and value. In this instance, all new values will become effective on rising edge of CSCON.

Read Register - To read the value of a Configuration register, the timing diagram illustrated in Figure 2-13 should be followed by the host microcontroller.

Note: When reading more than one register successively, it is not compulsory to toggle CSCON back high between two read sequences. The bytes are alternatively considered as address and value.
2.11.2 SPI DATA

Write Byte (before/during TX) - To write bytes into the FIFO, the timing diagram illustrated in Figure 2-14 should be followed by the host microcontroller.

Note: It is compulsory to toggle CSDAT back high between each byte written. The byte is pushed into the FIFO on the rising edge of CSDAT.

FIGURE 2-14: WRITE BYTES SEQUENCE (EXAMPLE DIAGRAM FOR 2 BYTES)

Read Byte (after/during RX) - To read bytes from the FIFO, the timing diagram illustrated in Figure 2-15 should be followed by the host microcontroller.

Note: It is recommended to toggle CSDAT back high between each byte read.

FIGURE 2-15: READ BYTES SEQUENCE (EXAMPLE DIAGRAM FOR 2 BYTES)
2.12 FIFO and Shift Register (SR)

In Buffered and Packet modes of operation, data to be transmitted and data that has been received are stored in a configurable First In First Out (FIFO) buffer. The FIFO is accessed through the SPI data interface and provides several interrupts for transfer management.

The FIFO is 1 byte (8 bits) wide; therefore, it only performs byte (parallel) operations, whereas the demodulator functions serially. A shift register (SR) is therefore employed to interface the demodulator and the FIFO. In Transmit mode it takes bytes from the FIFO and outputs them serially (MSB first) at the programmed bit rate to the modulator. Similarly, in Receive mode the shift register gets bit-by-bit data from the demodulator and writes them byte-by-byte to the FIFO. This is illustrated in Figure 2-16.

2.13 MRF89XA Configuration, Control and Status Registers

The memory in the MRF89XA transceiver is implemented as static RAM and is accessible through the SPI port. The memory configuration of the MRF89XA is illustrated in Figure 2-17 and Figure 2-18.
The MRF89XA registers functionally handles command, configuration, control, status or data/FIFO fields as listed in Table 2-6. The registers operate on parameters common to transmit and receive modes, Interrupts, Sync pattern, crystal oscillator and packets. The FIFO serves as a buffer for data transmission and reception. There is a shifted register (SR) to handle bit shifts for the FIFO during transmission and reception. POR sets default values in all Configuration/Control/Status registers.
### TABLE 2-6: CONFIGURATION/CONTROL/STATUS REGISTER DESCRIPTION

#### General Configuration Registers: Size – 13 Bytes, Start Address – 0x00

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>GCONREG</td>
<td>General Configuration Register</td>
<td>Transceiver mode, frequency band selection, VCO trimming, PLL frequency dividers selection</td>
</tr>
<tr>
<td>0x01</td>
<td>DMODREG</td>
<td>Data and Modulation Configuration Register</td>
<td>Modulation type, Data mode, OOK threshold type, IF gain</td>
</tr>
<tr>
<td>0x02</td>
<td>FDEVREG</td>
<td>Frequency Deviation Control Register</td>
<td>Frequency deviation in FSK Transmit mode</td>
</tr>
<tr>
<td>0x03</td>
<td>BRSREG</td>
<td>Bit Rate Set Register</td>
<td>Operational bit rate</td>
</tr>
<tr>
<td>0x04</td>
<td>FLTHREG</td>
<td>Floor Threshold Control Register</td>
<td>Floor threshold in OOK Receive mode</td>
</tr>
<tr>
<td>0x05</td>
<td>FIFOCREG</td>
<td>FIFO Configuration Register</td>
<td>FIFO size and threshold</td>
</tr>
<tr>
<td>0x06</td>
<td>R1CREG</td>
<td>R1 Counter Set Register</td>
<td>Value input for R1 counter</td>
</tr>
<tr>
<td>0x07</td>
<td>P1CREG</td>
<td>P1 Counter Set Register</td>
<td>Value input for P1 counter</td>
</tr>
<tr>
<td>0x08</td>
<td>S1CREG</td>
<td>S1 Counter Set Register</td>
<td>Value input for S1 counter</td>
</tr>
<tr>
<td>0x09</td>
<td>R2CREG</td>
<td>R2 Counter Set Register</td>
<td>Value input for R2 counter</td>
</tr>
<tr>
<td>0x0A</td>
<td>P2CREG</td>
<td>P2 Counter Set Register</td>
<td>Value input for P2 counter</td>
</tr>
<tr>
<td>0x0B</td>
<td>S2CREG</td>
<td>S2 Counter Set Register</td>
<td>Value input for S2 counter</td>
</tr>
<tr>
<td>0x0C</td>
<td>PACREG</td>
<td>Power Amplifier Control Register</td>
<td>Ramp Control of PA regulator output voltage in OOK</td>
</tr>
</tbody>
</table>

#### Interrupt Configuration Registers: Size – 3 Bytes, Start Address – 0x0D

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0D</td>
<td>FTXRXIREG</td>
<td>FIFO, Transmit and Receive Interrupt Request Configuration Register</td>
<td>Interrupt request (IRQ0 and IRQ1) in Receive mode, interrupt request (IRQ1) in Transmit mode, interrupt request for FIFO full, empty and overrun</td>
</tr>
<tr>
<td>0x0E</td>
<td>FTPRIIREG</td>
<td>FIFO Transmit PLL and RSSI Interrupt Configuration Register</td>
<td>FIFO fill method, FIFO fill, interrupt request (IRQ0) for transmit start, interrupt request for RSSI, PLL lock enable and status</td>
</tr>
<tr>
<td>0x0F</td>
<td>RSTHIREG</td>
<td>RSSI Threshold Interrupt Request Configuration Register</td>
<td>RSSI threshold for interrupt</td>
</tr>
</tbody>
</table>

#### Receiver Configuration Registers: Size – 6 Bytes, Start Address – 0x10

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x10</td>
<td>FILCREG</td>
<td>Filter Configuration Register</td>
<td>Passive filter bandwidth selection, sets the receiver bandwidth (Butterworth filter)</td>
</tr>
<tr>
<td>0x11</td>
<td>PFCREG</td>
<td>Polyphase Filter Configuration Register</td>
<td>Selects the central frequency of the polyphase filter</td>
</tr>
<tr>
<td>0x12</td>
<td>SYMCREG</td>
<td>Sync Control Register</td>
<td>Enables polyphase filter (in OOK receive mode, bit synchronizer control, Sync word recognition, Sync word size, Sync word error)</td>
</tr>
<tr>
<td>0x13</td>
<td>RESVREG</td>
<td>Reserved Register</td>
<td>Reserved for future use</td>
</tr>
</tbody>
</table>
### Receiver Configuration Registers: Size – 6 Bytes, Start Address – 0x14

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x14</td>
<td>RSTSREG</td>
<td>RSSI Status Read Register</td>
<td>RSSI output</td>
</tr>
<tr>
<td>0x15</td>
<td>OOKCREG</td>
<td>OOK Configuration Register</td>
<td>RSSI threshold size in OOK demodulator, RSSI threshold period in OOK demodulator, cut-off frequency of the OOK threshold in demodulator</td>
</tr>
</tbody>
</table>

### Sync Word Configuration Registers: Size – 4 Bytes, Start Address – 0x16

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x16</td>
<td>SYNCV31REG</td>
<td>Sync Value 1st Byte Configuration Register</td>
<td>Configuring first byte of the 32-bit Sync word</td>
</tr>
<tr>
<td>0x17</td>
<td>SYNCV23REG</td>
<td>Sync Value 2nd Byte Configuration Register</td>
<td>Configuring second byte of the 32-bit Sync word</td>
</tr>
<tr>
<td>0x18</td>
<td>SYNCV15REG</td>
<td>Sync Value 3rd Byte Configuration Register</td>
<td>Configuring third byte of the 32-bit Sync word</td>
</tr>
<tr>
<td>0x19</td>
<td>SYNCV07REG</td>
<td>Sync Value 4th Byte Configuration Register</td>
<td>Configuring fourth byte of the 32-bit Sync word</td>
</tr>
</tbody>
</table>

### Transmitter Configuration Registers: Size – 1 Byte, Start Address – 0x1A

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1A</td>
<td>TXCONREG</td>
<td>Transmit Configuration Register</td>
<td>Transmit interpolation cut-off frequency, power output</td>
</tr>
</tbody>
</table>

### Oscillator Configuration Registers: Size – 1 Byte, Start Address – 0x1B

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1B</td>
<td>CLKOREG</td>
<td>Clock Output Control Register</td>
<td>Clock-out control, frequency</td>
</tr>
</tbody>
</table>

### Packet Handling Configuration Registers: Size – 4 Bytes, Start Address – 0x1C

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1C</td>
<td>PLOADREG</td>
<td>Payload Configuration Register</td>
<td>Enable Manchester encoding/decoding, payload length</td>
</tr>
<tr>
<td>0x1D</td>
<td>NADDSREG</td>
<td>Node Address Set Register</td>
<td>Node’s local address for filtering of received packets</td>
</tr>
<tr>
<td>0x1E</td>
<td>PKTCREG</td>
<td>Packet Configuration Register</td>
<td>Packet format, size of the preamble, whitening, CRC on/off, address filtering of received packets, CRC status</td>
</tr>
<tr>
<td>0x1F</td>
<td>FCRCREG</td>
<td>FIFO CRC Configuration Register</td>
<td>FIFO auto-clear (if CRC failed), FIFO access</td>
</tr>
</tbody>
</table>
2.14 General Configuration Registers

2.14.1 GENERAL CONFIGURATION REGISTER DETAILS

REGISTER 2-1: GCONREG: GENERAL CONFIGURATION REGISTER (ADDRESS:0X000) (POR:0X28)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOD&lt;2:0&gt;</td>
<td>FBS&lt;1:0&gt;</td>
<td>VCOT&lt;1:0&gt;</td>
<td>RPS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

R = Readable bit  W = Writable bit  U = Unimplemented bit, read as ‘0’
-n = Value at POR  ‘1’ = Bit is set  ‘0’ = Bit is cleared  x = Bit is unknown
r = Reserved

bit 7-5  CMOD<2:0>: Chip Mode bits
These bits select the mode of operation of the transceiver.
111 = Reserved; do not use
110 = Reserved; do not use
101 = Reserved; do not use
100 = Transmit mode
011 = Receive mode
010 = Frequency Synthesizer mode
001 = Stand-by mode (default)
000 = Sleep mode

bit 4-3  FBS<1:0>: Frequency Band Select bits
These bits set the frequency band to be used in Sub-GHz range.
11 = Reserved
10 = 950-960 MHz or 863-870 MHz (application circuit dependent)
01 = 915-928 MHz (default)
00 = 902-915 MHz

bit 2-1  VCOT<1:0>: TX bits
For each AFC cycle run, these bits will toggle between logic ‘1’ and logic ‘0’.
11 = Vtune + 180 mV typ
10 = Vtune + 120 mV typ
01 = Vtune + 60 mV typ
00 = Vtune determined by tank inductors values (default)

bit 0  RPS: RPS Select bit
This bit selects between the two sets of frequency dividers of the PLL, Ri/Pi/Si. For more information, see Section 3.2.7, Frequency Calculation.
1 = Enable R2/P2/S2 set
0 = Enable R1/P1/S1 set (default)
2.14.2 DATA AND MODULATION CONFIGURATION REGISTER DETAILS

REGISTER 2-2: DMODREG: DATA AND MODULATION CONFIGURATION REGISTER
(ADDRESS:0X01) (POR:0X88)

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MODSEL&lt;1:0&gt;</td>
<td>DMODE0</td>
<td>OOKTYP&lt;1:0&gt;</td>
<td>DMODE1</td>
<td>IFGAIN&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown

R = Reserved

bit 7-6 MODSEL<1:0>: Modulation Type Selection bits
These bits set the type of modulation to be used in Sub-GHz range.
11 = Reserved
10 = FSK (default)
01 = OOK
00 = Reserved

bit 5 DMODE0: Data Mode 0 bit
Setting this bit selects the data operational mode as LSB. Use this bit with DMODE1 to select the operational mode.
0 = Default

bit 4-3 OOKTYP<1:0>: OOK Demodulator Threshold Type bits
The combination of these bits selects the Demodulator Threshold Type for operation.
11 = Reserved
10 = Average Mode
01 = Peak Mode (default)
00 = Fixed threshold mode

bit 2 DMODE1: Data Mode 1 bit
Setting this bit selects the data operational mode as MSB. Use this bit with DMODE0 to select the operational mode.
0 = Default

bit 1-0 IFGAIN<1:0>: IF Gain bits.
Selects gain on the IF chain.
11 = -13.5 dB
10 = -9 dB
01 = -4.5 dB
00 = 0 dB (maximal gain) (default)

Note 1: The combination of DMODE1:DMODE0 selects the Data Operation mode. See Table 2-7 for the available Data Operation mode settings.

TABLE 2-7: DATA OPERATION MODE SETTINGS

<table>
<thead>
<tr>
<th>Data Operation Mode</th>
<th>DMODE1</th>
<th>DMODE0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Continuous (default mode)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Buffer</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Packet</td>
<td>1</td>
<td>x (x = 0/1)</td>
</tr>
</tbody>
</table>
2.14.3 FREQUENCY DEVIATION CONTROL REGISTER DETAILS

REGISTER 2-3: FDEVREG: FREQUENCY DEVIATION CONTROL REGISTER
(ADDRESS:0x02) (POR:0x03)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FDVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’

-bit = Value at POR  
‘1’ = Bit is set  
‘0’ = Bit is cleared  
x = Bit is unknown

r = Reserved

bit 7-0  

FDVAL<7:0>: Frequency Deviation Value bits

The bits indicate single side frequency deviation (in bit value) in FSK Transmit mode.

\[
 f_{dev} = \frac{f_{xtal}}{(32 \times (FDVAL + 1))}
\]

Where,
FDVAL is the value in the register and has the range from 0 ≤ FDVAL ≤ 255. Refer to Section 3.3.3, fdev Setting in FSK Mode and Section 3.3.4, fdev Setting in OOK Mode for more information on the fdev setting for FSK and OOK modes.

**Note 1:**  
fdev is used throughout the data sheet to understand the term frequency deviation and is calculated using FDVAL<7:0> from FDEVREG.

2.14.4 BIT RATE SET REGISTER DETAILS

REGISTER 2-4: BRSREG: BIT RATE SET REGISTER (ADDRESS:0x03) (POR:0x07)

<table>
<thead>
<tr>
<th>r</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as ‘0’

-bit = Value at POR  
‘1’ = Bit is set  
‘0’ = Bit is cleared  
x = Bit is unknown

r = Reserved

bit 7  

Reserved: Reserved bit; do not use

0 = Reserved (default)

bit 6-0  

BRVAL<6:0>: Bit Rate Value bits

These bits set the bit rate (in bit value) of:

\[
 BitRate = \frac{f_{xtal}}{(64(BRVAL + 1))}
\]

BRVAL<6:0> = 0000111 ≥ Bit Rate = 25 kbps NRZ (default)

Where, BRVAL is the value in the register and has the range from 0 ≤ BRVAL ≤ 127

**Note 1:**  
The Bit Rates are good for crystal frequency of 12.8 MHz which is taken as reference throughout the data sheet.
2.14.5 FLOOR THRESHOLD CONTROL
REGISTER DETAILS

REGISTER 2-5: FLTHREG: FLOOR THRESHOLD CONTROL REGISTER
(ADDRESS: 0x04) (POR: 0x0C)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FTOVAL<7:0>:** Floor Threshold OOK Value bits
The bits indicate Floor threshold in OOK receive mode.
FTOVAL<7:0> = 00001100 ≥ 6 dB (default)
FTOVAL assumes 0.5 dB RSSI Step

2.14.6 FIFO CONFIGURATION REGISTER
DETAILS

REGISTER 2-6: FIFOCREG: FIFO CONFIGURATION REGISTER (ADDRESS: 0x05) (POR: 0x0F)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FSIZE<1:0>:** FIFO Size Selection bits
These bits set the size/number of FIFO locations.
11 = 64 bytes
10 = 48 bytes
01 = 32 bytes
00 = 16 bytes (default)

**FTINT<5:0>:** FIFO Threshold Interrupt bits
Setting these bits selects the FIFO threshold for interrupt source. Refer to Section 3.6.2, Interrupt Sources and Flags for more information.

FTINT<5:0> = 001111 (default)
FIFO_THRESHOLD interrupt source's behavior depends on the running mode (TX, RX or Stand-by mode).
2.14.7 R1 COUNTER SET REGISTER
DETAILS

REGISTER 2-7:  R1CREG: R1 COUNTER SET REGISTER (ADDRESS:0x06) (POR:0x77)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1CVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7-0  R1CVAL<7:0>: R1 Value bits
These bits indicate the value in R1 counter to generate carrier frequencies in FSK mode. R1CVAL<7:0> = 0x77 (default)
R1CVAL is activated if RPS = 0 in GCONREG. Also, default values R1, P1 and S1 generate 915 MHz in FSK Mode.

2.14.8 P1 COUNTER SET REGISTER
DETAILS

REGISTER 2-8:  P1CREG: P1 COUNTER SET REGISTER (ADDRESS:0x07) (POR:0x64)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1CVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7-0  P1CVAL<7:0>: P1 Value bits
These bits indicate the value in P1 counter to generate carrier frequencies in FSK mode. P1CVAL<7:0> = 0x64 (default)
P1CVAL is activated if RPS = 0 in GCONREG. Also default values R1, P1 and S1 generate 915 MHz in FSK Mode.
2.14.9 S1 COUNTER SET REGISTER DETAILS

REGISTER 2-9:  S1CREG: S1 COUNTER SET REGISTER (ADDRESS:0x08) (POR:0x32)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S1CVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7-0  S1CVAL<7:0>: S1 Value bits
These bits indicate the value in S1 counter to generate carrier frequencies in FSK mode.
S1CVAL<7:0> = 0x32 (default)

S1CVAL is activated if RPS = 0 in GCONREG. Also default values R1, P1 and S1 generate 915 MHz in FSK Mode.

2.14.10 R2 COUNTER SET REGISTER DETAILS

REGISTER 2-10:  R2CREG: R2 COUNTER SET REGISTER (ADDRESS:0x09) (POR:0x74)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R2CVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7-0  R2CVAL<7:0>: R2 Value bits
These bits indicate the value in R2 counter to generate carrier frequencies in FSK mode.
R2CVAL<7:0> = 0x74 (default)

R2CVAL is activated if RPS = 1 in GCONREG. Also default values R2, P2 and S2 generate 920 MHz in FSK Mode.
2.14.11  P2 COUNTER SET REGISTER

DETAILS

REGISTER 2-11:  P2CREG: P2 COUNTER SET REGISTER (ADDRESS:0x0A) (POR:0x62)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>P2CVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown
r = Reserved

bit 7-0  P2CVAL<7:0>: P2 Value bits

These bits indicate the value in P2 counter to generate carrier frequencies in FSK mode.
P2CVAL<7:0> = 0x62 (default)
P2CVAL is activated if RPS = 1 in GCONREG. Also default values R2, P2 and S2 generate 920 MHz in FSK Mode.

2.14.12  S2 COUNTER SET REGISTER

DETAILS

REGISTER 2-12:  S2CREG: S2 COUNTER SET REGISTER (ADDRESS:0x0B) (POR:0x32)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>S2CVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

R = Readable bit
W = Writable bit
U = Unimplemented bit, read as ‘0’
-n = Value at POR
‘1’ = Bit is set
‘0’ = Bit is cleared
x = Bit is unknown
r = Reserved

bit 7-0  S2CVAL<7:0>: S2 Value bits

These bits indicate the value in S2 counter to generate carrier frequencies in FSK mode.
S2CVAL<7:0> = 0x32 (default).
S2CVAL is activated if RPS = 1 in GCONREG. Also default values R2, P2 and S2 generate 920 MHz in FSK Mode.
2.14.13 **POWER AMPLIFIER CONTROL REGISTER DETAILS**

**REGISTER 2-13: PACREG: POWER AMPLIFIER CONTROL REGISTER**

ADDRESS:0x0C  (POR:0x38)

<p>| | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>R/W-1</td>
<td>R/W-1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7-5</td>
<td><strong>Reserved</strong>: Reserved bits; do not use</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>001</td>
<td>Reserved (default)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 4-3</td>
<td><strong>PARC&lt;1:0&gt;</strong>: Power Amplifier Ramp Control bits. These bits control the RAMP rise and fall times of the TX PA regulator output voltage in OOK mode.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>23 µs (default)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>15 µs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>01</td>
<td>8.5 µs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>00</td>
<td>3 µs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 2-0</td>
<td><strong>Reserved</strong>: Reserved bits; do not use</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>000</td>
<td>Reserved (default)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
2.15 Interrupt Configuration Registers

2.15.1 FIFO TRANSMIT AND RECEIVE INTERRUPT REQUEST CONFIGURATION REGISTER DETAILS

REGISTER 2-14: FTXRXIREG: FIFO TRANSMIT AND RECEIVE INTERRUPT REQUEST CONFIGURATION REGISTER (ADDRESS:0x0D) (POR:0x00)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRQ0RXS&lt;1:0&gt;</td>
<td>IRQ1RXS&lt;1:0&gt;</td>
<td>IRQ1TX</td>
<td>FIFOFULL</td>
<td>FIFOEMPTY</td>
<td>FOVRRUN</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7-6
IRQ0RXS<1:0>: IRQ0 Receive Stand-by bits
These bits control the IRQ0 source in Receive and Stand-by modes:

If DMODE1:DMODE0 = 00  ➔ Continuous Mode (default)
  11 = SYNC
  10 = SYNC
  01 = RSSI
  00 = Sync (default)

If DMODE1:DMODE0 = 01  ➔ Buffer Mode
  11 = SYNC
  10 = FIFOEMPTY(1)
  01 = WRITEBYTE
  00 = - (default)

If DMODE1:DMODE0 = 1x  ➔ Packet Mode
  11 = SYNC or ARDSMATCH(3) (if address filtering is enabled)
  10 = FIFOEMPTY(1)
  01 = WRITEBYTE
  00 = PLREADY(2) (default)

bit 5-4
IRQ1RXS<1:0>: IRQ1 Receive Stand-by bits
These bits control the IRQ1 source in Receive and Stand-by modes:

If DMODE1:DMODE0 = 00  ➔ Continuous Mode (default)
  xx = DCLK

If DMODE1:DMODE0 = 01  ➔ Buffer Mode
  11 = FIFO_THRESHOLD(1)
  10 = RSSI
  01 = FIFOFULL(1)
  00 = - (default)

If DMODE1:DMODE0 = 1x  ➔ Packet Mode
  11 = FIFO_THRESHOLD(1)
  10 = RSSI
  01 = FIFOFULL(1)
  00 = CRCOK (default)

Note 1: This mode is also available in Stand-by mode.
2: PLREADY = Payload ready
3: ARDSMATCH = Address Match
REGISTER 2-14:  FTXRXIREG: FIFO TRANSMIT AND RECEIVE INTERRUPT REQUEST CONFIGURATION REGISTER (ADDRESS:0x0D) (POR:0x00) (CONTINUED)

bit 3  IRQ1TX: Transmit IRQ1 bit
This bit selects IRQ1 as source in Transmit mode.

If DMODE1:DMODE0 = 00 ➔ Continuous Mode (default):
× = DCLK

If DMODE1:DMODE0 = 01 ➔ Buffer Mode or 1x ➔ Packet Mode:
1 = TXDONE
0 = FIFOFULL (default)

bit 2  FIFOFULL: FIFO Full bit
This bit indicates FIFO Full through the IRQ source
1 = FIFO full
0 = FIFO not full

bit 1  FIFOEMPTY: FIFO Empty bit
This bit indicates FIFO empty through the IRQ source
1 = FIFO not Empty
0 = FIFO Empty

bit 0  FOVRRUN: FIFO Overrun Clear bit
This bit indicates if FIFO overrun occurred.
1 = FIFO Overrun occurred
0 = No FIFO Overrun occurred
Writing a ’1’ for this bit clears flag and FIFO.

Note 1: This mode is also available in Stand-by mode.
2: PLREADY = Payload ready
3: ADRSMATCH = Address Match
### 2.15.2 FIFO TRANSMIT PLL AND RSSI INTERRUPT REQUEST CONFIGURATION REGISTER DETAILS

**REGISTER 2-15: FTPRIREG: FIFO TRANSMIT PLL AND RSSI INTERRUPT REQUEST CONFIGURATION REGISTER (ADDRESS: 0x0E) (POR: 0x01)**

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIFOFM: FIFO Filling Method bits</td>
<td>FIFOFSC: FIFO Filling Status or Control bits</td>
<td>TXDONE: Transmit Done bit</td>
<td>IRQ0TXST: Transmit Start with IRQ0 bit</td>
<td>Reserved: Reserved bit</td>
<td>RIRQS: RSSI IRQ Source</td>
</tr>
<tr>
<td>This bit decides the method of filling FIFO (supports Buffer mode only)</td>
<td>This bit indicates the status of FIFO filling and also controls the filling up of FIFO (supports Buffer Mode only)</td>
<td>This bit selects and IRQ source.</td>
<td>This bit indicates transmit start condition with IRQ0 as source.</td>
<td>Reserved</td>
<td>RSSI IRQ Source</td>
</tr>
<tr>
<td>1 = Manually controlled by FIFO fill</td>
<td>1 = Start filling the FIFO</td>
<td>1 = TXDONE (goes high when the last bit has left the shift register).</td>
<td>1 = Transmit starts if FIFO is not empty, IRQ0 mapped to FIFOEMPTY</td>
<td>1 = Set bit to '1' (required)(^1)</td>
<td>1 = Detected signal is above the value determined by the RTIVAL&lt;7:0&gt; bits (RSTHIREG&lt;7:0&gt;)</td>
</tr>
<tr>
<td>0 = Automatically starts when a sync word is detected (default)</td>
<td>0 = Stop filling the FIFO</td>
<td>0 = TX still in process</td>
<td>0 = Start transmission when the number of bytes in FIFO is greater than or equal to threshold set by the FTINT&lt;5:0&gt; bits (FIFOCREG&lt;5:0&gt;), IRQ0 mapped to FIFO_THRESHOLD</td>
<td>0 = Reserved (default)</td>
<td>0 = Detected signal is less than the value determined by the RTIVAL&lt;7:0&gt; bits (RSTHIREG&lt;7:0&gt;)</td>
</tr>
</tbody>
</table>

**Note 1:** Setting this bit to '0' disables the RSSI IRQ source. It can be left enabled at any time, and the user can choose to map this interrupt to IRQ0/IRQ1 or not.
REGISTER 2-15: FTPRIREG: FIFO TRANSMIT PLL AND RSSI INTERRUPT REQUEST CONFIGURATION REGISTER (ADDRESS:0x0E) (POR:0x01) (CONTINUED)

<table>
<thead>
<tr>
<th>bit 1</th>
<th>LSTSPLL: Lock Status of PLL bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PLL locked (lock detected)</td>
</tr>
<tr>
<td>0</td>
<td>PLL not locked</td>
</tr>
</tbody>
</table>

Writing a ‘1’ for this bit clears LSTSPLL.

<table>
<thead>
<tr>
<th>bit 0</th>
<th>LENPLL: Lock Enable of PLL bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PLL lock detect enabled (default)</td>
</tr>
<tr>
<td>0</td>
<td>PLL lock detect disabled</td>
</tr>
</tbody>
</table>

The PLL lock detect flag is mapped to the PLOCK pin (pin 23), and pin 23 is a High-Z pin.

Note 1: Setting this bit to ‘0’ disables the RSSI IRQ source. It can be left enabled at any time, and the user can choose to map this interrupt to IRQ0/IRQ1 or not.

2.15.3 RSSI THRESHOLD INTERRUPT REQUEST REGISTER DETAILS

REGISTER 2-16: RSTHIREG: RSSI THRESHOLD INTERRUPT REQUEST CONFIGURATION REGISTER (ADDRESS:0x0F) (POR:0x00)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>R</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
<td>R/W-0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown
- r = Reserved

bit 7-0 RTIVAL<7:0>: RSSI Threshold for Interrupt Value bits

These bits indicate the RSSI threshold value for interrupt request

RTIVAL<7:0> = 00000000 (default)
2.16 Receiver Configuration Registers

2.16.1 FILTER CONFIGURATION REGISTER DETAILS

REGISTER 2-17: FILCREG: FILTER CONFIGURATION REGISTER (ADDRESS:0x10) (POR:0xA3)

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \text{PASFILV&lt;3:0&gt;} )</td>
<td>( \text{BUTFILV&lt;3:0&gt;} )</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7-4 \( \text{PASFILV<3:0>} \): Passive Filter Value bits

These bits indicate the typical single sideband bandwidth of the passive low-pass filter.

- 1111 = 987 kHz
- 1110 = 676 kHz
- 1101 = 514 kHz
- 1100 = 458 kHz
- 1011 = 414 kHz
- 1010 = 378 kHz (default)
- 1001 = 321 kHz
- 1000 = 262 kHz
- 0111 = 234 kHz
- 0110 = 211 kHz
- 0101 = 184 kHz
- 0100 = 157 kHz
- 0011 = 137 kHz
- 0010 = 109 kHz
- 0001 = 82 kHz
- 0000 = 65 kHz

bit 3-0 \( \text{BUTFILV<3:0>} \): Butterworth Filter Value bits

These bits set the receiver bandwidth both in FSK and OOK mode.

\[
f_c = f_o + 200 \text{ kHz} \times \frac{f_{\text{xtal}} \text{MHz}}{12.8 \text{MHz}} \times \left(1 + \text{val(BUTFILV)}\right)\]

Where,

- \( f_c \) is the cut-off frequency
- \( f_o \) is the local oscillator frequency (center frequency)
- \( f_{\text{xtal}} \) is the crystal oscillator frequency

Note: \( f_c - f_o = 100 \text{ kHz} \) only when \( f_{\text{xtal}} = 12.8 \text{ MHz} \).
2.16.2 POLYPHASE FILTER CONFIGURATION REGISTER DETAILS

REGISTER 2-18: PFCREG: POLYPHASE FILTER CONFIGURATION REGISTER
(ADDRESS: 0x11) (POR: 0x38)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>r</th>
<th>r</th>
<th>r</th>
<th>r</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLCFV&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>bit 7-4</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLCFV&lt;3:0&gt;: Polyphase Centre Frequency Value bits</td>
<td></td>
</tr>
<tr>
<td>These bits indicate the center frequency of the polyphase filter (typically recommended to 100 kHz).</td>
<td></td>
</tr>
<tr>
<td>POLCFV&lt;3:0&gt; = 0011 → fo = 100 kHz (default)</td>
<td></td>
</tr>
<tr>
<td>fo = 200 kHz * (fxtal MHz) * (1 + val(POLCFV)) / 8</td>
<td></td>
</tr>
<tr>
<td>Where,</td>
<td></td>
</tr>
<tr>
<td>POLCFV &lt;3:0&gt; is the value in the register</td>
<td></td>
</tr>
<tr>
<td>fo is the cut-off frequency</td>
<td></td>
</tr>
<tr>
<td>fo is the local oscillator frequency (center frequency)</td>
<td></td>
</tr>
<tr>
<td>fxtal is the crystal oscillator frequency</td>
<td></td>
</tr>
</tbody>
</table>

bit 3-0 | Reserved<3:0>: Reserved bits; do not use |
| 1000 = Reserved (default) |
2.16.3  SYNC CONTROL REGISTER

DETAILS

REGISTER 2-19:  SYNCREG: SYNC CONTROL REGISTER (ADDRESS:0x12) (POR:0x18)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>r</th>
</tr>
</thead>
<tbody>
<tr>
<td>POLFilen</td>
<td>BSycnen</td>
<td>SYNcren</td>
<td>SYNCWSz&lt;1:0&gt;</td>
<td>SYNCten&lt;1:0&gt;</td>
<td></td>
<td></td>
<td>bit 7</td>
</tr>
<tr>
<td>bit 7 bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
-n = Value at POR  '1' = Bit is set  '0' = Bit is cleared  x = Bit is unknown
r = Reserved

bit 7  POLFilen: Polyphase Filter Enable bit
This bit enables the polyphase filter in OOK Receive mode.
1 = Polyphase filter enabled
0 = Polyphase filter disabled (default)

bit 6  BSycnen: Bit Synchronizer Enable bit
This bit controls the enabling and disabling of the bit synchronizer in Continuous receive mode.
1 = Bit Synchronizer disabled
0 = Bit Synchronizer enabled (default)

bit 5  SYNcren: SYNC Word Recognition Enable bit
1 = ON
0 = OFF (default)

bit 4-3  SYNCWSz<1:0>: SYNC Word Size bit
11 = 32 bits (default)
10 = 24 bits
01 = 16 bits
00 = 8 bits

bit 2-1  SYNCten<1:0>: SYNC Word Tolerated Error Numbers
These bits indicate the number of errors tolerated in the SYNC word recognition.
11 = 3 Errors
10 = 2 Errors
01 = 1 Errors
00 = 0 Errors (default)

bit 0  Reserved: Reserved bit; do not use
0 = Reserved (default)
### 2.16.4 RESERVED REGISTER DETAILS

REGISTER 2-20: RESVREG: RESERVED REGISTER (ADDRESS:0x13) (POR:0x07)

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>R = Readable bit</th>
<th>W = Writable bit</th>
<th>U = Unimplemented bit, read as '0'</th>
</tr>
</thead>
<tbody>
<tr>
<td>-n = Value at POR</td>
<td>'1' = Bit is set</td>
<td>'0' = Bit is cleared</td>
</tr>
<tr>
<td>r = Reserved</td>
<td></td>
<td>x = Bit is unknown</td>
</tr>
</tbody>
</table>

**bit 7-0**  
Reserved: Reserved bits; do not use  
00000111 = Reserved (default)

### 2.16.5 RSSI STATUS READ REGISTER DETAILS

REGISTER 2-21: RSTSREG: RSSI STATUS READ REGISTER\((1)\) (ADDRESS:0x14)

<table>
<thead>
<tr>
<th>bit 7</th>
<th>bit 6</th>
<th>bit 5</th>
<th>bit 4</th>
<th>bit 3</th>
<th>bit 2</th>
<th>bit 1</th>
<th>bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**bit 7-0**  
**RSSIVAL<7:0>:** RSSI Value bits  
These read-only bits indicate the RSSI output and each unit bit corresponds to 0.5 dB.

**Note 1:** POR is not applicable to this read-only register.
2.16.6 OOK CONFIGURATION REGISTER DETAILS

REGISTER 2-22: OOKCREG: OOK CONFIGURATION REGISTER (ADDRESS:0x15) (POR:0x00)

<table>
<thead>
<tr>
<th>Bit Position</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7-5</td>
</tr>
</tbody>
</table>

OOKTHSV<2:0>: OOK Threshold Step Value bits
These bits set the size of each decrement of the RSSI threshold in the OOK demodulator.

- 111 = 6.0 dB
- 110 = 5.0 dB
- 101 = 4.0 dB
- 100 = 3.0 dB
- 011 = 2.0 dB
- 010 = 1.5 dB
- 001 = 1.0 dB
- 000 = 0.5 dB (default)

OOKTHPV<2:0>: OOK Threshold Period Value bits
These bits set the period of decrement of the RSSI threshold in the OOK demodulator.

- 111 = 16 times in each chip period
- 110 = 8 times in each chip period
- 101 = 4 times in each chip period
- 100 = twice in each chip period
- 011 = once in each 8 chip periods
- 010 = once in each 4 chip periods
- 001 = once in each 2 chip periods
- 000 = once in each chip period (default)

OOKATHC<1:0>: OOK Average Threshold Cut-off bits
These bits set the cut-off frequency of the averaging for the average mode of the OOK threshold in the demodulator.

- 11 = f_c ~ BR/32.π
- 10 = Reserved; do not use
- 01 = Reserved; do not use
- 00 = f_c ~ BR/8.π (default)

Note 1: BR is the bit rate (for more information, refer to BRSREG (Register 2-22)).
2.17 Sync Word Configuration Registers

2.17.1 SYNC VALUE FIRST BYTE SET

REGISTER DETAILS

REGISTER 2-23: SYNCV31REG: SYNC VALUE FIRST BYTE CONFIGURATION REGISTER
(ADDRESS:0x16) (POR:0x00)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>bit 6</td>
<td>bit 5</td>
<td>bit 4</td>
<td>bit 3</td>
<td>bit 2</td>
<td>bit 1</td>
<td>bit 0</td>
</tr>
</tbody>
</table>

SYNCV<31:24>

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown
r = Reserved

bit 7-0  

**SYNCV<31:24>:** SYNC First Byte Value bits
These bits are to be set to configure the first byte of the SYNC word.
**SYNCV<31:24> = 00000000** (default)

2.17.2 SYNC VALUE SECOND BYTE SET

REGISTER DETAILS

REGISTER 2-24: SYNCV23REG: SYNC VALUE SECOND BYTE CONFIGURATION REGISTER
(ADDRESS:0x17) (POR:0x00)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>bit 6</td>
<td>bit 5</td>
<td>bit 4</td>
<td>bit 3</td>
<td>bit 2</td>
<td>bit 1</td>
<td>bit 0</td>
</tr>
</tbody>
</table>

SYNCV<23:16>

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown
r = Reserved

bit 7-0  

**SYNCV<23:16>:** SYNC Second Byte Value bits
These bits are to be set to configure the second byte of the SYNC word.
**SYNCV<23:16> = 00000000** (default)
2.17.3  SYNC VALUE THIRD BYTE SET
REGISTER DETAILS

REGISTER 2-25:  SYNCV15REG: SYNC VALUE THIRD BYTE CONFIGURATION REGISTER
(ADDRESS:0x138) (POR:0x00)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
-n = Value at POR  '1' = Bit is set  '0' = Bit is cleared  x = Bit is unknown
r = Reserved

SYNCV<15:8>: SYNC Third Byte Value bits
These bits are to be set to configure the third byte of the SYNC word.
SYNCV<15:8> = 00000000 (default)

2.17.4  SYNC VALUE FOURTH BYTE SET
REGISTER DETAILS

REGISTER 2-26:  SYNCV07REG: SYNC VALUE FOURTH BYTE CONFIGURATION REGISTER
(ADDRESS:0x19) (POR:0x00)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

R = Readable bit  W = Writable bit  U = Unimplemented bit, read as '0'
-n = Value at POR  '1' = Bit is set  '0' = Bit is cleared  x = Bit is unknown
r = Reserved

SYNCV<7:0>: SYNC Fourth Byte Value bits
These bits are to be set to configure the fourth byte of the SYNC word.
SYNCV<7:0> = 00000000 (default)
2.18 Transmitter Configuration Registers

2.18.1 TRANSMIT PARAMETER CONFIGURATION REGISTER DETAILS

REGISTER 2-27: TXCONREG: TRANSMIT PARAMETER CONFIGURATION REGISTER (ADDRESS:0x1A) (POR:0x7C)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>r</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7

TXIPOLFV<3:0>: Transmission Interpolation Filter Cut Off Frequency Value bits
These bits control the cut-off frequency \( f_c \) of the interpolation filter in the transmission path. \( f_c = 200 \text{ kHz} \) (default)

\[
f_c = 200 \text{ kHz} \times \left( \frac{f_{\text{statMHz}}}{12.8 \text{MHz}} \right) \times \left( \frac{\text{val}(\text{TXIPOLFV})}{8} \right)
\]

Where,
TXIPOLFV <3:0> is the value in the register
\( f_c \) is the cut-off frequency
\( f_{\text{stat}} \) is the local oscillator frequency (center frequency)
\( f_{\text{stat}} \) is the crystal oscillator frequency

bit 3-1
TXOPVAL<2:0>: Transmit Output Power Value bits (1 step ≈ 3dB)
111 = -8 dBm
110 = -5 dBm
101 = -2 dBm
100 = 1 dBm
011 = 4 dBm
010 = 7 dBm
001 = 10 dBm (default)
000 = 13 dBm

bit 0
Reserved: Reserved bit; do not use
0 = Reserved (default)
### 2.19 Oscillator Configuration Registers

#### 2.19.1 CLOCK OUTPUT CONTROL REGISTER DETAILS

**REGISTER 2-28: CLKOUTREG: CLOCK OUTPUT CONTROL REGISTER**

*(ADDRESS:0x1B) (POR:0xBC)*

<table>
<thead>
<tr>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>R/W-1</th>
<th>r</th>
<th>r</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKOCNTRL</td>
<td>CLKFREQ&lt;4:0&gt;</td>
<td>—</td>
<td>—</td>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
</tr>
</tbody>
</table>

**bit 7**  
**CLKOCNTRL:** Clock Output Control bit  
This bit enables the Clock Output from the transceiver.  
1 = Enabled (default), Clock frequency set by Clkout_freq (default)  
0 = Disabled

**bit 6-2**  
**CLKOFREQ<4:0>:** Clock Out Frequency bits  
These bits indicate value of the frequency of the Clock output.  

\[
\text{CLKOFREQ<4:0>} = \begin{cases} 
01111 & \Rightarrow f_{\text{clkout}} = 427 \text{ kHz (default)} \\
00000 & \text{or} \\
\frac{f_{\text{clkout}}}{2 \cdot \text{CLKOFREQ}}, & \text{for } \text{CLKOFREQ<4:0>} \neq 00000 
\end{cases}
\]

Where,  
\[f_{\text{clkout}}\] is the output frequency  
\[f_0\] is the local oscillator frequency  
\[f_{\text{xtal}}\] is the crystal oscillator frequency

**bit 1-0**  
**Reserved<1:0>:** Reserved bits; do not use  
00 = Reserved (default)
### 2.20 Packet Configuration Registers

#### 2.20.1 PAYLOAD CONFIGURATION REGISTER DETAILS

**REGISTER 2-29: PLOADREG: PAYLOAD CONFIGURATION REGISTER**

*(ADDRESS:0x1C) (POR:0x00)*

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCHSTREN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**REGISTER 2-30: NADDSREG: NODE ADDRESS SET REGISTER**

*(ADDRESS:0x1D) (POR:0x00)*

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>NLADDR&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bit 7**
- **MCHSTREN**: Manchester Encoding/Decoding Enable bit
  - 1 = Enabled
  - 0 = Disabled (default)

**Bit 6-0**
- **PLDPLEN<6:0>**: Payload Packet Length bits
  - These bits indicate payload packet length. If Pkt_format = 0, payload length. If Pkt_format = 1, max length in RX, not used in TX.
  - PLDPLEN<6:0> = 000000 (default)

**Bit 7-0**
- **NLADDR<7:0>**: Node Local Address bits
  - These bits are to be set to configure the Node Local Address for filtering of received packets.
  - NLADDR<7:0> = 00h (default)
2.20.3 PACKET CONFIGURATION
REGISTER DETAILS

REGISTER 2-31: PKTCREG: PACKET CONFIGURATION REGISTER
(ADDRESS:0x1E) (POR:0x48)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-1</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R/W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>PKTLENF</td>
<td>PRESIZE&lt;1:0&gt;</td>
<td>WHITEON</td>
<td>CHKCRCEN</td>
<td>ADDFIL&lt;1:0&gt;</td>
<td>STSCRCEN</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 7 PKTLENF: Packet Length Format bit
1 = Variable Length Format
0 = Fixed Length Format (default)

bit 6-5 PRESIZE<1:0>: Preamble Size bits
These bits indicate the size of the preamble bits to be transmitted.
11 = 4 bytes
10 = 3 bytes (default)
01 = 2 bytes
00 = 1 byte

bit 4 WHITEON: Whitening/Dewhitenhing Process Enable bit
1 = ON
0 = OFF (default)

bit 3 CHKCRCEN: Check (or Calculation) CRC Enable bit
1 = ON (default)
0 = OFF

bit 2-1 ADDFIL<1:0>: Address Filtering bits
These bits determine the mode of filter out the addresses of received packet
11 = Node Address & 0x00 & 0xFF Accepted; otherwise, rejected
10 = Node Address & 0x00 Accepted; otherwise, rejected
01 = Node Address Accepted; otherwise, rejected
00 = OFF (default)

bit 0 STSCRCEN: Status Check CRC Enable bit
This bit checks the status/result of the CRC of the current packet (read-only).
1 = OK
0 = Not OK
## FIFO CRC CONFIGURATION REGISTER DETAILS

### REGISTER 2-32: FCRCREG: FIFO CRC CONFIGURATION REGISTER

(ADDRESS:0x1F) (POR:0x00)

<table>
<thead>
<tr>
<th>R/W-0</th>
<th>R/W-0</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACFCRC</td>
<td>FRWAXS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

* R = Readable bit  
  W = Writable bit  
  U = Unimplemented bit, read as '0'
  -n = Value at POR
  '1' = Bit is set  
  '0' = Bit is cleared  
  x = Bit is unknown
  r = Reserved

**bit 7**  
**ACFCRC**: Auto Clear FIFO CRC bit  
This bit when enabled auto clears FIFO if CRC failed for the current packet.  
1 = Disabled  
0 = Enabled (default)

**bit 6**  
**FRWAXS**: FIFO Read/Write Access bit  
This bit indicate the read/write access for FIFO in Stand-by mode.  
1 = Read  
0 = Write (default)

**bit 5-0**  
**Reserved<5:0>**: Reserved bits; do not use  
00000 = Reserved (default)
### TABLE 2-8: CONFIGURATION/CONTROL/STATUS REGISTER MAP

<table>
<thead>
<tr>
<th>Register Function/Parameter Type</th>
<th>Register Address</th>
<th>Register Name</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>General</strong></td>
<td>0x00</td>
<td>GCONREG</td>
<td>CMOD&lt;2:0&gt;</td>
<td></td>
<td></td>
<td>FBS&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RPS 0x28</td>
</tr>
<tr>
<td></td>
<td>0x01</td>
<td>DMODREG</td>
<td>MODSEL&lt;1:0&gt;</td>
<td>DMODE0</td>
<td>OOKTYP&lt;1:0&gt;</td>
<td>DMODE1</td>
<td>IFGAIN&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>0x88</td>
</tr>
<tr>
<td></td>
<td>0x02</td>
<td>FDEVREG</td>
<td></td>
<td>FDVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x03</td>
</tr>
<tr>
<td></td>
<td>0x03</td>
<td>BRSREG</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x07</td>
</tr>
<tr>
<td></td>
<td>0x04</td>
<td>FLTHREG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0C</td>
</tr>
<tr>
<td></td>
<td>0x05</td>
<td>FIFOCREG</td>
<td>FSIZE&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0F</td>
</tr>
<tr>
<td></td>
<td>0x06</td>
<td>R1CREG</td>
<td>R1CVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x77</td>
</tr>
<tr>
<td></td>
<td>0x07</td>
<td>P1CREG</td>
<td>P1CVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x64</td>
</tr>
<tr>
<td></td>
<td>0x08</td>
<td>S1CREG</td>
<td>S1CVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x32</td>
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<tr>
<td></td>
<td>0x09</td>
<td>R2CREG</td>
<td>R2CVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td>0x74</td>
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<tr>
<td></td>
<td>0x0A</td>
<td>P2CREG</td>
<td>P2CVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x62</td>
</tr>
<tr>
<td></td>
<td>0x0B</td>
<td>S2CREG</td>
<td>S2CVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x32</td>
</tr>
<tr>
<td></td>
<td>0x0C</td>
<td>PACREG</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>_WRITE</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>0x38</td>
</tr>
<tr>
<td></td>
<td>0x0D</td>
<td>FTXRXIREG</td>
<td>IRQ0RXS&lt;1:0&gt;</td>
<td>IRQ1RXS&lt;1:0&gt;</td>
<td>IRQ1TX</td>
<td>FIFOFULL</td>
<td>FIFOEMPTY</td>
<td>FOVRRUN</td>
<td></td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td><strong>Interrupt</strong></td>
<td>0x0E</td>
<td>FTPRIREG</td>
<td>FIFOFM</td>
<td>FIFOFC</td>
<td>TXDONE</td>
<td>IRQ0TXST</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td>0x01</td>
</tr>
<tr>
<td></td>
<td>0x0F</td>
<td>RSTHIREG</td>
<td>RTIVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td></td>
<td>0x10</td>
<td>FILCREG</td>
<td>PASFILV&lt;3:0&gt;</td>
<td></td>
<td></td>
<td>Reserved</td>
<td>BUTFILV&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td>0xA3</td>
</tr>
<tr>
<td><strong>Receiver</strong></td>
<td>0x11</td>
<td>PFCREG</td>
<td>POLCFV&lt;3:0&gt;</td>
<td></td>
<td></td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td></td>
<td>0x38</td>
</tr>
<tr>
<td></td>
<td>0x12</td>
<td>SYNCREG</td>
<td>POLFLEN</td>
<td>BSYNCE</td>
<td>SYNCREN</td>
<td>SYNCWSZ&lt;1:0&gt;</td>
<td>SYNCTEN&lt;1:0&gt;</td>
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<td>0x18</td>
</tr>
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<td></td>
<td>0x13</td>
<td>RESVREG</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td>0x07</td>
</tr>
<tr>
<td></td>
<td>0x14</td>
<td>RSTSREG</td>
<td>RSSIVAL&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Read-only</td>
</tr>
<tr>
<td></td>
<td>0x15</td>
<td>OOKCREG</td>
<td>OOKTHSV&lt;2:0&gt;</td>
<td>OOKTHPV&lt;2:0&gt;</td>
<td>OOKATHC&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td><strong>SYNC Word</strong></td>
<td>0x16</td>
<td>SYNCV31REG</td>
<td>SYNCV&lt;31:24&gt;</td>
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<td></td>
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<td>0x60</td>
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<td></td>
<td>0x17</td>
<td>SYNCV23REG</td>
<td>SYNCV&lt;23:16&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td></td>
<td>0x18</td>
<td>SYNCV15REG</td>
<td>SYNCV&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td></td>
<td>0x19</td>
<td>SYNCV07REG</td>
<td>SYNCV&lt;7:0&gt;</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td>0x00</td>
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<tr>
<td><strong>Transmitter</strong></td>
<td>0x1A</td>
<td>TXCONREG</td>
<td>TXIPOLFV&lt;3:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reserved 0x7C</td>
</tr>
<tr>
<td></td>
<td>0x1B</td>
<td>CLKOUTREG</td>
<td>CLKCNTRL</td>
<td>CLKOFREQ&lt;4:0&gt;</td>
<td>PLDPLEN&lt;6:0&gt;</td>
<td></td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td>0xBC</td>
</tr>
<tr>
<td><strong>Packet</strong></td>
<td>0x1C</td>
<td>PLOADREG</td>
<td>MCHSTREN</td>
<td></td>
<td></td>
<td>PLDPLEN&lt;6:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x00</td>
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<tr>
<td></td>
<td>0x1D</td>
<td>NADDSREG</td>
<td>NLADDR&lt;7:0&gt;</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x00</td>
</tr>
<tr>
<td></td>
<td>0x1E</td>
<td>PKTCREG</td>
<td>PKTLENF</td>
<td>PRESIZE&lt;1:0&gt;</td>
<td>WHITEON</td>
<td>CHKCRCLEN</td>
<td>ADDFIL&lt;1:0&gt;</td>
<td>STSCRNC</td>
<td></td>
<td></td>
<td>0x48</td>
</tr>
<tr>
<td></td>
<td>0x1F</td>
<td>FCRCREG</td>
<td>ACFCRC</td>
<td>FRWAXS</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td></td>
<td></td>
<td>0x00</td>
</tr>
</tbody>
</table>
3.0 FUNCTIONAL DESCRIPTION

The functional block diagram of the MRF89XA is illustrated in Figure 3-1. The functional operations of individual blocks are explained in subsequent sections.

FIGURE 3-1: MRF89XA FUNCTIONAL BLOCK DIAGRAM
3.1 Reset of the Chip

A power-on Reset of the MRF89XA is triggered at power up. Additionally, a manual reset can be issued by controlling the TEST8 pin (pin 13).

3.1.1 POWER-ON RESET (POR)

If the application requires the disconnection of VDD from the MRF89XA, the user should wait for 10 ms from the end of the POR cycle before commencing communications using SPI. The TEST8 pin should be left floating during the POR sequence. Figure 3-2 illustrates the POR Timing.

**Note:** Any CLKOUT-related activity can also be used to detect that the chip is ready.

3.1.2 MANUAL RESET

A manual reset of the MRF89XA is possible even for applications in which VDD cannot be physically disconnected. The TEST8 pin should be pulled high for 100 µs and then released. The user should then wait 5 ms before using the chip. The pin is driven with an open-drain output, and therefore, is pulled high while the device is in POR. Figure 3-3 illustrates the Manual Reset Timing.

**Note:** When the TEST8 pin is driven high, an current consumption of up to 10 mA can be seen on Vdd.

---

**FIGURE 3-2: POR TIMING DIAGRAM**

![POR Timing Diagram](image1.png)

**FIGURE 3-3: MANUAL RESET TIMING DIAGRAM**

![Manual Reset Timing Diagram](image2.png)
3.2 Frequency Synthesis Description

3.2.1 REFERENCE OSCILLATOR

The crystal oscillator (XTAL) forms the reference oscillator of an Integer-N PLL. The crystal reference frequency and the software controlled dividers R, P, and S determine the output frequency of the PLL. The guidelines for selecting the appropriate crystal with specifications are explained in Section 4.6, Crystal Specification and Selection Guidelines.

3.2.2 BUFFERED CLOCK OUTPUT

The buffered clock output is a signal derived from \( f_{\text{xtal}} \). It can be used as a reference clock (or a sub-multiple of it) for the host microcontroller and is an output on the CLKOUT pin (pin 19). The pin is activated using the CLKOCNTRL bit (CLKOUTREG<7>). The output frequency (CLKOUT) division ratio is programmed through the Clock Out Frequency bits (CLKOFREQ5-CLKOFREQ1) in the Clock Output Control Register (CLKOUTREG<6:2>). The two uses of the CLKOUT output are:

- To provide a clock output for a host microcontroller, thus saving the cost of an additional oscillator. CLKOUT can be made available in any operation mode, except Sleep mode, and is automatically enabled at power-up.
- To provide an oscillator reference output. Measurement of the CLKOUT signal enables simple software trimming of the initial crystal tolerance.

3.2.3 CLOCK REGISTERS

The registers associated with the Clock and its control are:

- GCONREG (Register 2-1)
- CLKOUTREG (Register 2-28).

3.2.4 PHASE-LOCKED LOOP (PLL)

The frequency synthesizer of the MRF89XA is a fully integrated integer-N type PLL. The PLL circuit requires only five external components for the PLL loop filter and the VCO tank circuit.

3.2.5 PLL REGISTERS

The registers associated with the PLL are:

- GCONREG (Register 2-1)
- FTPRIREG (Register 2-15).

3.2.6 SW SETTINGS OF THE VCO

To guarantee the optimum operation of the VCO over the MRF89XA's frequency and temperature ranges, the settings listed in Table 3-1 should be programmed into the MRF89XA.
TABLE 3-1: FREQUENCY BAND SETTING

<table>
<thead>
<tr>
<th>Target Channel (MHz)</th>
<th>FBS1</th>
<th>FBS0</th>
</tr>
</thead>
<tbody>
<tr>
<td>863-870</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>902-915</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>915-928</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>950-960</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

3.2.6.1 Trimming the VCO Tank by Hardware and Software

To ensure that the frequency band of operation may be accurately addressed by the R, P, and S dividers of the synthesizer, it is necessary to ensure that the VCO is correctly centered. The MRF89XA built-in VCO trimming feature makes it easy and is controlled by the SPI interface. This tuning does not require any RF test equipment, and can be achieved by measuring Vtune, the voltage between the PLLN and PLLP pins (6 and 7 pins).

The VCO is centered if the voltage is within the range of 50 \( \leq V_{tune} (mV) \leq 150 \).

This measurement should be conducted when in Transmit mode at the center frequency (fo) of the desired band (for example, approximately 867 MHz in the 863-870 MHz band), with the appropriate frequency band setting using the (FBS<1:0> bits (GCONREG<4:3>).

If this inequality is not satisfied, adjust the VCOT<1:0> bits (GCONREG<2:0>) from '00' by monitoring Vtune. This allows the VCO voltage to be trimmed in +60 mV increments. If the desired voltage range is inaccessible, the voltage may be adjusted further by changing the tank circuit inductance value.

An increase in inductance results in an increase Vtune. In addition, for mass production, the VCO capacitance is piece-to-piece dependant. As such, the optimization proposed above should be verified on several prototypes, to ensure that the population is centered with 100 mV.

The register associated with VCO is:
• GCONREG (Register 2-1).

3.2.7 FREQUENCY CALCULATION

As illustrated in Figure 2-5, the PLL structure comprises three different dividers, R, P, and S, which set the output frequency through the LO. A second set of dividers is also available to allow rapid switching between a pair of frequencies: R1/P1/S1 and R2/P2/ S2. These six dividers are programmed by six independent registers (see Register 2-7 through Register 2-12), which are selected by GCONREG.

FSK Mode

The formula provided in Equation 3-1 gives the relationship between the local oscillator, and R, P and S values, when using FSK modulation.

**EQUATION 3-1:**

\[
f_{rf, fsk} = \frac{9}{8} \times f_{lo} \left[ P \times \left( \frac{1}{R1} + \frac{1}{R2} \right) + S \right]
\]

3.2.8 FSK MODE REGISTERS

The registers associated with FSK mode are:
• GCONREG (Register 2-1)
• DMODREG (Register 2-2).

OOK Mode

Due to the manner in which the baseband OOK symbols are generated, the signal is always offset by the FSK frequency deviation (FDVAL<7:0> as programmed in FDEVREG<7:0>). Therefore, the center of the transmitted OOK signal is represented by Equation 3-2.

**EQUATION 3-2:**

\[
f_{rf, ook, tx} = \frac{9}{8} \times f_{lo} - f_{dev}
\]

Consequently, in Receive mode, due to the low intermediate frequency (Low-IF) architecture of the MRF89XA, the frequency should be configured so as to ensure the correct low-IF receiver baseband center frequency, IF2, as shown in Equation 3-3.

**EQUATION 3-3:**

\[
f_{rf, ook, rx} = \frac{9}{8} \times f_{lo} - IF2
\]

As described in Section 3.4.4, Channel Filters, it is recommended that IF2 be set to 100 kHz.

3.2.9 OOK MODE REGISTERS

The registers associated with OOK mode are:
• GCONREG (Register 2-1)
• DMODREG (Register 2-2)
• FLTHREG (Register 2-5)
• OOKCREG (Register 2-22)
3.3 Transmitter

The MRF89XA is set to Transmit mode when the CMOD<2:0> bits (GCONREG<7:5>) are set to ‘100’ (see Register 2-1).

The transmitter chain in the MRF89XA is based on the same double-conversion architecture and uses the same intermediate frequencies as the receiver chain.

3.3.1 BIT RATE SETTING

In Continuous Transmit mode, setting the bit rate through the BRVAL<6:0> bits (BRSREG<6:0>) is useful to determine the frequency of DCLK. As explained in Section 3.9.1, TX Processing, DCLK will trigger an interrupt on the host microcontroller each time a new bit has to be transmitted, as shown in Equation 3-4.

EQUATION 3-4:

\[
BR = \frac{f_{\text{xdal}}}{64 \times (1 + \text{val(BRVAL<6:0>))}}
\]

3.3.2 ALTERNATIVE SETTINGS

Bit rate, frequency deviation, and TX interpolation filter settings are a function of the crystal frequency \(f_{\text{xtal}}\) of the reference oscillator. Settings other than those programmed with a 12.8 MHz crystal can be obtained by selecting the correct reference oscillator frequency.

3.3.3 \(f_{\text{dev}}\) SETTING IN FSK MODE

The frequency deviation, \(f_{\text{dev}}\), of the FSK transmitter is programmed through the FDVAL<7:0> bits (FDEVREG<7:0>), as shown in Equation 3-5.

EQUATION 3-5:

\[
f_{\text{dev}} = \frac{f_{\text{xtal}}}{32 \times (1 + \text{val(FDVAL<7:0>))}}
\]

For correct operation, the modulation index \(\beta\) should be equal to Equation 3-6.

EQUATION 3-6:

\[
\beta = \frac{2 \times f_{\text{dev}}}{BRVAL} \geq 2
\]

3.3.4 \(f_{\text{dev}}\) SETTING IN OOK MODE

\(f_{\text{dev}}\) has no physical meaning in OOK Transmit mode. However, due to the DDS baseband signal generation, the OOK signal is always offset by \(f_{\text{dev}}\) (see Section 3.2.7, Frequency Calculation). It is suggested that \(f_{\text{dev}}\) retains its default value of 100 kHz in OOK mode.

3.3.5 INTERPOLATION FILTER

After digital-to-analog conversion, the I and Q signals are smoothened by interpolation filters. Low-pass filters in this block digitally generates the signal and prevent the alias signals from entering the modulators. Its bandwidth can be programmed with the (TXIPOLFV<6:0> bits (TXPARCREG<7:1), and should be calculated as shown in Equation 3-7.

EQUATION 3-7:

\[
BW = 3 \times \left[ f_{\text{dev}} + \frac{BR}{2} \right]
\]

Where,

\(f_{\text{dev}}\) is the programmed frequency deviation as set in FDEVREG

\(BR\) is the physical bit rate of transmission

Note: Low interpolation filter bandwidth will attenuate the baseband I/Q signals, thus reducing the power of the FSK signal. Conversely, excessive bandwidth will degrade spectral purity.

For most of the applications a BW of around 125 KHz would be acceptable, but for wideband FSK modulation, the recommended filter setting cannot be reached. However, the impact on spectral purity will be negligible due to the existing wideband channel.
3.3.6 POWER AMPLIFIER

3.3.6.1 Rise and Fall Time Control

In OOK mode, the PA ramp times can be accurately controlled through the PARC<1:0> bits (PACONREG<4:3>). These bits directly control the slew rate of the PARS pin.

<table>
<thead>
<tr>
<th>PARC&lt;1:0&gt;</th>
<th>$t_{\text{PARS}}$ (µs)</th>
<th>$t_{\text{PAOUT}}$ (rise / fall)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>3</td>
<td>2.5 / 2 µs</td>
</tr>
<tr>
<td>01</td>
<td>8.5</td>
<td>5 / 3 µs</td>
</tr>
<tr>
<td>10</td>
<td>15</td>
<td>10 / 6 µs</td>
</tr>
<tr>
<td>11</td>
<td>23</td>
<td>20 / 10 µs</td>
</tr>
</tbody>
</table>

TABLE 3-2: POWER AMPLIFIER RISE/FALL TIMES

3.3.7 TRANSMIT MODE REGISTERS

The registers associated with Transmit mode are:

- GCONREG (Register 2-1)
- DMODREG (Register 2-2)
- FDEVREG (Register 2-3)
- BRSREG (Register 2-4)
- R1CREG (Register 2-7)
- P1CREG (Register 2-8)
- S1CREG (Register 2-9)
- R2CREG (Register 2-10)
- P2CREG (Register 2-11)
- S2CREG (Register 2-12)
- PACREG (Register 2-13)
- FTXRXIREG (Register 2-14)
- FTPRIREG (Register 2-15)

During the Transmit mode of MRF89XA, the Shift register takes bytes from the FIFO and outputs them serially (MSb first) at the programmed bit rate to the modulator. When the transmitter is enabled, it starts sending out data from the Shift register with respect to the set bit rate. After power-up and with the Transmit registers enabled, the transmitter preloads the FIFO with preambles before sending the actual data based on the mode of operation. Figure 3-4 illustrates the PA Control Timing.
### 3.4 Receiver

The MRF89XA is set to Receive mode when the CMOD<2:0> bits (GCONREG<7:5>) are set to '011' (see Register 2-1).

The receiver is based on the superheterodyne architecture. (In super heterodyne architecture you need to use a saw filter to give better image rejection). The front-end is composed of an LNA and a mixer whose gains are constant. The mixer down-converts the RF signal to an intermediate frequency, which is equal to one-eighth of the LO frequency, which in turn is equal to eight-ninths of the RF frequency. Behind this first mixer there is a variable gain IF amplifier that can be programmed from maximum gain of 13.5-0 dB in steps of 4.5 dB by altering the IFGAIN<1:0> bits (DMODREG<1:0>).

After the variable gain IF amplifier, the signal is down-converted into two I and Q base-band signals by two quadrature mixers that are fed by reference signals at one-eighth the LO frequency. These I and Q signals are then filtered and amplified before demodulation.

The first filter is a second-order passive R-C filter whose bandwidth can be programmed to 16 values with the PASFILV<3:0> bits (FILCREG<7:4>). The second filter can be configured as either a third-order Butterworth active filter, which acts as a low-pass filter for the zero-IF FSK configuration, or as a polyphase band-pass filter for the low-IF OOK configuration. To select Butterworth low-pass filter operation, the POLFILLEN bit (SYNCREG<7>) is set to '0'. The bandwidth of the Butterworth filter can be programmed to 16 values by configuring the BUTFILV<3:0> bits (FILCREG<3:0>). The low-IF configuration must be used for OOK modulation. This configuration is enabled when the POLFILLEN bit (SYNCREG<7>) is set to ‘1’. The center frequency (fo) of the polyphase filter can be programmed to 16 values by setting the POLCFV<3:0> bits (PFCREG<7:4>). The bandwidth of the filter can be programmed by configuring the BUTFILV<3:0> bits (FILCREG<3:0>). In OOK mode, the value of the low-IF is equal to the deviation frequency defined in FDEVREG.

In addition to the channel filtering, the function of the polyphase filter is to reject the image. Figure 3-5 illustrates the two configurations of the second IF filter. In the Butterworth configuration, FcBW is the 3 dB cut-off frequency. In the polyphase band-pass configuration, FOPP is the center frequency given by the POLCFV<3:0> bits (PFCREG<7:4>), and FCPP is the upper 3 dB bandwidth of the filter whose offset, referenced to FOPP, is given by BUTFILV<3:0> bits (FILCREG<3:0>).

#### 3.4.1 MRF89XA SECOND IF FILTER DETAILS

**FIGURE 3-5: IF FILTERS IN FSK AND OOK MODES**

After filtering, the I and Q signals are each amplified by a chain of 11 amplifiers having 6 dB of gain each. The outputs of these amplifiers and their intermediate 3 dB nodes are used to evaluate the received signal strength (RSSI). Limiters are located behind the 11 amplifiers of the I and Q chains and the signals at the output of these limiters are used by the FSK demodulator. The RSSI output is used by the OOK demodulator. The global bandwidth of the entire base-band chain is given by the bandwidths of the passive filter, the Butterworth filter, the amplifier chain, and the limiter. The maximum achievable global bandwidth when the bandwidths of the first three blocks are programmed at their upper limit is approximately 350 kHz.

#### 3.4.2 LNA AND FIRST MIXER

In Receive mode, the RFIO pin is connected to a fixed gain, common-gate, Low Noise Amplifier (LNA). The performance of this amplifier is such that the Noise Figure (NF) of the receiver is estimated to be approximately 7 dB.

#### 3.4.3 IF GAIN AND SECOND I/Q MIXER

Following the LNA and first down-conversion, there is an IF amplifier whose gain can be programmed from -13.5-0 dB in 4.5 dB steps, through the IFGAIN<1:0> bits (DMODREG<1:0>). The default setting corresponds to 0 dB gain, but lower values can be used to increase the RSSI dynamic range. For more information, refer Section 3.4.7, received signal strength (RSSI).
3.4.4 CHANNEL FILTERS
The second mixer stages are followed by the channel select filters. The channel select filters have a strong influence on the noise bandwidth and selectivity of the receiver and hence its sensitivity. Each filter comprises a passive and an active section.

3.4.4.1 Passive Filter
Each channel select filter features a passive second-order RC filter, with a bandwidth programmable through the PASFILV<3:0> bits (FILCREG<7:4>). As the wider of the two filters, its effect on the sensitivity is negligible, but its bandwidth must be set up to optimize blocking immunity. The value entered into this register sets the single side bandwidth of this filter. For optimum performance it should be set to three to four times the cut-off frequency (fc) of the active Butterworth (or Polyphase) filter described in Section 3.4.4.2, Active Filter, and as shown in Equation 3-8.

\[
3\times f_{\text{ButterFilter}} \leq B_{\text{passive,filter}} \leq 4\times f_{\text{ButterFilter}}
\]

3.4.4.2 Active Filter
The “fine” channel selection is performed by an active, third-order, Butterworth filter, which acts as a low-pass filter for the zero-IF configuration (FSK), or a complex Polyphase filter for the low-IF (OOK) configuration. The POLFILEN bit (SYNCREG<7>) enables or disables the Polyphase filter.

Figure 3-6 illustrates the required bandwidth of this filter that varies between the two demodulation modes.

**FIGURE 3-6: ACTIVE CHANNEL FILTER DESCRIPTION**

FSK mode: The 99% energy bandwidth of an FSK modulated signal is approximated, as shown in Equation 3-9.

\[
BW_{99\%,\text{fsk}} = 2\times\left[f_{\text{dev}} + \frac{BR}{2}\right]
\]

The BUTFILV<3:0> bits from FILCREG set co the cut-off frequency (fc) of the filter. In a zero-IF configuration, the FSK lobes are centered on the virtual “DC” frequency. The choice of co should be such that the modulated signal falls in the filter bandwidth, anticipating the Local Oscillator frequency drift over the operating temperature and aging of the device as shown in Equation 3-10.

\[
2\times f_c > BW_{99\%,\text{fsk}} + LO_{\text{drifts}}
\]

Figure 3-11 illustrates an accurate overview of the filter bandwidth vs. setting.

OOK mode: The 99% energy bandwidth of an OOK modulated signal is approximated, as shown in Equation 3-11.

\[
BW_{99\%,\text{ook}} = \frac{2}{t_{\text{bit}}} = 2\times BR
\]
The POLCFV<3:0> bits (PFCREG<7:4>) set $f_o$, the center frequency of the polyphase filter when activated. $f_o$ should always be chosen to be equal to the low Intermediate Frequency of the receiver (IF2). Because low IF frequency of the OOK receiver denoted by IF2 can always be replaced by $f_o$ for any calculations or monitoring purposes.

The following setting is recommended:

- $f_o = 100$ kHz
- POLCFV<3:0> = 0011.

The value stored as BUTFILV<3:0> bits (FILCREG<3:0>) determines $f_c$, the filter cut-off frequency. Therefore, $f_c$ should be set according to Equation 3-12.

**EQUATION 3-12:**

$$2*(f_c - f_o) > BW_{99\%\_ook} + LO_{drifts}$$

Where,

- $f_c$ is the cut-off frequency
- $f_o$ is the center frequency

Again, $f_c$ as a function of the BUTFILV<3:0> bits, is described in Section 3.4.6, Channel Filters Setting in OOK Mode.

### 3.4.5 CHANNEL FILTERS SETTING IN FSK MODE

$f_c$, the 3dB cut-off frequency of the Butterworth filter used in FSK reception, is programmed through the BUTFILV<3:0> bits (FILCREG<3:0>). However, the entire receiver chain influences this cut-off frequency. The channel select and resultant filter bandwidths are illustrated in Figure 3-7.

Table 4-2 suggests filter settings in FSK mode along with the corresponding passive filter bandwidth and the accepted tolerance on the crystal reference.

**FIGURE 3-7: ACTUAL BW OF BUTTERWORTH FILTER**

![Butterworth Filter BW, FSK](image)

- Actual
- Theoretical
- BW

**TABLE 4-2**

<table>
<thead>
<tr>
<th>Val BUTFILV&lt;3:0&gt; [d]</th>
<th>Butterworth Filter BW, FSK</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-2</td>
<td>Actual BW</td>
</tr>
<tr>
<td>3-4</td>
<td>Theoretical BW</td>
</tr>
<tr>
<td>5-6</td>
<td>BW</td>
</tr>
<tr>
<td>7-8</td>
<td></td>
</tr>
<tr>
<td>9-10</td>
<td></td>
</tr>
<tr>
<td>11-12</td>
<td></td>
</tr>
<tr>
<td>13-14</td>
<td></td>
</tr>
<tr>
<td>15-16</td>
<td></td>
</tr>
</tbody>
</table>
3.4.6 CHANNEL FILTERS SETTING IN OOK MODE

The center frequency, $f_o$, is always set to 100 kHz. The chart in Figure 3-8 illustrates the receiver bandwidth when the BUTFILV<3:0> bits (FILCREG<3:0>) are changed when the polyphase filter is activated. Table 4-2 suggests a few filter settings in OOK mode along with the corresponding passive filter bandwidth and the accepted tolerance on the crystal reference.

3.4.7 RECEIVED SIGNAL STRENGTH (RSSI)

After filtering, the In-phase and Quadrature signals are amplified by a chain of 11 amplifiers, each with 6dB gain. The outputs of these amplifiers are used to evaluate the RSSI.

3.4.7.1 Resolution and Accuracy

When the RSSI resolution is 0.5 dB, the absolute accuracy is not expected to be better than ±3dB due to process and external component variation. Higher accuracy while performing absolute RSSI measurements will require additional calibration.

3.4.7.2 Acquisition Time

In OOK mode, the RSSI evaluates the signal strength by sampling I(t) and Q(t) signals 16 times in each period of the chosen IF2 frequency (refer to Section 2.10.1, Receiver Architecture). In FSK mode, the signals are sampled 16 times in each $f_{dev}$ period, $f_{dev}$ being the frequency deviation of the companion transmitter. An average is then performed over a sliding window of 16 samples. Therefore, the RSSI output register RSTSREG (RSSIVAL<7:0>) is updated 16 times in each $f_{dev}$ or IF2 period.

The following settings are recommended:

- **FSK Mode:** Ensure that the $f_{dev}$ parameter (as described in the FDEVREG register (Register 2-3) through the FDVAL<7:0> bits)) remains consistent with the actual frequency deviation of the companion transmitter.
- **OOK reception:** Ensure that the $f_{dev}$ parameter (as described in the FDEVREG register (Register 2-3) through the FDVAL<7:0> bits)) is equal to the frequency of the I(t) and Q(t) signals (that is, the second Intermediate Frequency, IF2, of the receiver). Note that, this IF2 equals $f_o$, the center frequency of the polyphase filter.
3.4.7.3 Dynamic Range

The dynamic range of the RSSI is more than 70 dB, extending from the nominal sensitivity level. The IF gain, set by the IFGAIN<1:0> bits (DMODREG<1:0>), is used to achieve this dynamic range.

The RSSI response versus the input signal that is independent of the receiver filter bandwidth. However, in the absence of any input signal, the minimum value directly reflects upon the noise floor of the receiver, which is dependant on the filter bandwidth of the receiver. Figure 3-9 illustrates the RSSI Dynamic Range Response.

FIGURE 3-9: RSSI DYNAMIC RANGE

![RSSI Dynamic Range Graph](image)

3.4.7.4 RSSI IRQ Source

The MRF89XA can be used to detect a RSSI level above a preconfigured threshold. The threshold is set using RTIVAL<7:0> bits (RSTHIREG<7:0>) and the IRQ status stored in the RIRQS bit (FTPRIREG<2>), which is cleared by writing a '1'.

An interrupt can be mapped to the IRQ0 or IRQ1 pins through the IRQ0RXS<1:0> and IRQ1RXS<1:0> bits (FTXRXIREG<7:6> and FTXRXIREG<5:4>). Figure 3-10 illustrates the timing diagram of the RSSI interrupt source, with the RTIVAL<7:0> bits (RSTHIREG<7:0>) set to '11100'.

FIGURE 3-10: RSSI IRQ TIMING DIAGRAM

![RSSI IRQ Timing Diagram](image)
3.4.8 $f_{dev}$ SETTING IN RECEIVE MODE

The effect of the $f_{dev}$ setting is different for FSK and OOK modes:

3.4.8.1 FSK RX Mode

In FSK mode, the $f_{dev}$ setting as configured by FDVAL<7:0> bits (FDEVREG<7:0>), sets sampling frequencies on the receiver. The user should program the right values to make it consistent with the frequency deviation of the FSK signal that is received.

3.4.8.2 OOK RX Mode

The frequency deviation $f_{dev}$, as described previously, sets the sampling rate of the RSSI block. It is therefore necessary to set $f_{dev}$ to the recommended low-IF frequency, IF2, of 100 kHz:

$$f_{dev} = IF2 = 100 \text{ kHz}$$

FDVAL<7:0> = 00000011

3.4.9 FSK DEMODULATOR

The FSK demodulator provides data polarity information based on the relative phase of the input I and Q signals at the baseband. Its outputs can be fed to the Bit Synchronizer to recover the timing information. The user can use the raw, unsynchronized, output of the FSK demodulator in Continuous mode.

The FSK demodulator of the MRF89XA operates effectively for FSK signals with a modulation index greater than or equal to two, as shown in Equation 3-13.

$$\beta = \frac{2 \times f_{dev}}{BRVAL} \geq 2$$

3.4.10 OOK DEMODULATOR

The OOK demodulator performs a comparison of the RSSI output and a threshold value. Three different threshold modes are available, which can be programmed through the OOKTYP<1:0> bits (DMODREG<4:3>).

The recommended mode of operation is the Peak Threshold mode, as illustrated in Figure 3-11.

In Peak Threshold mode, the comparison threshold level is the peak value of the RSSI, reduced by 6 dB. In the absence of an input signal or during the reception of a logical '0', the acquired peak value is decremented by one based on the step value of the OOKTHSV<2:0> bits (OOKCREG<7:5>) for every period value based on OOKTHPV<2:0> bits (OOKCREG<4:2>).

When the RSSI output is null for a long time (for example, after a long string of zeros is received, or if no transmitter is present), the peak threshold level will continue falling until it reaches the "Floor Threshold" that is programmed through the FTOVAL<7:0> bits (FLTHREG<7:0>).

The default settings of the OOK demodulator lead to the performance stated in Section 5.0, Electrical Characteristics.
3.4.10.1 Optimizing the Floor Threshold

The FTOVAL<7:0> bits (FLTHREG<7:0>) determine the sensitivity of the OOK receiver, as it sets the comparison threshold for weak input signals (that is, those close to the noise floor). Significant sensitivity improvements can be generated if configured correctly.

The noise floor of the receiver at the demodulator input depends on the following conditions:

- The noise figure of the receiver
- The gain of the receive chain from antenna to base band
- The matching, including SAW filter
- The bandwidth of the channel filters

The setting of the FTOVAL<7:0> bits are application-dependant. The procedure shown in the flow chart in Figure 3-12 is recommended to optimize the FTOVAL<7:0> bits.

The new floor threshold value found during this test should be the value used for OOK reception with those receiver settings.

Note that if the output signal on DATA is a logic ‘1’, the value due to the FTOVAL<7:0> bits is below the noise floor of the receiver chain. Conversely, if the output signal on DATA is a logic ‘1’, the value due to the FTOVAL<7:0> bits is several dB above the noise floor.

*FIGURE 3-12: FLOOR THRESHOLD OPTIMIZATION*

1. Set MRF89XA in OOK RX mode
2. Adjust Bit Rate, Channel filter BW
3. Default OOKTHSV<2:0> setting
4. No input signal
5. Continuous mode

- Monitor DATA pin (pin 20)
- Increment FTOVAL<7:0>

- Glitch activity on DATA?
  - Yes
  - No
- Optimization complete
3.4.10.2 Optimizing OOK Demodulator Response for Fast Fading Signals

A sudden drop in signal strength can cause the bit error rate to increase. For applications, where the expected signal drop can be estimated, the OOK demodulator parameters set by the OOKTHSV<2:0> and OOKTHPV<2:0> bits (OOKCREG<7:5> and OOKCREG<4:2>) can be optimized.

For a given number of threshold decrements per bit, specified by OOKTHPV<2:0>:

- 000 ➞ once in each chip period (default)
- 001 ➞ once in 2 chip periods
- 010 ➞ once in 4 chip periods
- 011 ➞ once in 8 chip periods
- 100 ➞ twice in each chip period
- 101 ➞ 4 times in each chip period
- 110 ➞ 8 times in each chip period
- 111 ➞ 16 times in each chip period

For each decrement of value from OOKTHSV<2:0> bits:

- 000 ➞ 0.5 dB (default)
- 001 ➞ 1.0 dB
- 010 ➞ 1.5 dB
- 011 ➞ 2.0 dB
- 100 ➞ 3.0 dB
- 101 ➞ 4.0 dB
- 110 ➞ 5.0 dB
- 111 ➞ 6.0 dB

3.4.10.3 Alternative OOK Demodulator Threshold Modes

In addition to the Peak OOK threshold mode, the user can alternatively select other two threshold detectors:

- Fixed threshold: The value is selected through the OOKCREG register (for more information, refer to Section 3.4.10.1, Optimizing the Floor Threshold).
- Average threshold: Data supplied by the RSSI block is averaged with the cut-off frequency.

In Equation 3-14, the higher cut-off frequency enables a sequence of up to eight consecutive ’0’s or ’1’s to be supported, while the lower cut-off frequency presented in Equation 3-15 allows for the correct reception of up to 32 consecutive ’0’s or ’1’s.

**EQUATION 3-14:**

\[
OOKATHC<1:0> = 00 \Rightarrow f_{\text{cutoff}} = \frac{BRVAL<6:0>}{8\pi}
\]

**EQUATION 3-15:**

\[
OOKATHC<1:0> = 11 \Rightarrow f_{\text{cutoff}} = \frac{BRVAL<6:0>}{32\pi}
\]
3.4.11 BIT SYNCHRONIZER

The Bit Synchronizer (BitSync) block provides a clean and synchronized digital output that is free of glitches. Figure 3-13 illustrates the BitSync block output when a Raw Demodulator FSK or OOK output is fed to it.

FIGURE 3-13: BitSync BLOCK OUTPUT SIGNALS

The BitSync can be disabled by setting the BSYNCEN bit (SYNCREG<6>) to ‘1’ and by holding the IRQ1 pin (pin 22) low. However, for optimum receiver performance, it has to be used when the device is running in Continuous mode. With this option a DCLK signal is present on the IRQ1 pin.

The BitSync is automatically activated in Buffered and Packet modes. The bit synchronizer bit-rate is controlled by the BRVAL<6:0> bits (BRSREG<6:0>). For a given bit rate, this parameter is determined by Equation 3-16.

EQUATION 3-16:

\[
BR = \frac{f_{\text{stat}}}{64 \times [1 + \text{val(BRVAL<6:0>)}]}
\]

For proper operation, the Bit Synchronizer must first receive three bytes of alternating logic value preamble, (that is, ‘0101’ sequences). After this start-up phase, the rising edge of the DCLK signal is centered on the demodulated bit. Subsequent data transitions will preserve this centering. This has two implications:

- If the bit rates of Transmitter and Receiver are known to be the same, the MRF89XA will be able to receive an infinite unbalanced sequence (all ‘0’ s or all ‘1’ s) with no restriction.
- If there is a difference in bit rate between TX and RX, the amount of adjacent bits at the same level that the BitSync can withstand. It can be estimated as given in Equation 3-17.

EQUATION 3-17:

\[
\text{NumberOfBits} = \frac{1}{2} \frac{BR}{\Delta BR}
\]

This implies approximately six consecutive unbalanced bytes when the Bit Rate precision is 1%, which is easily achievable (crystal tolerance is or should be at least in the range of 50 to 100 ppm).

3.4.12 ALTERNATIVE SETTINGS FOR BITSYNC AND ACTIVE FILTER

Bit Synchronizer and Active channel filter settings are a function of the reference oscillator crystal frequency, \(f_{\text{stat}}\). Settings other than those programmable with a 12.8 MHz crystal can be obtained by selecting the correct reference oscillator frequency.
3.4.13 DATA OUTPUT
After OOK or FSK demodulation, the baseband signal is made available to the user on the DATA pin (pin 20), when Continuous mode is selected. In Buffered and Packet modes, the data is retrieved from the FIFO through the SPI.

During Receive mode, the received data is filled into the Shift register and then transferred onto the FIFO stack. The FIFO is configured to generate an interrupt after receiving a defined number of bits.

When the internal FIFO is enabled, the FIFO interrupt, which is configured through the IRQ0 and IRQ1 pins (pin 21 and 22), acts as a FIFOFULL interrupt, indicating that the FIFO has been filled to its preprogrammed limit. The receiver starts filling the FIFO with data when it identifies the synchronous pattern through the synchronous pattern recognition circuit. It is recommended to set the threshold to at least half the length of the register (8 bits) to ensure that the external host microcontroller has time to set up. The synchronous pattern recognition circuit prevents the FIFO from being filled up with noise, and therefore avoids overloading the external host microcontroller.

3.4.14 RECEIVE MODE REGISTERS
The registers associated with Receive mode are:
- GCONREG (Register 2-1)
- DMODREG (Register 2-2)
- FDDEVREG (Register 2-3)
- BRSPREG (Register 2-4)
- FLTHREG (Register 2-5)
- FIFOCREG (Register 2-6)
- FTXRXIREG (Register 2-14)
- FTPRIREG (Register 2-14)
- RSTHIREG (Register 2-16)
- FILCREG (Register 2-17)
- PFCREG (Register 2-18)
- SYNCREG (Register 2-19)
- RSTSREG (Register 2-21)
- OOKCREG (Register 2-22)
- SYNCV31REG (Register 2-23)
- SYNCV23REG (Register 2-24)
- SYNCV15REG (Register 2-25)
- SYNCV07REG (Register 2-26)

3.5 Control Block Description
3.5.1 SPI INTERFACE
For more information on standard SPI between the MRF89XA and a Microcontroller, refer to Section 2.11, Serial Peripheral Interface (SPI).

3.5.2 SPI REGISTERS
The registers associated with SPI communication are:
- GCONREG (Register 2-1)
- DMODREG (Register 2-2)
- FDDEVREG (Register 2-3)
- BRSPREG (Register 2-4)

3.6 FIFO Handling
The hardware description of the FIFO is described in Section 2.12, FIFO and Shift Register (SR). The FIFO is handled by selecting the size of the FIFO, FIFO interrupts, and clearing the FIFO.

3.6.1 SIZE SELECTION
The FIFO width is programmable to 16, 32, 48 or 64 bytes using the FSIZE<1:0> bits (FIFOCREG<7:6>).

3.6.2 INTERRUPT SOURCES AND FLAGS
The MRF89XA generates an interrupt request for the host microcontroller by pulling the IRQ0 or IRQ1 pins low or high based on the events and configuration settings of these interrupts. All interrupt sources and flags are configured through the Interrupt Configuration registers, based on the occurrence of the following events:
- Interrupt Requests (IRQ0 and IRQ1) during different receive stand-by data modes (such as Continuous, Buffer and Packet) for the following event occurrences: SYNC, RSSI, PLREADY, ARDSMATCH and /FIFOEMPTY.

For example, Write Byte. The WRITEBYTE interrupt source goes high for one bit period each time a new byte is transferred from the shift register to the FIFO (that is, each time a new byte is received).
- Interrupt Requests (IRQ0 and IRQ1) during transmit modes (such as Continuous, Buffer and Packet) for the following event occurrences: Data Clock, FIFOFULL, Transmit Done, Transmit Start with IRQ0 and IRQ1.

For example, TX Done. The TXDONE interrupt source goes high when the FIFO is empty and the Shift register’s last bit has been sent to the modulator (that is, the last bit of the packet has been sent). One bit period delay is required after the rising edge of TXDONE to ensure correct RF transmission of the last bit. In practice this may not require special care in the MCU software due to IRQ processing time.
• Interrupt Requests (IRQ0 and IRQ1) during FIFO operations include:
  - FIFO Full: FIFOFULL interrupt source is high when the last FIFO byte (that is, the entire FIFO) is full; otherwise it is low.
  - FIFO Overrun Clear: FOVRRUN flag is set when a new byte is written by the user (in TX or Stand-by modes) or the Shift register (in RX mode) while the FIFO is full. Data is lost and the flag should be cleared by writing a ‘1’ (note that the FIFO will be cleared).
  - FIFO Empty: FIFOEMPTY interrupt source is low when byte 0 (that is, whole FIFO) is empty; otherwise, it is high.

- FIFO Threshold: FIFO_THRESHOLD interrupt source’s behavior depends on the running mode (TX, RX or Stand-by modes) and the threshold itself can be programmed through the FIFOCREG (B value). This behavior is illustrated in Figure 3-14.

Note: When retrieving data from the FIFO, FIFOEMPTY is updated on CSDAT falling edge (that is, when FIFOEMPTY is updated to low state the currently started read operation must be completed). In other words, the FIFOEMPTY state must be checked after each read operation for a decision on the next one (FIFOEMPTY = 1: more byte(s) to read; FIFOEMPTY = 0: no more bytes to read).

3.6.3 FIFO CLEARING

Table 3-3 below summarizes the status of the FIFO when switching between different modes.

<table>
<thead>
<tr>
<th>From</th>
<th>To</th>
<th>FIFO Status</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stand-by</td>
<td>TX</td>
<td>Cleared</td>
<td>In Buffered mode, FIFO cannot be written in Stand-by before TX</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Not cleared</td>
<td>In Packet mode, FIFO can be written in Stand-by before TX</td>
</tr>
<tr>
<td>RX</td>
<td>TX</td>
<td>Cleared</td>
<td>—</td>
</tr>
<tr>
<td>RX</td>
<td>Stand-by</td>
<td>Not cleared</td>
<td>In Packet and Buffered modes, FIFO can be read in Stand-by after RX</td>
</tr>
<tr>
<td>TX</td>
<td>RX</td>
<td>Cleared</td>
<td>—</td>
</tr>
<tr>
<td>TX</td>
<td>Stand-by</td>
<td>Not cleared</td>
<td>—</td>
</tr>
<tr>
<td>Any</td>
<td>Sleep</td>
<td>Cleared</td>
<td>—</td>
</tr>
</tbody>
</table>

3.6.4 FIFO AND INTERRUPT REGISTERS

The registers associated with FIFO and Interrupts are:
- GCONREG (Register 2-1)
- DMODREG (Register 2-2)
- FDEVREG (Register 2-3)
- BRSREG (Register 2-4)
- FLTHREG (Register 2-5)
- FIFOCREG (Register 2-6)
- FTXRXIREG (Register 2-14)
- FTPRIIREG (Register 2-15)
- RSTHIREG (Register 2-16)
- FILCREG (Register 2-17)
- PFCREG (Register 2-18)
- SYNCREG (Register 2-19)
- RSTSSREG (Register 2-21)
- OOKCREG (Register 2-22)
- FCRCREG (Register 2-32)

All the other interrupts through RSSI, SYNC, Payload, WRITEBYTE, DCLK, PLL Lock are handled through either of these interrupts discussed in the preceding sections.
3.7 Sync Word Recognition

Sync word recognition (also called as pattern recognition) is activated by setting the SYNCREN bit (SYNCREG<5>). The bit synchronizer must be activated. The block behaves like a shift register; it continuously compares the incoming data with its internally programmed Sync word and asserts the Sync IRQ source on each occasion that a match is detected. This is illustrated in Figure 3-15.

During the comparison of the demodulated data, the first bit received is compared with bit 7 (MSb) of the byte at address 22 and the last bit received is compared with bit 0 (LSb) of the last byte whose address is determined by the length of the Sync word. When the programmed Sync word is detected the user can assume that this incoming packet is for the node and can be processed accordingly.

3.7.1 Configuration

Size: Sync word size can be set to 8, 16, 24 or 32 bits through the SYNCWSZ<1:0> bits (SYNCREG<5:4>). In Packet mode this field is also used for Sync word generation in TX mode.

Error Tolerance: The number of errors tolerated in the Sync word recognition can be set to 0, 1, 2 or 3 through the SYNCTEN<1:0> bits (SYNCREG<2:1>).

Value: The Sync word value is configured in the Sync Word Parameters in the related Configuration Registers. In Packet mode this field is also used for Sync word generation in TX mode.

3.7.2 Packet Handler

The packet handler is the block used in Packet mode. Its functionality is described in Section 3.11, Packet Mode.

3.7.3 Control

The control block configures and controls the behavior of the MRF89XA according to the settings programmed in the configuration registers.

3.7.4 Sync Registers

The registers associated with Sync are:

- GCONREG (Register 2-1)
- DMODREG (Register 2-2)
- FDEVREG (Register 2-3)
- BRSPREG (Register 2-4)
- FLTHREG (Register 2-5)
- FIFOCREG (Register 2-6)
- FTXRXIREG (Register 2-14)
- FTPRIREG (Register 2-15)
- RSTHIREG (Register 2-16)
- FILCREG (Register 2-17)
- PFCREG (Register 2-18)
- SYNCREG (Register 2-19)
- RSTSREG (Register 2-21)
- OOKCREG (Register 2-22)
- SYNCV31REG (Register 2-23)
- SYNCV23REG (Register 2-24)

**FIGURE 3-15: SYNC WORD RECOGNITION**

```
RX DATA (NRZ)  Bit N-x = SSYNCVAL<o>  Bit N-1 = SYNCVAL<0>  Bit N = SYNCVAL<0>  DCLK  SYNC
```

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3.8 Data Processing

3.8.1 DATA PROCESSING BLOCK

The MRF89XA data processing blocks are as illustrated in the Figure 3-16. The role of the data processing block is to interface the data to/from the modulator/demodulator and the host microcontroller access points (SPI, Interrupts (IRQ0 and IRQ1), DATA pins). It also controls all the configuration registers.

The circuit contains several control blocks which are described in the following paragraphs.

The MRF89XA implements several data operation modes, each with their own data path through the data processing section. Depending on the data operation mode selected, some control blocks are active while others remain disabled.

3.8.2 DATA OPERATION MODES

The MRF89XA has three different data operation modes which can be selected by the user or programmer:

- Continuous mode: Each bit transmitted or received is accessed in real time at the DATA pin. This mode may be used if adequate external signal processing is available.
- Buffered mode: Each byte transmitted or received is stored in a FIFO and accessed through the SPI bus. The host microcontroller processing overhead reduced significantly compared to Continuous mode operation. The packet length is unlimited.
- Packet mode (recommended): User only provides/retrieves payload bytes to/from the FIFO. The packet is automatically built with preamble, Sync word, and optional CRC, DC free encoding and the reverse operation is performed in reception. The host microcontroller processing overhead is further reduced compared to Buffered mode. The maximum payload length is limited to the maximum FIFO limit of 64 bytes.

![MRF89XA DATA PROCESSING BLOCK DIAGRAM]

![TABLE 3-4: DATA OPERATION MODE SELECTION]

<table>
<thead>
<tr>
<th>Data Operation Mode</th>
<th>DMODE1</th>
<th>DMODE0</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Continuous</td>
<td>0</td>
<td>0</td>
<td>FTXRXIREG</td>
</tr>
<tr>
<td>Buffered</td>
<td>0</td>
<td>1</td>
<td>FTXRXIREG</td>
</tr>
<tr>
<td>Packet</td>
<td>1</td>
<td>x</td>
<td>FTXRXIREG</td>
</tr>
</tbody>
</table>
### 3.9 Continuous Mode

In Continuous mode, the NRZ data to/from the modulator/demodulator is accessed by the host microcontroller on the bidirectional DATA pin (pin 20). The SPI Data, FIFO, and packet handler are therefore inactive. Figure 3-17 illustrates the Continuous mode of operation.

#### FIGURE 3-17: CONTINUOUS MODE BLOCK DIAGRAM

![Continuous Mode Block Diagram](image)

#### FIGURE 3-18: TX PROCESSING IN CONTINUOUS MODE

![TX Processing in Continuous Mode](image)

### 3.9.1 TX PROCESSING

In TX mode, a synchronous data clock for a host microcontroller is provided on the IRQ1 pin (pin 22). Its timing with respect to the data is illustrated in Figure 3-18. DATA is internally sampled on the rising edge of DCLK so the microcontroller can change the logic state anytime outside the setup/hold time zone. The setup and hold times are shown in gray in the Figure 3-18.

The use of DCLK is compulsory in FSK and optional in OOK.

### 3.9.2 RX PROCESSING

If the bit synchronizer is disabled, the raw demodulator output is made directly available on the DATA pin and no DCLK signal is provided.

Conversely, if the bit synchronizer is enabled, synchronous cleaned data and clock are made available on the DATA and IRQ1 pins (pin 20 and 22). DATA is sampled on the rising edge of DCLK and updated on the falling edge as shown in Figure 3-19.
FIGURE 3-19: RX PROCESSING IN CONTINUOUS MODE

![Diagram of RX processing in continuous mode with DATA (NRZ) and DCLK signals.]

Note: In Continuous mode, it is always recommended to enable the bit synchronizer to clean the DATA signal even if the DCLK signal is not used by the Microcontroller (bit synchronizer is automatically enabled in Buffered and Packet mode).

3.9.3 INTERRUPT SIGNALS MAPPING

The following table gives the description of the interrupts available in Continuous mode.

**TABLE 3-5: INTERRUPT MAPPING IN CONTINUOUS RX MODE**

<table>
<thead>
<tr>
<th>Interrupt Name</th>
<th>Interrupts</th>
<th>Data Mode</th>
<th>Interrupt Type</th>
<th>Interrupt Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRQ0RXS&lt;1:0&gt;</td>
<td>00 (default)</td>
<td>IRQ0</td>
<td>Continuous</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td>01</td>
<td>IRQ0</td>
<td>Continuous</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>IRQ0</td>
<td>Continuous</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>IRQ0</td>
<td>Continuous</td>
<td>Output</td>
</tr>
<tr>
<td>IRQ1RXS&lt;1:0&gt;</td>
<td>00 (default)</td>
<td>IRQ1</td>
<td>Continuous</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td>01</td>
<td>IRQ1</td>
<td>Continuous</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>IRQ1</td>
<td>Continuous</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>IRQ1</td>
<td>Continuous</td>
<td>Output</td>
</tr>
</tbody>
</table>

Note 1: In Continuous mode, no interrupt is available in Stand-by mode.

2: See also the DMODE1:DMODE0 bits in the FTXRXIREG and FTPRIREG registers.

**TABLE 3-6: INTERRUPT MAPPING IN CONTINUOUS TX MODE**

<table>
<thead>
<tr>
<th>Interrupt Name</th>
<th>Interrupts</th>
<th>Data Mode</th>
<th>Interrupt Type</th>
<th>Interrupt Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRQ0TXST</td>
<td>0</td>
<td>IRQ0</td>
<td>Continuous</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>IRQ0</td>
<td>Continuous</td>
<td>Output</td>
</tr>
<tr>
<td>IRQ1TX</td>
<td>0 (default)</td>
<td>IRQ1</td>
<td>Continuous</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>IRQ1</td>
<td>Continuous</td>
<td>Output</td>
</tr>
</tbody>
</table>

Note 1: In Continuous mode, no interrupt is available in Stand-by mode.

2: Also refer the DMODE1:DMODE0 bits in the FTXRXIREG and FTPRIREG registers for details.
3.9.4 HOST MICROCONTROLLER INTERFACE/REQUIRED CONNECTIONS

Note that some connections may not be needed depending on the application:
- IRQ0: If Sync and RSSI interrupts are not used, leave the pin floating.
- IRQ1: If the device is never used in TX FSK mode (DCLK connection is not compulsory in RX and TX OOK modes), leave the pin floating.
- SDO: If no read register access is needed, pull-up to VDD through a 100 kΩ resistor.

Note: The CSDAT pin (pin15), which is unused in Continuous mode, should be pulled-up to VDD through a 100 kΩ resistor.

Table 2-4 details the MRF89XA pin configuration and chip mode.

3.9.5 CONTINUOUS MODE EXAMPLE

The data processing related registers are appropriately configured as listed Table 3-7. In this example we assume that both the Bit synchronizer and Sync word recognition are on.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Register Bits</th>
<th>TX</th>
<th>RX</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMODREG</td>
<td>DMODE0, DMODE1</td>
<td>X</td>
<td>X</td>
<td>Defines data operation mode (→ Continuous)</td>
</tr>
<tr>
<td>FTXRXIRES</td>
<td>IRQ0RXS&lt;1:0&gt;</td>
<td>X</td>
<td></td>
<td>Defines IRQ0 source in RX mode</td>
</tr>
<tr>
<td>SYNCREG</td>
<td>SYNCREN</td>
<td>X</td>
<td></td>
<td>Enables Sync word recognition</td>
</tr>
<tr>
<td>SYNCREG</td>
<td>SYNCWSZ&lt;1:0&gt;</td>
<td>X</td>
<td></td>
<td>Defines Sync word size</td>
</tr>
<tr>
<td>SYNCREG</td>
<td>SYNCWTEN&lt;1:0&gt;</td>
<td>X</td>
<td></td>
<td>Defines the error tolerance on Sync word recognition</td>
</tr>
<tr>
<td>SYNCV31REG</td>
<td>SYNCV&lt;31:24&gt;</td>
<td>X</td>
<td></td>
<td>Defines Sync word value</td>
</tr>
<tr>
<td>SYNCV23REG</td>
<td>SYNCV&lt;23:16&gt;</td>
<td>X</td>
<td></td>
<td>Defines Sync word value</td>
</tr>
<tr>
<td>SYNCV15REG</td>
<td>SYNCV&lt;15:8&gt;</td>
<td>X</td>
<td></td>
<td>Defines Sync word value</td>
</tr>
<tr>
<td>SYNCV07REG</td>
<td>SYNCV&lt;7:0&gt;</td>
<td>X</td>
<td></td>
<td>Defines Sync word value</td>
</tr>
</tbody>
</table>
3.10 Buffered Mode

In Buffered mode operation the NRZ data to/from the modulator or demodulator is not accessed by the host microcontroller but is stored in the FIFO and accessed via the SPI data interface. This frees the host microcontroller for other tasks between processing data from the MRF89XA. In addition, it simplifies software development overhead and reduces microcontroller performance requirements (i.e., speed, response). Note that in this mode the packet handler stays inactive. The interface for Buffer mode is shown in Figure 3-21.

An important feature is also the ability to empty the FIFO in Stand-by mode, ensuring low-power consumption and adding greater software flexibility.

**Note:** In this case Bit Synchronizer is automatically enabled in Buffered mode. The Sync word recognition must be enabled (SYNCREN = 1) independently of the FIFO filling method selected (FIFOFM).

3.10.1 TX PROCESSING

After entering TX in Buffered mode, the MRF89XA expects the host microcontroller to write to the FIFO, through the SPI data interface, and all the data bytes to be transmitted (preamble, Sync word, payload).

Actual transmission of the first byte will start either when the FIFO is not empty (that is, first byte written by the host microcontroller) or when the FIFO is full depending on the IRQ0TXST bit (FTPRIREG<4>) setting.

In Buffered mode the packet length is not limited, as long as there are bytes inside the FIFO to be sent. When the last byte is transferred to the SR, the FIFOEMPTY IRQ source is issued to interrupt the host microcontroller, when the FIFO can still be filled with additional bytes if required.

When the last bit of the last byte has left the Shift Register (SR) (i.e., eight bit periods later), the TXDONE interrupt source is issued and the user can exit TX mode after waiting at least one bit period from the last bit processed by the modulator. If the transmitter is switched OFF during transmission (for example, entering another chip mode), it will stop immediately, even if there is still unsent data.
3.10.2 RX PROCESSING

After entering RX in Buffered mode, the MRF89XA requires the host microcontroller to get received data from the FIFO. The FIFO will start being filled with received bytes either when a Sync word has been detected (in this case only the bytes following the Sync word are filled into the FIFO) or when the FIFOFSC bit (FPPRIREG<6>) is issued by the user depending on the state of bit, FIFOFM (FTPRIREG<7>).

In Buffered mode, the packet length is not limited that is, as long as FIFOFSC is set the received bytes are shifted into the FIFO.

The host microcontroller software must therefore manage the transfer of the FIFO contents by interrupt and ensure reception of the correct number of bytes. In this mode, even if the remote transmitter has stopped, the demodulator will output random bits due to noise.

When the FIFO is full, the FIFOFULL IRQ (source) is issued to alert the host microcontroller that at that time, the FIFO can still be unfilled without data loss. If the FIFO is not unfilled, after the SR is full (that is, 8 bits periods later) FOVRRUN is asserted and the SR’s content is lost.

Figure 3-23 illustrates RX processing with a 16 byte FIFO size and FIFOFSC = 0. Note that in the example of Section 3.10.5, Buffered Mode Example, the host microcontroller does not retrieve any bytes from the FIFO through SPI data interface, causing an overrun.
3.10.3 INTERRUPT SIGNALS MAPPING

Table 3-8 and Table 3-9 describes the interrupts available in Buffered mode.

### TABLE 3-8: INTERRUPT MAPPING IN BUFFERED RX AND STAND-BY MODE

<table>
<thead>
<tr>
<th>Interrupt Name</th>
<th>Interrupts</th>
<th>Data Mode</th>
<th>Interrupt Type</th>
<th>RX Interrupt Source</th>
<th>Stand-by Interrupt Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRQ0RXS&lt;1:0&gt;</td>
<td>IRQ0</td>
<td>Buffered</td>
<td>Output</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>00 (default)</td>
<td>IRQ0</td>
<td>Buffered</td>
<td>Output</td>
<td>WRITEBYTE</td>
<td>—</td>
</tr>
<tr>
<td>01</td>
<td>IRQ0</td>
<td>Buffered</td>
<td>Output</td>
<td>FIFOEMPTY</td>
<td>FIFOEMPTY</td>
</tr>
<tr>
<td>10</td>
<td>IRQ0</td>
<td>Buffered</td>
<td>Output</td>
<td>Sync Pattern</td>
<td>—</td>
</tr>
</tbody>
</table>

**Note:** Also refer the DMODE1 and DMODE0 bits in the FTXRXIREG and FTPRIREG registers for details.

### TABLE 3-9: INTERRUPT MAPPING IN BUFFERED TX MODE

<table>
<thead>
<tr>
<th>Interrupt Name</th>
<th>Interrupts</th>
<th>Data Mode</th>
<th>Interrupt Type</th>
<th>Interrupt Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRQ0TXST</td>
<td>IRQ0</td>
<td>Buffered</td>
<td>Output</td>
<td>FIFOEMPTY</td>
</tr>
<tr>
<td>0 (default)</td>
<td>IRQ0</td>
<td>Buffered</td>
<td>Output</td>
<td>FIFOEMPTY</td>
</tr>
<tr>
<td>1</td>
<td>IRQ0</td>
<td>Buffered</td>
<td>Output</td>
<td>FIFOEMPTY</td>
</tr>
<tr>
<td>IRQ1TX</td>
<td>IRQ1</td>
<td>Buffered</td>
<td>Output</td>
<td>FIFOFULL</td>
</tr>
<tr>
<td>0 (default)</td>
<td>IRQ1</td>
<td>Buffered</td>
<td>Output</td>
<td>TXDONE</td>
</tr>
<tr>
<td>1</td>
<td>IRQ1</td>
<td>Buffered</td>
<td>Output</td>
<td>FIFOFULL</td>
</tr>
</tbody>
</table>

**Note:** Also refer the DMODE1 and DMODE0 bits in the FTXRXIREG and FTPRIREG registers for details.

3.10.4 HOST MICROCONTROLLER CONNECTIONS IN BUFFERED MODE

Depending on the application, some host microcontroller connections may not be required:

- **IRQ0:** if none of the relevant IRQ sources are used, leave the pin floating.
- **IRQ1:** if none of the relevant IRQ sources are used, leave the pin floating.
- **SDO:** if no read register access is needed and the device is used in TX mode only. In this case, pull-up to VDD through a 100 kΩ resistor.

**Note:** The `DATA` pin (pin 20), which is unused in Buffered mode, should be pulled-up to VDD through a 100 kΩ resistor. Table 2-4, provides details about the MRF89XA pin configuration and chip mode.

### FIGURE 3-24: HOST MCU CONNECTIONS IN BUFFERED MODE

3.10.5 BUFFERED MODE EXAMPLE

The data processing related registers are appropriately configured as listed in Table 3-10. In this example we assume Sync word recognition is on and FIFOFM = 0.
### TABLE 3-10: CONFIGURATION REGISTERS RELATED TO DATA PROCESSING IN BUFFERED MODE

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Register Bits</th>
<th>TX</th>
<th>RX</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMODEREG</td>
<td>DMODE0, DMODE1</td>
<td>X</td>
<td>X</td>
<td>Defines data operation mode (→Buffered)</td>
</tr>
<tr>
<td>FIFOCREG</td>
<td>FSIZE&lt;1:0&gt;</td>
<td>X</td>
<td>X</td>
<td>Defines FIFO size</td>
</tr>
<tr>
<td>FIFOCREG</td>
<td>FTINT&lt;5:0&gt;</td>
<td>X</td>
<td>X</td>
<td>Defines FIFO threshold</td>
</tr>
<tr>
<td>FTXRXIREG</td>
<td>IRQ0RXS&lt;1:0&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines IRQ0 source in RX mode</td>
</tr>
<tr>
<td>FTXRXIREG</td>
<td>IRQ1RXS&lt;1:0&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines IRQ1 source in RX mode</td>
</tr>
<tr>
<td>FTXRXIREG</td>
<td>IRQ1TX</td>
<td>X</td>
<td>—</td>
<td>Defines IRQ1 source in TX mode</td>
</tr>
<tr>
<td>FTXRREG</td>
<td>IRQ0TXST</td>
<td>X</td>
<td>—</td>
<td>Defines IRQ0 source in TX mode</td>
</tr>
<tr>
<td>FTXRREG</td>
<td>FIFOFSC</td>
<td>—</td>
<td>X</td>
<td>Controls FIFO filling status</td>
</tr>
<tr>
<td>SYNCREG</td>
<td>SYNCWZS&lt;1:0&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines Sync word size</td>
</tr>
<tr>
<td>SYNCREG</td>
<td>SYNCTEN&lt;1:0&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines the error tolerance on Sync word recognition</td>
</tr>
<tr>
<td>SYNCV31REG</td>
<td>SYNCV&lt;31:24&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines Sync word value</td>
</tr>
<tr>
<td>SYNCV23REG</td>
<td>SYNCV&lt;23:16&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines Sync word value</td>
</tr>
<tr>
<td>SYNCV15REG</td>
<td>SYNCV&lt;15:8&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines Sync word value</td>
</tr>
<tr>
<td>SYNCV07REG</td>
<td>SYNCV&lt;7:0&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines Sync word value</td>
</tr>
</tbody>
</table>

**TX Mode:**

1. Program TX start condition and IRQs: Start TX when FIFO is not empty (IRQ0TXST = 1) and IRQ1 mapped to TXDONE (IRQ1TX = 1).
2. Go to TX mode (and wait for TX to be ready, see Figure 5-3).
3. Write packet bytes into FIFO. TX starts when the first byte is written (IRQ0TXST = 1). Assumption: The FIFO is being filled through the SPI Data faster than being unfilled by SR.
4. Wait for TXDONE interrupt (+ 1 bit period).
5. Go to Sleep mode.

**RX Mode:**

1. Program RX/Stand-by interrupts: IRQ0 mapped to FIFOEMPTY (IRQ0RXS<1:0> = 10) and IRQ1 mapped to FIFO threshold (IRQ1RXS<1:0> = 11). Configure FIFO threshold to an appropriate value (for example, to detect packet end, if its length is known).
2. Go to RX mode (note that RX is not ready immediately, see Section 5.3.1, Optimized Receive Cycle for more information).
3. Wait for FIFO threshold interrupt (i.e., Sync word has been detected and FIFO has filled up to the defined threshold).
4. If it is packet end, go to Stand-by (SR’s content is lost).
5. Read packet byte from FIFO until FIFOEMPTY goes low (or correct number of bytes is read).
6. Go to Sleep mode.
3.11 Packet Mode

Similar to Buffered mode operation, in Packet mode the NRZ data to/from the modulator or demodulator is not directly accessed by the host microcontroller, but it is stored in the FIFO and accessed through the SPI data interface.

The MRF89XA’s packet handler also performs several packet oriented tasks such as Preamble and Sync word generation, CRC calculation/check, DC scrambling (whitening/dewhitenning of data), address filtering. This simplifies the software still further and reduces microcontroller overhead by performing these repetitive tasks within the MRF89XA itself.

Another important feature is the ability to fill and empty the FIFO in Stand-by mode, ensuring optimum power consumption and adding more flexibility to the software. Figure 3-25 shows the interface diagram during Packet Mode.

Note: Bit Synchronizer and Sync word recognition are automatically enabled in Packet mode.

FIGURE 3-25: PACKET MODE BLOCK DIAGRAM
3.11.0.1 Packet Format

Two packet formats are supported: Fixed length and Variable length, which are selected by the PKTLENF bit (PKTCREG<7>). The maximum size of the payload is limited by the size of the FIFO selected (16, 32, 48 or 64 bytes).

3.11.0.2 Fixed Length Packet Format

In applications where the packet length is fixed in advance, this mode of operation may be useful to minimize RF overhead (no length byte field is required). All nodes, whether TX only, RX only, or TX/RX will be programmed with the same packet length value.

The length of the payload is set by the PLDPLEN<6:0> bits (PLOADREG<6:0>) and is limited by the size of the FIFO selected. The length stored in this register relates only to the payload, which includes the message and the optional address byte. In this mode, the payload must contain at least one byte (that is, address or message).

A fixed length packet frame format is illustrated in Figure 3-26, which contains the following fields:

- Preamble (1010...)
- Sync word (Network ID)
- Optional Address byte (Node ID)
- Message data
- Optional 2-bytes CRC checksum

FIGURE 3-26: FIXED LENGTH PACKET FORMAT
3.11.0.3 Variable Length Packet Format

This mode is necessary in applications where the length of the packet is not known in advance and can vary over time. It is then necessary for the transmitter to send the length information together with each packet in order for the receiver to operate properly.

In this mode the length of the payload, indicated by the length byte in Figure 3-27, is given by the first byte of the FIFO and is limited only by the width of the FIFO selected. In this mode, the payload must contain at least 2 bytes (that is, length plus address or message byte).

A variable length packet frame format is illustrated in Figure 3-27, which contains the following fields:

- Preamble (1010...)
- Sync word (Network ID)
- Length byte
- Optional Address byte (Node ID)
- Message data
- Optional 2-bytes CRC checksum

**Note:** The length byte is not included in the CRC calculation.

**FIGURE 3-27: VARIABLE LENGTH PACKET FORMAT**

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preamble 1 to 4 bytes</td>
<td>Optional DC free data coding</td>
</tr>
<tr>
<td>Sync Word 1 to 4 bytes</td>
<td>CRC checksum calculation</td>
</tr>
<tr>
<td>Length byte</td>
<td>Length</td>
</tr>
<tr>
<td>Address byte</td>
<td>Message 0 to (FIFO size - 1) bytes</td>
</tr>
<tr>
<td>Message data</td>
<td>CRC 2-bytes</td>
</tr>
<tr>
<td>Payload/FIFO</td>
<td>Fields added by the packet handler in TX and processed and removed in RX</td>
</tr>
<tr>
<td></td>
<td>Optional, user provided field which are part of the payload</td>
</tr>
<tr>
<td></td>
<td>Message part of the payload</td>
</tr>
</tbody>
</table>
3.11.1 TX PROCESSING

In TX mode, the packet handler dynamically builds the packet by performing the following operations on the payload available in the FIFO:

- Add a programmable number of preamble bytes
- Add a programmable Sync word
- Optionally calculating CRC over complete payload field (optional length byte plus optional address byte plus message) and appending the 2 bytes checksum.
- Optional DC-free encoding of the data (Manchester or Whitening).

Only the payload (including optional address and length fields) is to be provided by the user in the FIFO.

Assuming that the device is in TX mode, and then depending on the setting of the IRQ0TXST bit (FTPRI-REG<4>), packet transmission (starting with programmed preamble) will start either after the first byte is written into the FIFO (IRQ0TXST = 1) or after the number of bytes written reaches the user defined threshold (IRQ0TXST = 0). The FIFO can be fully or partially filled in Stand-by mode through the FRWAXS bit (FCRCREG<6>). In this case, the start condition will only be checked when entering TX mode.

At the end of the transmission (TXDONE = 1), the user must explicitly exit TX mode if required (for example, back to Stand-by mode).

While in TX mode, before and after packet transmission (not enough bytes or TXDONE), additional preamble bytes are sent to the modulator. When the start condition is met, the current additional preamble byte is completely sent before the transmission of the next packet (that is, programmed preamble) is started.

3.11.2 RX PROCESSING

In RX mode the packet handler extracts the user payload to the FIFO by performing the following operations:

- Receiving the preamble and stripping off the preamble
- Detecting the Sync word and stripping off the Sync word
- Optional DC-free decoding of data
- Optionally checking the address byte
- Optionally checking CRC and reflecting the result on the STSCRCEN bit (PKTREG<0>) and CRCOK from IRQ source (for more information, refer to Register 2-14).

Only the payload (including optional address and length fields) is made available in the FIFO.

PLREADY and CRCOK interrupts (the latter only if CRC is enabled) can be generated to indicate the end of the packet reception (for more information, refer to Register 2-14).

By default, if the CRC check is enabled and fails for the current packet, the FIFO is automatically cleared and neither of the two interrupts is generated and new packet reception is started. This autoclear function can be disabled via the ACFCRC bit (FCRCREG<7>) and, in this case, even if CRC fails, the FIFO is not cleared and only the PLREADY IRQ source is issued.

Once fully received, the payload can also be fully or partially retrieved in Stand-by mode from the FRWAXS bit. At the end of the reception, although the FIFO automatically stops being filled, it is still up to the user to explicitly exit RX mode if required (for example, go to Stand-by mode to get payload). The FIFO must be empty for a new packet reception to start.

3.11.3 PACKET FILTERING

MRF89XA packet handler offers several mechanisms for packet filtering ensuring that only useful packets are made available to the host microcontroller, significantly reducing system power consumption and software complexity.

3.11.3.1 Sync Word-Based

Sync word filtering or recognition is enabled in Packet mode. It is used for identifying the start of the payload and also for network identification. As described earlier, the Sync word recognition block is configured (with size, error tolerance, value) from the SYNCREG, SYNCSZ, SYNCTEN, SYNCV31-0 bits in the SYNCREG, SYNCV31REG, SYNCV23REG, SYNCV15REG and SYNCV07REG Configuration registers. This information is used for appending Sync word in TX and filtering packets in RX.

Every received packet that does not start with this locally configured Sync word is automatically discarded and no interrupt is generated.

When the Sync word is detected, payload reception automatically starts and the Sync IRQ source is issued.

3.11.3.2 Length Based

In variable length Packet mode, the PLDPLEN<6:0> bits (PLOADREG<6:0>) must be programmed with the maximum length permitted. If the received length byte is smaller than this maximum, the packet is accepted and processed; otherwise, it is discarded.

To disable this function the user should set the value of the PLDPLEN<6:0> bits to the value of the FIFO size selected.

Note: The received length byte, as part of the payload, is not stripped off the packet and is made available in the FIFO.
3.11.3.3 Address Based

Address filtering can be enabled through the ADDFIL<1:0> bits (PKTCREG<2:1>). It adds another level of filtering above Sync word, which is typically useful in multi-node networks where a network ID is shared between all nodes (Sync word) and each node has its own ID (address).

Three address based filtering options are available:

- **ADDFIL = 01**: Received address field is compared with the internal register, NADDSREG. If they match, the packet is accepted and processed; otherwise, it is discarded.
- **ADDFIL = 10**: Received address field is compared with the internal register, NADDSREG, and the constant 0x00. If either is a match, the received packet is accepted and processed; otherwise, it is discarded. This additional check with a constant is useful for implementing broadcast in multi-node networks.
- **ADDFIL = 11**: Received address field is compared with the internal register, NADDSREG, and the constants 0x00 and 0xFF. If any of the three matches, the received packet is accepted and processed, otherwise it is discarded. These additional checks with constants are useful for implementing broadcast commands of all nodes.

Here the received address byte, as part of the payload, is not stripped off the packet and is made available in the FIFO. In addition, NADDSREG and ADDFIL<1:0> bits from PKTCREG only apply to RX. On TX side, if address filtering is expected, the address byte should be put into the FIFO like any other byte of the payload.

3.11.3.4 CRC-Based

The CRC check is enabled by setting the CHKCRCEN bit (PKTCREG<3>). This bit is used for checking the integrity of the message. A 16-bit CRC checksum is calculated on the payload part of the packet and is appended to the end of the transmitted message. The CRC checksum is calculated on the received payload and compared to the transmitted CRC. The result of the comparison is stored in the STSCRCEN bit (PKTCREG<0>) and an interrupt can also be generated on IRQ1.

- On the TX side a two byte CRC checksum is calculated on the payload part of the packet and appended to the end of the message.
- On the RX side the checksum is calculated on the received payload and compared with the two checksum bytes received. The result of the comparison is stored in the STSCRCEN bit from and the CRCOK IRQ source (refer to Register 2-14 for details).

By default, if the CRC check fails, the FIFO is cleared and no interrupt is generated. This filtering function can be disabled through the ACFCRC bit (FCRCREG<7>) and if CRC fails, the FIFO is not cleared and only the PLREADY interrupt goes high (for more information, refer to Register 2-14). In both the cases, the two CRC checksum bytes are stripped off by the packet handler and only the payload is made available in the FIFO.

The CRC is based on the CCITT polynomial as illustrated in Figure 3-28. This implementation also detects errors due to leading and trailing zeros. For more information on CRC polynomial computation in C#, see Appendix B: “CRC Computation in C# (convertible to c)”

![CRC Polynomial Implementation](image)
3.11.4 DC-FREE DATA MECHANISMS

The payload to be transmitted may contain long sequences of ‘1’s and ‘0’s, which introduces a DC bias in the transmitted signal, which causes a non-uniform power distribution spectrum over the occupied channel bandwidth. These sequences also degrade the performance of the demodulation and data, and clock recovery functions in the receiver, which basically introduces data dependencies in the normal operation of the demodulator. System performance can be enhanced if the payload bits are randomized to reduce DC biases and increase the number of bit transitions. Therefore, it is useful if the transmitted data is random and DC-free.

To handle such instances, two techniques are available in the packet handler: Manchester encoding and Data Whitening. However, only one of the two methods should be enabled at a time.

3.11.4.1 Manchester Data Encoding

Manchester encoding/decoding is enabled by setting the MCHSTREN bit (PLOADREG<7>) and can be used in Packet mode only. The NRZ data is converted to Manchester code by coding ‘1’ as ‘10’ and ‘0’ as ‘01’.

Figure 3-29 illustrates Manchester data encoding. NRZ data is converted to Manchester by encoding 1 bits as 10 chip sequences, and 0 bits as 01 chip sequences. Manchester encoding guarantees DC-balance and frequent data transitions in the encoded data. The maximum Manchester chip rate corresponds to the maximum bit rate given in the Transmitter Electrical specifications in Table 5-6.

In this case, the maximum chip rate is the maximum bit rate given in the specifications section and the actual bit rate is half the chip rate. Manchester encoding and decoding is only applied to the payload and CRC checksum while preamble and Sync word are kept NRZ. However, the chip rate from preamble to CRC is the same and defined by the BRVAL<6:0> bits (BRSREG<6:0>) (Chip Rate = Bit Rate NRZ = 2 x Bit Rate Manchester).

Therefore Manchester encoding/decoding is made transparent for the user, who still provides/retrieves NRZ data to/from the FIFO. See the Manchester encoding/decoding bit pattern in Figure 3-30.

3.11.4.2 Data Whitening

Another technique called data whitening or scrambling is widely used for randomizing the user data before radio transmission. The data is whitened using a random sequence on the TX side and dewhitenen on the RX side using the same sequence. Compared to Manchester technique it has the advantage of retaining the NRZ data rate (that is, actual bit rate is not halved).

The whitening/dewhittening process is enabled by setting the WHITEN1 bit (PKTCREG<4>). A 9-bit Linear Feedback Shift Register (LFSR) is used to generate a random sequence. The payload and 2-byte CRC checksum is then XORed with this random sequence as illustrated in Figure 3-31. The data is dewhitenen on the receiver side by XORing with the same random sequence.

Payload whitening/dewhitenen is made transparent for the user, who still provides/retrieves NRZ data to/from the FIFO.

---

**FIGURE 3-29: MANCHESTER DATA ENCODING**

**FIGURE 3-30: MANCHESTER ENCODING/DECODING**

In the figure, the top row represents the transmitted data, the middle row shows the Manchester encoded data, and the bottom row illustrates the User/NRZ bits. The chip rate (BR) and bit rate (NRZ) are indicated in the legend. The Manchester encoding/decoding process is shown for different scenarios, including Manchester encoding enabled and disabled, and for different data patterns.
3.11.5 INTERRUPT SIGNAL MAPPING

Table 3-11 and Table 3-12 provides the descriptions of the interrupts available in Packet mode.

**TABLE 3-11: INTERRUPT MAPPING IN RX AND STAND-BY IN PACKET MODE**

<table>
<thead>
<tr>
<th>Interrupt Name</th>
<th>Interrupts</th>
<th>Data Mode</th>
<th>Interrupt Type</th>
<th>RX Interrupt Source</th>
<th>Stand-by Interrupt Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRQ0RXS&lt;1:0&gt;</td>
<td>IRQ0</td>
<td>Packet</td>
<td>Output</td>
<td>PLREADY</td>
<td>—</td>
</tr>
<tr>
<td>00 (default)</td>
<td>IRQ0</td>
<td>Packet</td>
<td>Output</td>
<td>WRITEBYTE</td>
<td>—</td>
</tr>
<tr>
<td>01 IRQ0</td>
<td>Packet</td>
<td>Output</td>
<td>FIFOEMPTY</td>
<td>FIFOEMPTY</td>
<td>—</td>
</tr>
<tr>
<td>11 IRQ0</td>
<td>Packet</td>
<td>Output</td>
<td>Sync/Address Match(2)</td>
<td>—</td>
<td></td>
</tr>
</tbody>
</table>

**TABLE 3-12: INTERRUPT MAPPING IN TX PACKET MODE**

<table>
<thead>
<tr>
<th>Interrupt Name</th>
<th>Interrupts</th>
<th>Data Mode</th>
<th>Interrupt Type</th>
<th>Interrupt Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRQ0TXST</td>
<td>IRQ0</td>
<td>Packet</td>
<td>Output</td>
<td>FIFO_THRESHOLD</td>
</tr>
<tr>
<td>0 (default)</td>
<td>IRQ0</td>
<td>Packet</td>
<td>Output</td>
<td>FIFOEMPTY</td>
</tr>
<tr>
<td>IRQ1TX</td>
<td>IRQ1</td>
<td>Packet</td>
<td>Output</td>
<td>FIFOFULL</td>
</tr>
</tbody>
</table>

Note 1: Address Match valid only if Address Filtering is Enabled.

Note 2: Also refer the DMODE1 and DMODE0 bits in the FTXRXIREG and FTPRIREG registers for details.

**FIGURE 3-31: DATA WHITENING**

LFSR Polynomial = x^9 + x^5 + 1

Transmit data — Whitened data
3.11.6 HOST MICROCONTROLLER INTERFACE CONNECTIONS IN PACKET MODE

Depending on the application, some of the host microcontroller connections may not be needed:

- IRQ0: If none of the relevant IRQ sources are used. In this case, leave the pin floating.
- IRQ1: If none of the relevant IRQ sources are used. In this case, leave the pin floating.
- SDO: If no read register access is needed and the device is used in TX mode only. In this case, pull up to VDD through a 100 kΩ resistor.

**Note:** The DATA pin (pin 20), which is unused in Packet mode, should be pulled-up to VDD through a 100 kΩ resistor. Table 2-4, provides details about MRF89XA pin configuration and chip mode.

3.11.7 PACKET MODE EXAMPLE

The data processing related registers are appropriately configured as shown in Table 3-13. In this example we assume CRC is enabled with autoclear on.

### TABLE 3-13: CONFIGURATION REGISTERS RELATED TO DATA PROCESSING (ONLY) IN PACKET MODE

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Register Bits</th>
<th>TX</th>
<th>RX</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMODREG</td>
<td>DMODE0, DMODE1</td>
<td>X</td>
<td>X</td>
<td>Defines data operation mode (→Packet)</td>
</tr>
<tr>
<td>FIFOCREG</td>
<td>FSIZE&lt;1:0&gt;</td>
<td>X</td>
<td>X</td>
<td>Defines FIFO size</td>
</tr>
<tr>
<td>FIFOCREG</td>
<td>FTINT&lt;5:0&gt;</td>
<td>X</td>
<td>X</td>
<td>Defines FIFO threshold</td>
</tr>
<tr>
<td>FTXRXIREG</td>
<td>IRQ0RXS&lt;1:0&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines IRQ0 source in RX &amp; Stand-by modes</td>
</tr>
<tr>
<td>FTXRXIREG</td>
<td>IRQ1RXS&lt;1:0&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines IRQ1 source in RX &amp; Stand-by modes</td>
</tr>
<tr>
<td>FTXRXIREG</td>
<td>IRQ1TX</td>
<td>X</td>
<td>—</td>
<td>Defines IRQ1 source in TX mode</td>
</tr>
<tr>
<td>FTPRIIREG</td>
<td>IRQ0TXST</td>
<td>X</td>
<td>—</td>
<td>Defines IRQ0 source in TX mode</td>
</tr>
<tr>
<td>SYNCREG</td>
<td>SYNCREN</td>
<td>—</td>
<td>X</td>
<td>Enables Sync word recognition</td>
</tr>
<tr>
<td>SYNCREG</td>
<td>SYNCWSZ&lt;1:0&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines Sync word size</td>
</tr>
<tr>
<td>SYNCREG</td>
<td>SYNTEN&lt;1:0&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines the error tolerance on Sync word recognition</td>
</tr>
<tr>
<td>SYNCV31REG</td>
<td>SYNCV&lt;31:24&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines Sync word value</td>
</tr>
<tr>
<td>SYNCV23REG</td>
<td>SYNCV&lt;23:16&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines Sync word value</td>
</tr>
<tr>
<td>SYNCV15REG</td>
<td>SYNCV&lt;15:8&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines Sync word value</td>
</tr>
<tr>
<td>SYNCV07REG</td>
<td>SYNCV&lt;7:0&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines Sync word value</td>
</tr>
<tr>
<td>PLOADREG</td>
<td>MCHSTREN</td>
<td>X</td>
<td>X</td>
<td>Enables Manchester encoding/decoding</td>
</tr>
<tr>
<td>PLOADREG</td>
<td>PLDPLEN&lt;6:0&gt;</td>
<td>X(1)</td>
<td>X</td>
<td>Length in fixed format, max RX length in variable format</td>
</tr>
<tr>
<td>NADDSREG</td>
<td>NLADDR&lt;7:0&gt;</td>
<td>—</td>
<td>X</td>
<td>Defines node address for RX address filtering</td>
</tr>
<tr>
<td>PKTCREG</td>
<td>PKTLENF</td>
<td>X</td>
<td>X</td>
<td>Defines packet format (fixed or variable length)</td>
</tr>
<tr>
<td>PKTCREG</td>
<td>PRESIZE&lt;1:0&gt;</td>
<td>X</td>
<td>—</td>
<td>Defines the size of preamble to be transmitted</td>
</tr>
<tr>
<td>PKTCREG</td>
<td>WHITEON</td>
<td>X</td>
<td>X</td>
<td>Enables whitening/de-whitening process</td>
</tr>
<tr>
<td>PKTCREG</td>
<td>CRCEN</td>
<td>X</td>
<td>X</td>
<td>Enables CRC calculation/check</td>
</tr>
<tr>
<td>PKTCREG</td>
<td>ADDFIL&lt;1:0&gt;</td>
<td>—</td>
<td>X</td>
<td>Enables and defines address filtering</td>
</tr>
<tr>
<td>PKTCREG</td>
<td>CRSTSEN</td>
<td>X</td>
<td>X</td>
<td>Enables CRC Status check</td>
</tr>
<tr>
<td>FCRCERG</td>
<td>ACFCRC</td>
<td>—</td>
<td>X</td>
<td>Enables FIFO autoclear if CRC failed</td>
</tr>
<tr>
<td>FCRCERG</td>
<td>FRWAXS</td>
<td>X</td>
<td>X</td>
<td>Defines FIFO access in Stand-by mode</td>
</tr>
</tbody>
</table>

**Note 1:** Fixed format only.

---

**FIGURE 3-32: HOST MCU CONNECTIONS IN PACKET MODE**

MRF89XA

PIC®

Microcontroller
TX Mode:
1. Program TX start condition and IRQs: Start TX when FIFO is not empty (IRQ0TXST = 1) and IRQ1 mapped to TXDONE (IRQ1TX = 1)
2. Set CMOD = Stand-by mode and enable FIFO access in Stand-by mode.
3. Write all payload bytes into FIFO (FRWAXS = 0, Stand-by interrupts can be used if needed).
4. Go to TX mode. When TX is ready (automatically handled) TX starts (IRQ0TXST = 1).
5. Wait for TXDONE interrupt (plus one bit period).
6. Go to Sleep mode.

RX Mode:
1. Program RX/Stand-by interrupts: IRQ0 mapped to FIFOEMPTY (IRQ0RXS = 10) and IRQ1 mapped to FIFO Threshold (IRQ1RXS = 00). Configure FIFO Threshold to an appropriate value (for example, to detect packet end, if its length is known).
2. Go to RX mode by setting the CMOD register. FIFO threshold interrupt, when the FIFO is full with received contents. So you have to enable IRQ1 to "CRCOK" interrupt.
3. Wait for CRCOK interrupt.
4. Go to Stand-by mode.
5. Read payload byte from FIFO until FIFOEMPTY goes low (FRWAXS = 1).
6. Go to Sleep mode.

3.11.8 ADDITIONAL INFORMATION TO HANDLE PACKET MODE

If the number of bytes filled for transmission is greater than the actual length of the packet to be transmitted and IRQ0TXST = 1, the FIFO is cleared after the packet has been transmitted. Therefore, the extra bytes in the FIFO are lost. Otherwise, if IRQ0TXST = 0, the extra bytes are kept in the FIFO. This opens up the possibility of transmitting more than one packet by filling the FIFO with multiple packet messages.

It is not possible to receive multiple packets. After a packet has been received and filled in the FIFO all its contents needs to be read (that is, the FIFO must be empty for a new packet reception to be initiated).

The PLREADY interrupt goes high when the last payload byte is available in the FIFO and remains high until all its data are read. Similar behavior is applicable to ARDSMTP and CRCOK interrupts.

The CRC result is available in the STSCRCEN bit immediately as the CRCOK and PLREADY interrupt sources are triggered. In RX mode, the STSCRCEN bit is cleared when the complete payload has been read from the FIFO. If the payload is read in Stand-by mode, the STSCRCEN bit is cleared when the user goes back to RX mode and a new Sync word is detected.

The FIFOFM and FIFOFSC bits have no meaning in Packet mode and should be set to their default values only.

3.11.9 PACKET MODE REGISTERS

The registers associated with Packet mode are:

- GCONREG (Register 2-1)
- DMODREG (Register 2-2)
- FDEVREG (Register 2-3)
- BRSREG (Register 2-4)
- FLTHREG (Register 2-5)
- FIFOCREG (Register 2-6)
- FXRXIREG (Register 2-14)
- FTPRIREG (Register 2-15)
- RSTHIREG (Register 2-16)
- FLCREG (Register 2-17)
- PFCREG (Register 2-18)
- SYNCREG (Register 2-19)
- RSTSREG (Register 2-21)
- OOKCREG (Register 2-22)
- SYNCP31REG (Register 2-23)
- SYNCP23REG (Register 2-24)
- SYNCP15REG (Register 2-25)
- SYNCP07REG (Register 2-26)
- PLOADREG (Register 2-29)
- NADDSREG (Register 2-30)
- PKTCREG (Register 2-31)
- FCRCREG (Register 2-32)
3.12 Initialization

Certain control register values must be initialized for basic operations of the MRF89XA. These values differ from the POR values and provide improved operational parameters. These settings are normally made once after a Reset. After initialization, the other features of the MRF89XA device can be configured based on the application. Accessing a register is implied as a command to the MRF89XA device through the SPI port.

The steps to initialize the MRF89XA using the control registers are as follows:

1. In the GCONREG register:
   a) Set the Chip Mode (CMOD<2:0>), Frequency Band (FBS<1:0>) and VCO Trim (VCOT<1:0>) bits.
   b) Program the Frequency band.
   c) Set the Trim bits to appropriately tune in the VCO.

2. In the DMODREG register:
   a) Select the Modulation Type using the MODSEL<1:0> bits.
   b) Enable DATA mode for Transmission using the DMODE0 and DMODE1 bits.
   c) Select gain for IF chain using the IFGAIN<1:0> bits.
   d) In the FDEVREG register, program the Frequency Deviation bits (FDVAL<7:0>).

3. In the BRSREG register, program the Bit Rate using the BRVAL<6:0> bits.

4. In the FLTHREG register, set the Floor Threshold for OOK using the FTOVAL<7:0> bits.

5. In the FIFOCREG register, configure the FIFO Size and FIFO Threshold using theFSIZE<1:0> and FTINT<5:0> bits.

6. In the PACREG register, configure the Power Amplifier Ramp Control using the PARC<1:0> bits.

7. In the FTXRXIREG register:
   a) Configure the RX interrupts for IRQ0 and IRQ1 using the IRQ0RXS<1:0> and IRQ1RXS<1:0> bits.
   b) Configure the TX interrupts for IRQ1 using the IRQ1TX bit.

8. In the FTPRIREG register:
   a) Configure the TX interrupts for IRQ0 using the IRQ0TXST bit.
   b) Enable PLL Lock for interrupt on IRQ1 using the LENPLL bit.

9. In the RSTHIREG, program the RSSI Threshold value for interrupt request using the RTIVAL<7:0> bits.

10. In the FILCREG register, enable the Passive Filter using the PASFILV<3:0> bits.

11. Configure RX parameters:
   a) Enable Passive Filter with value as set in step 11.
   b) Set $f_c$ and $f_o$.
   c) Enable SYNC and Set SYNC Word, Size, Length and Tolerance.
   d) Set configuration bytes for OOK Threshold from OOKCREG

12. In the SYNCREG register, set SYNCWSZ<1:0> = 11 for 32-bit SYNC word.

13. Configure TX parameters:
   a) Change or Reset $f_c$.
   b) In the TXCONREG register, enable TX and its transmit power using the TXPOLFV<3:0> and TXOPVAL<2:0> bits.

14. In the CLKOUTREG register, configure the Clock Settings using the CLKOCNTRL and CLKOFOREQ<4:0> bits.

15. Configure the Packet Frame parameters in the PLOADREG, NADDSREG, PKTCREG and FCRCREG registers:
   a) Enable Manchester Encoding
   b) Set packet format and length of the packet
   c) Set Node local address
   d) Program preamble variables
   e) Configure CRC parameters
   f) Enable Address Filtering

16. In the FCRCREG register, enable FIFO write access using the FRWAXS bit.

Note 1: Program registers 0x00 - 0x1F with appropriate settings. (General Configuration Parameters, IRQ Parameters, Packet Parameters).

2: Clear the PLL Lock flag by setting the LSTSPLL bit (FTPRIREG 0x0E<1>) to '1'.

3: Program CMOD bits (GCONREG 0x00 <7:5>) to '0b010 Frequency Synthesizer mode.

4: Verify the PLL lock flag through the LSTSPPL bit (FTPRIREG 0x0E<1>). If LSTSPPL = 1, it implies that the MRF89XA is ready to operate at the frequency indicated by the Ri/Pi/Si register set.

5: Program the CMOD bits (GCONREG 0x00 <7:5>) to '0b001 Standby mode.'
3.13 Battery Power Management Configuration Values

Battery life can be greatly extended in MRF89XA applications where transmissions from field nodes are infrequent, or network communications can be concentrated in periodic time slots. For example, field nodes in many wireless alarm systems report operational status a few times a day, and can otherwise sleep unless an alarm condition occurs. Sensor networks that monitor parameters that change relatively slowly, such as air and soil temperature in agricultural settings, switching lights ON/OFF, only need to transmit updates a few times per an hour.

At room temperature, the MRF89XA draws a maximum of 1 µA in Sleep mode, with a typical value of 100 nA. To achieve minimum Sleep mode current, the CSCON pin (pin 14), SDI pin (pin 17) and SCK pin (pin 18) must be held logic low, while the CSDAT pin (pin 15) and SDO pin (pin 16) must be held logic high.

The MRF89XA can go from Sleep mode through Stand-by mode and Synthesizer mode to Transmit (or Receive) mode in less than 6 ms. For configuring and driving the device different operating modes refer to Table 2-3. At a data rate of 33.33 kbps, a 32-byte packet with a 4-byte preamble and a 4-byte start pattern takes about 10 ms to transmit. Assume that the MRF89XA then switches to Receive mode for one second to listen for a response and returns to Sleep mode. On the basis of reporting every six hours, the ON to Sleep duty cycle is about 1:21,259, greatly extending battery life over continuous transmit-receive or even stand-by operation.

The required timing accuracy for the microcontrollers in a sleep-cycled application depends on several factors:

- The required “time-stamp” accuracy of data reported by sleeping field nodes. R-C Sleep mode timers built into many microcontrollers have a tolerance of ±20% or more. For applications that require more accurate time-stamping, many microcontrollers can run on a watch crystal during Sleep mode and achieve time-stamp accuracies better than one second per 24 hours.
- If the base station and any routing nodes present in a network must sleep cycle in addition to the field nodes. Watch crystal control will usually be needed to keep all nodes accurately synchronized to the active time slots.
- If the base station and any routing nodes present in a network can operate continuously (AC powered, solar charged batteries), and a loose time stamp accuracy is OK, the microcontrollers in sleeping field nodes can usually operate from internal low-accuracy R-C timers.

Note: Many host microcontrollers cannot be operated from the MRF89XA buffered clock output if sleep cycling is planned. In Sleep mode, the MRF89XA buffered clock output is disabled, which will disable the microcontroller unless it is capable of automatically switching to an internal clock source when external clocking is lost.

Therefore, as previously mentioned, Sleep mode is the lowest power consumption mode in which the clock and all functional blocks of the device are disabled. In case of an interrupt, the device wakes up, switches to Active mode and an interrupt signal generated on the IRQ pin indicates the change in state to the host microcontroller. The source of the interrupt can be determined by reading the status word of the device.

To reduce current consumption, the MRF89XA should be placed in the low-power consuming Sleep mode. In Sleep mode, the 12.8 MHz main oscillator is turned OFF, disabling the RF and baseband circuitry. Data is retained in the control and FIFO registers and the transceiver is accessible through the SPI port. The MRF89XA will not enter Sleep mode if any interrupt remains active, regardless of the state of the CLKOCNTRL bit (CLKOUTREG<7>). This way, the microcontroller can always have a clock signal to process the interrupt. To prevent high-current consumption, which results in shorter battery life, it is highly recommended to process and clear interrupts before entering Sleep mode. The functions which are not necessary should be turned off to avoid unwanted interrupts. To minimize current consumption, the MRF89XA supports different power-saving modes, along with an integrated wake-up timer.

When switching from Sleep mode to Stand-by mode, the crystal oscillator will be active for no more than 5 ms. Switching from Stand-by mode to Synthesizer mode, the PLL will lock in less than 0.5 ms. PLL lock can be monitored on the PLOCK pin (pin 23) of the MRF89XA. The radio can then be switched to either Transmit or Receive mode. When switching from any other mode back to Sleep mode, the device will drop to its Sleep mode current in less than 1 ms.
To make the MRF89XA device enter into Sleep mode, certain control register values must be initialized. The sequence to program the control registers for entering into Sleep mode and Wake-up modes are as follows:

For Sleep mode:
1. Check the IRQ bit status
2. Handle Interrupts
3. Configure the GCONREG register
4. Set/Reset CLKOUT in the CLKOUTREG register

**EXAMPLE 3-1: TO PUT THE MRF89XA INTO SLEEP MODE**

Set CMOD<2:0> (GCONREG<2:0>) = 0

The MRF89XA device can wake up from any interrupt activity.

For Wake-up mode perform any one the following task:
- Enter in TX/RX mode
- Enable CLKOUT
- Set the INT pin

**EXAMPLE 3-2: TO WAKE THE MRF89XA FROM SLEEP MODE**

Set CMOD<2:0> (GCONREG<2:0>) = 1

### 3.13.1 POWER-SAVING MODE REGISTERS

The registers associated with power-saving modes are:
- GCONREG (Register 2-1)
- DMODREG (Register 2-2)
- FDEVREG (Register 2-3)
- BRSREG (Register 2-4)
- FTXRXIREG (Register 2-14)
- FTPRIREG (Register 2-15)
- CLKOUTREG (Register 2-28)
4.0 APPLICATION DETAILS

4.1 Application Schematic

An application circuit schematic of the MRF89XA with a matching circuit of the SAW filter and antenna is illustrated in Figure 4-1. This application design (that is, schematics and BOM) can be replicated in the final application board for optimum performance.

FIGURE 4-1: APPLICATION CIRCUIT SCHEMATIC

Note: Component values for C11, C12, and L6 depend on antenna impedance.
4.1 RF Transmitter Matching

The optimum load for the RF port at a given frequency band is listed in Table 4-1. These load values in the table are expected by the RF port pins to have as an antenna load for maximum power transfer. For all antenna applications, an RF choke inductor (L2) must be included during transmission because the RF outputs are of open-collector type.

4.2 Antenna Components

The MRF89XA is single-ended and has an unbalanced input and output impedance close to 30-j25. Therefore, it only requires a matching circuit to the SAW filter and antenna. The C11, C12, and L6 are part of the matching network these components make for the antenna circuit. L1, C4, and C5 are tuned to provide that impedance (30+j25) to the RFIO pin. In this case, the transceiver will be able to transfer all power toward the antenna. This impedance is called Optimum Load Impedance. L2 is a RF choke inductor. L3 and L4 are basically VCO inductors. The details are shown in Figure 4-1.

<table>
<thead>
<tr>
<th>Band</th>
<th>FL1</th>
<th>C5</th>
<th>C4</th>
<th>L1</th>
</tr>
</thead>
<tbody>
<tr>
<td>868 MHz</td>
<td>TA0801A</td>
<td>1.8 pF</td>
<td>22 pF</td>
<td>8.2 nH</td>
</tr>
<tr>
<td>915 MHz</td>
<td>TA0281A</td>
<td>1.8 pF</td>
<td>30 pF</td>
<td>10 nH</td>
</tr>
</tbody>
</table>

Note 1: The SAW filter can be of EPCOS (B3717 and B3588) or Taisaw (TA0801A and TA0281A) for 868 MHz and 915 MHz respectively with matching components remaining the same as shown in Figure 4-1 and Table 4-1.

4.3 SAW FILTER

FL1 is a SAW filter. While in Transmitting mode, the SAW filter is used to suppress the harmonics. While in Receiving mode, the SAW filter is used to reject the image frequencies and out-of-band interfering signals.

4.3.1 SAW FILTER PLOT

Figure 4-2 and Figure 4-3 illustrates the plots of the SAW filter used in the application circuit. The plots shown are representative. For exact specifications, refer to the SAW Filter manufacturer data sheet.
FIGURE 4-2: 868 MHz SAW FILTER PLOT

FIGURE 4-3: 915 MHz SAW FILTER PLOT
4.4 POWER AMPLIFIER

The Power Amplifier (PA) integrated in the MRF89XA operates under a regulated voltage supply of 1.8V. The external RF choke inductor is biased by an internal regulator output made available on the PARS pin (pin 29). These features help PA output power to be consistent over the power supply range. This is important for applications that allow predictable RF performance and battery life.

4.4.1 OPTIMUM LOAD IMPEDANCE

As the PA and the LNA front-ends in the MRF89XA share the same input/output pin, they are internally matched to approximately 50Ω. Figure 4-4 illustrates optimum load impedance of RFIO through an impedance chart.

**Note:** Refer to Section 4.7, Bill of Materials for an optimized PA load setting.
4.4.2 SUGGESTED PA BIASING AND MATCHING

The recommended PA bias and matching circuit is illustrated in Figure 4-5.

FIGURE 4-5: RECOMMENDED PA BIASING AND OUTPUT MATCHING

Refer to Section 4.7, Bill of Materials for the optimized matching arrangement for each frequency band.

4.4.3 COMMON INPUT AND OUTPUT FRONT-END

The Receiver and Transmitter share the same RFIO pin (pin 31). Figure 4-6 illustrates the configuration of the common RF front-end.

In Transmit mode, the PA and PA regulator are active, with the voltage on the PARS pin equal to the nominal voltage of the regulator (1.8V). The external inductance is used to bias the PA.

In Receive mode, both the PA and PA regulator are OFF and PARS is tied to ground. The RF choke inductor is then used to bias the LNA.

FIGURE 4-6: FRONT-END DESCRIPTION
4.4.4 PLL LOOP FILTER

To adequately reject spurious components arising from the comparison frequency FCOMP, an external second order loop filter is used. Figure 4-7 illustrates the loop filter circuit.

The recommendations made in Section 3.2.4.1, PLL Requirements and the loop filter proposed in the application schematic’s BOM in Section 4.7, Bill of Materials can be used. The loop filter settings are frequency band independent and are hence relevant to all implementations of the MRF89XA.

4.4.5 VOLTAGE CONTROLLED OSCILLATOR (VCO)

The integrated VCO requires only two external tank circuit inductors. As the input is differential, the two inductors should have the same nominal value. The performance of these components is important for both the phase noise and the power consumption of the PLL.

It is recommended that a pair of high Q factor inductors is selected. These should be mounted orthogonally to other inductors (in particular the PA choke) to reduce spurious coupling between the PA and VCO. These measures may reduce radiated pulling effects and undesirable transient behavior, thus minimizing spectral occupancy. Ensuring a symmetrical layout of the VCO inductors will improve PLL spectral purity.

4.5 VDD Line Filtering

During the Reset event (caused by power-on, a glitch on the supply line or a software Reset), the Vdd line should be kept clean. Noise or a periodic disturbing signal superimposed on the supply voltage may prevent the device from getting out of the Reset state. To avoid this, adequate filters should be made available on the power supply lines to keep the distorting signal level below 100-150 mV peak-to-peak, in the DC to 50 kHz range for 200 ms, from Vdd ramp start. The usage of regulators or switching power supplies may sometimes introduce switching noise on the Vdd line, hence follow the power supply manufacturer’s recommendations on how to decrease the ripple of regulator IC and/or how to shift the switching frequency.

4.6 Crystal Specification and Selection Guidelines

Table 4-2 lists the crystal resonator specification for the crystal reference oscillator circuit of the MRF89XA. This specification covers the full range of operation of the MRF89XA and is used in the application schematic (for more information, see Section 4.7, Bill of Materials).

<table>
<thead>
<tr>
<th>Name</th>
<th>Description</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>f_{xtal}</td>
<td>Nominal frequency</td>
<td>9</td>
<td>12.800</td>
<td>15</td>
<td>MHz</td>
</tr>
<tr>
<td>CLOAD</td>
<td>Load capacitance for f_{xtal}</td>
<td>10</td>
<td>15</td>
<td>16.5</td>
<td>pF</td>
</tr>
<tr>
<td>Rm</td>
<td>Motional resistance</td>
<td>—</td>
<td>—</td>
<td>100</td>
<td>Ohms</td>
</tr>
<tr>
<td>Co</td>
<td>Shunt capacitance</td>
<td>1</td>
<td>—</td>
<td>7</td>
<td>pF</td>
</tr>
<tr>
<td>\Delta f_{xtal}</td>
<td>Calibration tolerance at 25+/-3°C</td>
<td>-15</td>
<td>—</td>
<td>+15</td>
<td>ppm</td>
</tr>
<tr>
<td>\Delta f_{xtal}(\Delta T)</td>
<td>Stability over temperature range [-40°C; +85°C]</td>
<td>-20</td>
<td>—</td>
<td>+20</td>
<td>ppm</td>
</tr>
<tr>
<td>\Delta f_{xtal}(\Delta t)</td>
<td>Aging (first year)</td>
<td>5</td>
<td>—</td>
<td>5</td>
<td>ppm</td>
</tr>
</tbody>
</table>

Note: The initial frequency tolerance, temperature stability and ageing performance should be chosen in accordance with the target operating temperature range and the receiver bandwidth selected.
## 4.7 Bill of Materials

<table>
<thead>
<tr>
<th>Designator</th>
<th>Value</th>
<th>Description</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>0.047 μF</td>
<td>Capacitor, Ceramic, 10V, +/-10%, X7R, SMT 0402</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C2</td>
<td>0.22 μF</td>
<td>Capacitor, Ceramic, 16V, +/-10%, X7R, SMT 0402</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C3</td>
<td>1 μF</td>
<td>Capacitor, Ceramic, 6.3V, +/-10%, X5R, SMT 0603</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C4</td>
<td>22 pF</td>
<td>Capacitor, Ceramic, 50V, +/-5%, UHI-Q NP0, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>C5</td>
<td>1.8 pF</td>
<td>Capacitor, Ceramic, 50V, +/-0.1 pF, UHI-Q NP0, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>C7</td>
<td>33 pF</td>
<td>Capacitor, Ceramic, 50V, +/-5%, C0G, SMT 0402</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C8</td>
<td>0.1 μF</td>
<td>Capacitor, Ceramic, 16V, +/-10%, C0G, SMT 0402</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C9</td>
<td>680 pF</td>
<td>Capacitor, Ceramic, 50V, +/-5%, C0G, SMT 0402</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C10</td>
<td>0.01 μF</td>
<td>Capacitor, Ceramic, 16V, +/-10%, X7R, SMT 0402</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C11</td>
<td>4.3 pF</td>
<td>Capacitor, Ceramic, 50V, +/-0.1 pF, UHI-Q NP0, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>C12</td>
<td>1.5 pF</td>
<td>Capacitor, Ceramic, 50V, +/-0.1 pF, UHI-Q NP0, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>FL1</td>
<td>TA0801A</td>
<td>SAW Filter</td>
<td>Taisaw</td>
</tr>
<tr>
<td>L1</td>
<td>8.2 nH</td>
<td>Inductor, Ceramic, +/-5%, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>L2</td>
<td>100 nH</td>
<td>Inductor, Ceramic, +/-5%, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>L3</td>
<td>6.8 nH</td>
<td>Inductor, Wirewound, +/-5%, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>L4</td>
<td>6.8 nH</td>
<td>Inductor, Wirewound, +/-5%, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>L6</td>
<td>10 nH</td>
<td>Inductor, Ceramic, +/-5%, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>R1</td>
<td>1 ohm</td>
<td>Resistor, 1%, +/-100 ppm/C, SMT 0402</td>
<td>Vishay/Dale</td>
</tr>
<tr>
<td>R2</td>
<td>100K ohm</td>
<td>Resistor, 5%, +/-100 ppm/C, SMT 0402</td>
<td>Yageo</td>
</tr>
<tr>
<td>R3</td>
<td>6.8K ohm</td>
<td>Resistor, 1%, +/-100 ppm/C, SMT 0402</td>
<td>Yageo</td>
</tr>
<tr>
<td>R4</td>
<td>0 ohm</td>
<td>Resistor, SMT 0402</td>
<td>Yageo</td>
</tr>
<tr>
<td>R5</td>
<td>—</td>
<td>Not Populated</td>
<td>—</td>
</tr>
<tr>
<td>U1</td>
<td>MRF89XA</td>
<td>Transceiver</td>
<td>Microchip Technology Inc.</td>
</tr>
<tr>
<td>X1</td>
<td>12.800 MHz</td>
<td>Crystal, +/-10 ppm, 15 pF, ESR 100 ohms, SMT 5x3.2mm</td>
<td>—</td>
</tr>
</tbody>
</table>

**Note:** For battery powered applications, a high value capacitance should be implemented in parallel with C1 (typically 10 μF) to offer a low impedance voltage source during startup sequences.
### TABLE 4-4: MRF89XA APPLICATION SCHEMATIC BILL OF MATERIALS FOR 915 MHZ

<table>
<thead>
<tr>
<th>Designator</th>
<th>Value</th>
<th>Description</th>
<th>Manufacturer</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>0.047 μF</td>
<td>Capacitor, Ceramic, 10V, +/-10%, X7R, SMT 0402</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C2</td>
<td>0.22 μF</td>
<td>Capacitor, Ceramic, 16V, +/-10%, X7R, SMT 0402</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C3</td>
<td>1 μF</td>
<td>Capacitor, Ceramic, 6.3V, +/-10%, X5R, SMT 0603</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C4</td>
<td>30 pF</td>
<td>Capacitor, Ceramic, 25V, +/-5%, UHI-Q NP0, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>C5</td>
<td>1.8 pF</td>
<td>Capacitor, Ceramic, 50V, +/-0.1 pF, UHI-Q NP0, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>C7</td>
<td>33 pF</td>
<td>Capacitor, Ceramic, 50V, +/-5%, C0G, SMT 0402</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C8</td>
<td>0.1 μF</td>
<td>Capacitor, Ceramic, 16V, +/-10%, C0G, SMT 0402</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C9</td>
<td>680 pF</td>
<td>Capacitor, Ceramic, 50V, +/-5%, C0G, SMT 0402</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C10</td>
<td>0.01 μF</td>
<td>Capacitor, Ceramic, 16V, +/-10%, X7R, SMT 0402</td>
<td>Murata Electronics North America</td>
</tr>
<tr>
<td>C11</td>
<td>1.0 pF</td>
<td>Capacitor, Ceramic, 50V, +/-0.1 pF, UHI-Q NP0, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>C12</td>
<td>0.9 pF</td>
<td>Capacitor, Ceramic, 50V, +/-0.1 pF, UHI-Q NP0, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>FL1</td>
<td>TA0281A</td>
<td>SAW Filter</td>
<td>Taisaw</td>
</tr>
<tr>
<td>L1</td>
<td>10 nH</td>
<td>Inductor, Ceramic, +/-5%, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>L2</td>
<td>100 nH</td>
<td>Inductor, Ceramic, +/-5%, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>L3</td>
<td>5.6 nH</td>
<td>Inductor, Wirewound, +/-5%, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>L4</td>
<td>5.6 nH</td>
<td>Inductor, Wirewound, +/-5%, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>L6</td>
<td>10 nH</td>
<td>Inductor, Ceramic, +/-5%, SMT 0402</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>R1</td>
<td>1 ohm</td>
<td>Resistor, 1%, +/-100 ppm/C, SMT 0402</td>
<td>Vishay/Dale</td>
</tr>
<tr>
<td>R2</td>
<td>100K ohm</td>
<td>Resistor, 5%, +/-100 ppm/C, SMT 0402</td>
<td>Yageo</td>
</tr>
<tr>
<td>R3</td>
<td>6.8K ohm</td>
<td>Resistor, 1%, +/-100 ppm/C, SMT 0402</td>
<td>Yageo</td>
</tr>
<tr>
<td>R4</td>
<td>—</td>
<td>Not Populated</td>
<td>—</td>
</tr>
<tr>
<td>R5</td>
<td>0 ohm</td>
<td>Resistor, SMT 0402</td>
<td>Yageo</td>
</tr>
<tr>
<td>U1</td>
<td>MRF89XA</td>
<td>Transceiver</td>
<td>Microchip Technology Inc.</td>
</tr>
<tr>
<td>X1</td>
<td>12.800 MHz</td>
<td>Crystal, +/-10 ppm, 15 pF, ESR 100 ohms, SMT 5x3.2mm</td>
<td>—</td>
</tr>
</tbody>
</table>

**Note:** For battery powered applications, a high value capacitance should be implemented in parallel with C1 (typically 10 μF) to offer a low impedance voltage source during startup sequences.
4.8 General PCB Layout Design

The following guidelines can be used to assist in high-frequency PCB layout design.

The printed circuit board is usually comprised of two or four basic FR4 layers.

The two-layer printed circuit board has mixed signal/power/RF and common ground routed in both the layers (see Figure 4-8).

The four-layer printed circuit board (see Figure 4-9) is comprised of the following layers:

- Signal layout
- RF ground
- Power line routing
- Common ground

The following guidelines explain the requirements of the previously mentioned layers:

- It is important to keep the original PCB thickness, because any change will affect antenna performance (see total thickness of dielectric) or microstrip lines’ characteristic impedance.
- For good transmit and receive performance, the trace lengths at the RF pins must be kept as short as possible. Using small, surface mount components (in 0402/0603 package) yields good performance and keeps the RF circuit small. RF connections should be short and direct.
- Except for the antenna layout, avoid sharp corners because they can act as an antenna. Round corners will eliminate possible future EMI problems.
- Digital lines are prone to be very noisy when handling periodic waveforms and fast clock/switching rates. Avoid RF signal layout close to any of the digital lines.
- A VIA filled ground patch underneath the IC transceiver is mandatory.
- The power supply must be distributed to each pin in a star topology, and low-ESR capacitors must be placed at each pin for proper decoupling noise.

- Thorough decoupling on each power pin is beneficial for reducing in-band transceiver noise, particularly when this noise degrades performance. Usually, low value caps (27-47 pF) combined with large value caps (100 nF) will cover a large spectrum of frequency.
- Passive component (inductors) should be in the high-frequency category and the Self-Resonant Frequency (SRF) should be at least two times higher than the operating frequency.
- The additional trace length affects the crystal oscillator by adding parasitic capacitance to the overall load of the crystal. To minimize this, place the crystal as close as possible to the RF device.
- Setting short and direct connections between the components on board minimizes the effects of “frequency pulling” that might be introduced by stray capacitance. It even allows the internal load capacitance of the chip to be more effective in properly loading the crystal oscillator circuit.
- Long run tracks of clock signal may radiate and cause interference. This can degrade receiver performance and add harmonics or unwanted modulation to the transmitter.
- Keep clock connections as short as possible and surround the clock trace with an adjacent ground plane pour. Pouring helps in reducing any radiation or crosstalk due to long run traces of the clock signal.
- Low value decoupling capacitors, typically 0.01-0.1 µF, should be placed for VDD of the chip and for bias points of the RF circuit.
- High value decoupling capacitors, typically 2.2-10 µF, should be placed at the point where power is applied to the PCB.
- Power supply bypassing is necessary. Poor bypassing contributes to conducted interference, which can cause noise and spurious signals to couple into the RF sections, significantly reducing the performance.

**FIGURE 4-8: TWO BASIC COPPER FR4 LAYERS**

![Signal/Power/RF and Common Ground](image)

**Dielectric Constant = 4.5**

![Signal/Power/RF and Common Ground](image)
FIGURE 4-9: FOUR BASIC COPPER FR4 LAYERS

- Signal Layout
- Dielectric Constant = 4.5
- RF Ground
- Dielectric Constant = 4.5
- Power Line Routing
- Dielectric Constant = 4.5
- Ground
5.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

- Ambient temperature under bias.............................................................................................................................................. -40°C to +85°C
- Storage temperature .................................................................................................................................................................... -55°C to +125°C
- Lead temperature (soldering, max 10s)......................................................................................................................... +260°C
- Voltage on VDD with respect to VSS ........................................................................................................................................ -0.3V to 6V
- Voltage on any combined digital and analog pin with respect to VSS (except RFIO and VDD) ........................................ -0.3V to (VDD + 0.3V)
- Voltage on open-collector outputs (RFIO)(*).......................................................................................................................... -0.3V to 3.7V
- Input current into pin (except VDD and VSS)............................................................................................................................ -25 mA to 25 mA
- Electrostatic discharge with human body model .................................................................................................................. 1000V

Note 1: At maximum, voltage on RFIO cannot be higher than 6V.

NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
5.1 ESD Notice

The MRF49XA is a high-performance radio frequency device, it satisfies:

- Class II of the JEDEC standard JESD22-A114-B (Human Body Model) of 2 KV, except on all of the RF pins where it satisfies Class 1A.
- Class III of the JEDEC standard JESD22-C101C (Charged Device Model) on all pins.

It should thus be handled with all the necessary ESD precautions to avoid any permanent damage.

### TABLE 5-1: RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ambient Operating Temperature</td>
<td>-40</td>
<td>—</td>
<td>+85</td>
<td>°C</td>
<td>—</td>
</tr>
<tr>
<td>Supply Voltage for RF, Analog and Digital Circuits</td>
<td>2.1</td>
<td>—</td>
<td>3.6</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>Supply Voltage for Digital I/O</td>
<td>2.1</td>
<td>—</td>
<td>3.6</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>Input High Voltage (VIH)</td>
<td>0.5 * VDD</td>
<td>—</td>
<td>VDD + 0.3</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>Input Low Voltage (VIL)</td>
<td>-0.3V</td>
<td>—</td>
<td>0.2 * VDD</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>DC Voltage on Open Collector Outputs (RFIO)</td>
<td>VDD – 1.5</td>
<td>—</td>
<td>VDD + 1.5</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>DC Peak Voltage on Open Collector Outputs (IO)</td>
<td>VDD – 1.5</td>
<td>—</td>
<td>VDD + 1.5</td>
<td>V</td>
<td>—</td>
</tr>
</tbody>
</table>

**Note 1:** At minimum, VDD – 1.5V should not be lower than 1.8V.

**Note 2:** At maximum, VDD + 1.5V should not be higher than 3.7V.

### TABLE 5-2: CURRENT CONSUMPTION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Chip Mode</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDDSSL</td>
<td>Sleep</td>
<td>—</td>
<td>0.1</td>
<td>2</td>
<td>µA</td>
<td>Sleep clock disabled, all blocks disabled</td>
</tr>
<tr>
<td>IDDST</td>
<td>Idle</td>
<td>—</td>
<td>—</td>
<td>65</td>
<td>80</td>
<td>µA Oscillator and baseband enabled</td>
</tr>
<tr>
<td>IDDFS</td>
<td>Frequency Synthesizer</td>
<td>—</td>
<td>1.3</td>
<td>1.7</td>
<td>mA</td>
<td>Frequency synthesizer running</td>
</tr>
<tr>
<td>IDDTX</td>
<td>TX</td>
<td>—</td>
<td>—</td>
<td>25</td>
<td>30</td>
<td>mA Output power = +10 dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>16</td>
<td>21</td>
<td>mA</td>
<td>Output power = +1 dBm(1)</td>
</tr>
<tr>
<td>IDDRX</td>
<td>RX</td>
<td>—</td>
<td>—</td>
<td>3.0</td>
<td>3.5</td>
<td>mA</td>
</tr>
</tbody>
</table>

**Note 1:** Guaranteed by design and characterization.

**Note 2:** Crystal CLOAD = 10 pF, C0 = 2.5 pF, RM = 15Ω.

**Note 3:** Measurement Conditions: Temp = 25°C, VDD = 3.3V, crystal frequency = 12.8 MHz, carrier frequency = 868 or 915 MHz, modulation FSK, data rate = 25 kbps, fdev = 50 kHz, fc = 100 kHz, unless otherwise specified.
### TABLE 5-3: DIGITAL I/O PIN INPUT SPECIFICATIONS(1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td></td>
<td></td>
<td>0.2 * VDD</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td></td>
<td></td>
<td>—</td>
<td>V</td>
<td>—</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Low Leakage Current(2)</td>
<td>-0.5</td>
<td>—</td>
<td>0.5</td>
<td>µA</td>
<td>VIL = 0V</td>
</tr>
<tr>
<td>IIH</td>
<td>Input High Leakage Current</td>
<td>-0.5</td>
<td></td>
<td>0.5</td>
<td>µA</td>
<td>VIH = VDD, VDD = 3.7</td>
</tr>
<tr>
<td>VOL</td>
<td>Digital Low Output Voltage</td>
<td></td>
<td></td>
<td>0.1 * VDD</td>
<td>—</td>
<td>IOL = 1 mA</td>
</tr>
<tr>
<td>VOH</td>
<td>Digital Low Output</td>
<td>0.9 * VDD</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>IOH = -1 mA</td>
</tr>
</tbody>
</table>

**Note 1:** Measurement Conditions: TA = 25°C, VDD = 3.3V, crystal frequency = 12.8 MHz, unless otherwise specified.

**Note 2:** Negative current is defined as the current sourced by the pin.

**Note 3:** On Pin 10 (OSC1) and 11 (OSC2), maximum voltages of 1.8V can be applied.

### TABLE 5-4: PLL PARAMETERS AC CHARACTERISTICS(1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>FRO</td>
<td>Frequency Ranges</td>
<td>863</td>
<td>870</td>
<td>902</td>
<td>MHz</td>
<td>Programmable but requires specific BOM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>902</td>
<td>928</td>
<td>950</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>950</td>
<td>960</td>
<td></td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>BRFSK</td>
<td>Bit Rate (FSK)</td>
<td>1.56</td>
<td>200</td>
<td></td>
<td>kbps</td>
<td>NRZ</td>
</tr>
<tr>
<td>BROOK</td>
<td>Bit Rate (OOK)</td>
<td>1.56</td>
<td>32</td>
<td></td>
<td>kbps</td>
<td>NRZ</td>
</tr>
<tr>
<td>FDFSFK</td>
<td>Frequency Deviation (FSK)</td>
<td>33</td>
<td>50</td>
<td>200</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>FXTAL</td>
<td>Crystal Oscillator Frequency</td>
<td>9</td>
<td>12.8</td>
<td>15</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>FSSTP</td>
<td>Frequency Synthesizer Step</td>
<td>—</td>
<td>2</td>
<td>—</td>
<td>kHz</td>
<td>Variable, depending on the frequency</td>
</tr>
<tr>
<td>TSOSC</td>
<td>Oscillator Wake-up Time</td>
<td>—</td>
<td>1.5</td>
<td>5</td>
<td>ms</td>
<td>From Sleep mode(1)</td>
</tr>
<tr>
<td>TSFS</td>
<td>Frequency Synthesizer Wake-up Time; at most, 10 kHz away from the Target</td>
<td>—</td>
<td>500</td>
<td>800</td>
<td>µs</td>
<td>From Stand-by mode</td>
</tr>
<tr>
<td>TSHOP</td>
<td>Frequency Synthesizer Hop Time; at most, 10 kHz away from the Target</td>
<td>—</td>
<td>180</td>
<td>—</td>
<td>µs</td>
<td>200 kHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>200</td>
<td>—</td>
<td>µs</td>
<td>1 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>250</td>
<td>—</td>
<td>µs</td>
<td>5 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>260</td>
<td>—</td>
<td>µs</td>
<td>7 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>290</td>
<td>—</td>
<td>µs</td>
<td>12 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>320</td>
<td>—</td>
<td>µs</td>
<td>20 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>340</td>
<td>—</td>
<td>µs</td>
<td>27 MHz step</td>
</tr>
</tbody>
</table>

**Note 1:** Guaranteed by design and characterization
### TABLE 5-5: RECEIVER AC CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSF</td>
<td>Sensitivity (FSK)</td>
<td>—</td>
<td>-107</td>
<td>—</td>
<td>dBm</td>
<td>— dBm 869 MHz, BR = 25 kbps, $f_{dev} = 50$ kHz, $f_c = 100$ kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>-103</td>
<td>—</td>
<td>dBm</td>
<td>— dBm 869 MHz, BR = 66.7 kbps, $f_{dev} = 100$ kHz, $f_c = 200$ kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>-105</td>
<td>—</td>
<td>dBm</td>
<td>— dBm 915 MHz, BR = 25 kbps, $f_{dev} = 50$ kHz, $f_c = 100$ kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>-101</td>
<td>—</td>
<td>dBm</td>
<td>— dBm 915 MHz, BR = 66.7 kbps, $f_{dev} = 100$ kHz, $f_c = 200$ kHz</td>
</tr>
<tr>
<td>RSO</td>
<td>Sensitivity (OOK)</td>
<td>—</td>
<td>-113</td>
<td>—</td>
<td>dBm</td>
<td>— dBm 869 MHz, 2 kbps NRZ $f_{f_c} - f_0 = 50$ kHz, $f_0 = 50$ kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>-106</td>
<td>—</td>
<td>dBm</td>
<td>— dBm 869 MHz, 16.7 kbps NRZ $f_{f_c} - f_0 = 100$ kHz, $f_0 = 100$ kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>-111</td>
<td>—</td>
<td>dBm</td>
<td>— dBm 915 MHz, 2 kbps NRZ $f_{f_c} - f_0 = 50$ kHz, $f_0 = 50$ kHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>-105</td>
<td>—</td>
<td>dBm</td>
<td>— dBm 915 MHz, 16.7 kbps NRZ $f_{f_c} - f_0 = 100$ kHz, $f_0 = 100$ kHz</td>
</tr>
<tr>
<td>CCR</td>
<td>Co-Channel Rejection</td>
<td>—</td>
<td>-12</td>
<td>—</td>
<td>dBc</td>
<td>— dBc Modulation as wanted signal</td>
</tr>
<tr>
<td>ACR</td>
<td>Adjacent Channel Rejection</td>
<td>—</td>
<td>27</td>
<td>—</td>
<td>dB</td>
<td>— dB Offset = 300 kHz, unwanted tone is not modulated</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>52</td>
<td>—</td>
<td>dB</td>
<td>— dB Offset = 600 kHz, unwanted tone is not modulated</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>57</td>
<td>—</td>
<td>dB</td>
<td>— dB Offset = 1.2 MHz, unwanted tone is not modulated</td>
</tr>
<tr>
<td>BI</td>
<td>Blocking Immunity</td>
<td>—</td>
<td>-48</td>
<td>—</td>
<td>dBm</td>
<td>— dBm Offset = 1 MHz, unmodulated</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>-37</td>
<td>—</td>
<td>dBm</td>
<td>— dBm Offset = 2 MHz, unmodulated, no SAW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>-33</td>
<td>—</td>
<td>dBm</td>
<td>— dBm Offset = 10 MHz, unmodulated, no SAW</td>
</tr>
<tr>
<td>RXBWF</td>
<td>Receiver Bandwidth in FSK Mode$^{(2)}$</td>
<td>50</td>
<td>—</td>
<td>250</td>
<td>kHz</td>
<td>Single side BW, Polyphase Off</td>
</tr>
<tr>
<td>RXBUW</td>
<td>Receiver Bandwidth in OOK Mode$^{(2)}$</td>
<td>50</td>
<td>—</td>
<td>400</td>
<td>kHz</td>
<td>Single side BW, Polyphase On</td>
</tr>
<tr>
<td>ITP3</td>
<td>Input Third Order Intercept Point</td>
<td>—</td>
<td>-28</td>
<td>—</td>
<td>dBm</td>
<td>— dBm Interferers at 1 MHz and 1.950 MHz offset</td>
</tr>
<tr>
<td>TSRWF</td>
<td>Receiver Wake-up Time</td>
<td>—</td>
<td>280</td>
<td>500</td>
<td>µs</td>
<td>— µs From FS to RX ready</td>
</tr>
<tr>
<td>TSRWS</td>
<td>Receiver Wake-up Time</td>
<td>—</td>
<td>600</td>
<td>900</td>
<td>µs</td>
<td>— µs From Stand-by to RX ready</td>
</tr>
<tr>
<td>TSRHOP</td>
<td>Receiver Hop Time from RX Ready to RX Ready with a Frequency Hop</td>
<td>—</td>
<td>400</td>
<td>—</td>
<td>µs</td>
<td>— µs 200 kHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>400</td>
<td>—</td>
<td>µs</td>
<td>— µs 1 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>460</td>
<td>—</td>
<td>µs</td>
<td>— µs 5 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>480</td>
<td>—</td>
<td>µs</td>
<td>— µs 7 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>520</td>
<td>—</td>
<td>µs</td>
<td>— µs 12 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>550</td>
<td>—</td>
<td>µs</td>
<td>— µs 20 MHz step</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>600</td>
<td>—</td>
<td>µs</td>
<td>— µs 27 MHz step</td>
</tr>
<tr>
<td>RSSIST</td>
<td>RSSI Sampling Time</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>1/$f_{dev}$</td>
<td>s From RX ready</td>
</tr>
<tr>
<td>RSSTDR</td>
<td>RSSI Dynamic Range</td>
<td>—</td>
<td>—</td>
<td>70</td>
<td>dB</td>
<td>— dB Ranging from sensitivity</td>
</tr>
</tbody>
</table>

**Note 1:** Guaranteed by design and characterization.

**Note 2:** This reflects the whole receiver bandwidth, as described by conditions for active and passive filters.
### TABLE 5-6: TRANSMITTER AC CHARACTERISTICS\(^{(1)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>RFOP</td>
<td>RF Output Power, Programmable with 8 Steps of typ. 3 dB</td>
<td>—</td>
<td>+12.5</td>
<td>—</td>
<td>dBm</td>
<td>Maximum power setting.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>-8.5</td>
<td>—</td>
<td>dBm</td>
<td>Minimum power setting.</td>
</tr>
<tr>
<td>PN</td>
<td>Phase Noise</td>
<td>—</td>
<td>-112</td>
<td>—</td>
<td>dBc/Hz</td>
<td>Measured with a 600 kHz offset at the transmitter output.</td>
</tr>
<tr>
<td>TXSP</td>
<td>Transmitted Spurious</td>
<td>—</td>
<td>—</td>
<td>-47</td>
<td>dBc</td>
<td>At any offset between 200 kHz and 600 kHz, unmodulated carrier, (f_{dev} = 50) kHz.</td>
</tr>
<tr>
<td>TX2</td>
<td>Second Harmonic</td>
<td>—</td>
<td>—</td>
<td>-40</td>
<td>dBm</td>
<td>No modulation, see Note 2</td>
</tr>
<tr>
<td>TX3</td>
<td>Third Harmonic</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>TX4</td>
<td>Fourth Harmonic</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>TXn</td>
<td>Harmonics above TX4</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>FSKDEV</td>
<td>FSK Deviation</td>
<td>±33</td>
<td>±55</td>
<td>-200</td>
<td>kHz</td>
<td>Programmable</td>
</tr>
<tr>
<td>TSTWF</td>
<td>Transmitter Wake-up Time</td>
<td>—</td>
<td>120</td>
<td>500</td>
<td>µs</td>
<td>From FS to TX ready.</td>
</tr>
<tr>
<td>TSTWS</td>
<td>Transmitter Wake-up Time</td>
<td>—</td>
<td>600</td>
<td>900</td>
<td>µs</td>
<td>From Stand-by to TX ready.</td>
</tr>
</tbody>
</table>

**Note 1:** Guaranteed by design and characterization.  
**Note 2:** Transmitter in-circuit performance with RFM recommended SAW filter and crystal.

### 5.2 Timing Specification and Diagram

### TABLE 5-7: SPI TIMING SPECIFICATION\(^{(1,2,3)}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPI Configure Clock Frequency</td>
<td>—</td>
<td>—</td>
<td>6</td>
<td>MHz</td>
<td>—</td>
</tr>
<tr>
<td>SPI Data Clock Frequency</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>MHz</td>
<td>—</td>
</tr>
<tr>
<td>Data Hold and Setup Time</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>µs</td>
<td>—</td>
</tr>
<tr>
<td>SDI Setup Time for SPI Configure</td>
<td>250</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td>SDI Setup Time for SPI Data</td>
<td>312</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td>CSCON Low to SCK Rising Edge; SCK Falling Edge to CSCON High</td>
<td>500</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td>CSDAT Low to SCK Rising Edge; SCK Falling Edge to CSDAT High</td>
<td>625</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td>CSCON Rising to Falling Edge</td>
<td>500</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>—</td>
</tr>
<tr>
<td>CSDAT Rising to Falling Edge</td>
<td>625</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td>—</td>
</tr>
</tbody>
</table>

**Note 1:** Typical Values: \(T_A = 25^\circ\)C, \(V_{DD} = 3.3\)V, crystal frequency = 12.8 MHz, unless otherwise specified.  
**Note 2:** Negative current is defined as the current sourced by the pin.
5.3 Switching Times and Procedures

As an ultra low-power device, the MRF89XA can be configured for low minimum average power consumption. To minimize consumption the following optimized transitions between modes are shown.

5.3.1 OPTIMIZED RECEIVE CYCLE

The lowest-power RX cycle is shown in Figure 5-1.

**FIGURE 5-1: OPTIMIZED RX CYCLE**

- Set MRF89XA in Stand-by mode
- Wait for XO settling
- Set MRF89XA in FS mode
- Wait for PLL settling
- Set MRF89XA in RX mode
- Wait for Receiver settling
- Receiver is ready:
  - RSSI sampling is valid after a 1/f<sub>dev</sub> period
  - Received data is valid
- MRF89XA can be put in Any other mode

**Note 1:** If the lock detect indicator is available on an external interrupt pin of the companion microcontroller, it can be used to optimize TSFS, without having to wait the maximum specified TSFS.
5.3.2  OPTIMIZED TRANSMIT CYCLE

FIGURE 5-2: OPTIMIZED TX CYCLE

- Set MRF89XA in Stand-by mode
- Wait for OSC settling
- 16 mA typ. @ 1 dBm
- Set MRF89XA in Stand-by mode
- Wait for OSC settling
- Set MRF89XA in FS mode
- Wait for PLL settling
- Set MRF89XA in TX mode
- Packet mode starts its operation
- Data transmission can start in Continuous and Buffered modes
- TX Time
- MRF89XA can be put in Any other mode
- IDDT
  - 1.3 mA typ.
- IDDFS
  - 65 µA typ.
- IDDSL
  - 100 nA typ.
- IDDT
  - 16 mA typ. @ 1 dBm

Note 1: TSFS time can be improved by using the external lock detector pin as an external interrupt trigger.
5.3.3 TRANSMITTER FREQUENCY HOP OPTIMIZED CYCLE

FIGURE 5-3: TX HOP CYCLE

1. Set R2/P2/S2
2. Set MRF89XA in FS mode, change Frequency Band Select bits (FBS<1:0>) if needed, then switch from R1/P1/S1 to R2/P2/S2

MRF89XA is in TX mode
On channel 1 (R1/P1/S1)

MRF89XA is now ready for data transmission

Set MRF89XA back in TX mode

IDD
16 mA typ. @1 dBm

IDDFS
1.3 mA typ.

Wait
TSTWF

Wait
TSHOP
5.3.4 RECEIVER FREQUENCY HOP
OPTIMIZED CYCLE

FIGURE 5-4: RX HOP CYCLE

MRF89XA
IDD
IDDR
3 mA typ.

IDDFS
1.3 mA typ.

Time

MRF89XA is in RX mode
On channel 1 (R1/P1/S1)

MRF89XA is ready
for data reception

Wait
TSRWF

Set MRF89XA back in RX mode

1. Set R2/P2/S2
2. Set MRF89XA in FS mode, change
Frequency Band Select bits (FBS<1:0>), then switch
from R1/P1/S1 to R2/P2/S2

Note: It is also possible to move from one channel to another without having to switch off the receiver. This method
is faster and overall draws more current. For timing information, refer to TSRHOP.
MRF89XA

5.3.5 RX → TX AND TX → RX JUMP CYCLES

FIGURE 5-5: RX → TX → RX CYCLE

MRF89XA is in RX mode

Set MRF89XA in TX mode

MRF89XA is now ready for data transmission

Wait TSWF

Set MRF89XA in RX mode

MRF89XA is ready to receive data

Wait TSWF

16 mA typ. @1 dBm

3.0 mA typ.

MRF89XA is in RX mode

IDD

IDD/
5.4 Typical Performance Characteristics

5.4.1 SENSITIVITY FLATNESS

FIGURE 5-6: SENSITIVITY ACROSS THE 869 MHz BAND

![Sensitivity Across the 869 MHz Band](image)

Note: Measured in FSK mode only. OOK sensitivity characteristics will be similar. The sensitivity difference along the band remains inside the ripple performance of the SAW filter (the nominal passband of the 869 MHz SAW filter is 868-870 MHz). The SAW filter ripple response is referenced to its insertion loss at 869 MHz and 915 MHz for each filter.

FIGURE 5-7: SENSITIVITY ACROSS THE 915 MHz BAND

![Sensitivity Across the 915 MHz Band](image)
5.4.2 SENSITIVITY VS. LO DRIFT

FIGURE 5-8: FSK SENSITIVITY LOSS VS. LO DRIFT

FIGURE 5-9: OOK SENSITIVITY LOSS VS. LO DRIFT

Note: In FSK mode, the default filter setting (‘A3’ at address 0x16) is kept, leading to $f_c = 96$ kHz typical. In OOK mode, ‘F3’ is set at address 0x16, leading to $(f_c - f_o) = 95$ kHz typical. Both of these settings ensure that the channel filter is wide enough, therefore characterizing the demodulator response and not the filter response.
5.4.3 SENSITIVITY VS. RECEIVER BW

FIGURE 5-10: FSK SENSITIVITY VS. RX BW

![Graph showing FSK sensitivity vs. receiver bandwidth.](image)

FIGURE 5-11: OOK SENSITIVITY CHANGE VS. RX BW

![Graph showing OOK sensitivity change vs. receiver bandwidth.](image)
5.4.4 SENSITIVITY STABILITY OVER TEMPERATURE AND VOLTAGE

FIGURE 5-12: SENSITIVITY STABILITY

Note: The sensitivity performance is very stable over the VDD range, and the effect of high temperature is minimal.
5.4.5 SENSITIVITY VS. BIT RATE

**FIGURE 5-13: FSK SENSITIVITY VS. BR**

![FSK Sensitivity vs. BR Graph]

**FIGURE 5-14: OOK SENSITIVITY VS. BR**

![OOK Sensitivity vs. BR Graph]
5.4.6 ADJACENT CHANNEL REJECTION

FIGURE 5-15: ACR IN FSK MODE

![Graph showing ACR in FSK mode with offset kHz on the x-axis and ACR [dB] on the y-axis.]

FIGURE 5-16: ACR IN OOK MODE

![Graph showing ACR in OOK mode with offset kHz on the x-axis and ACR [dB] on the y-axis.]

Note: In FSK mode, the unwanted signal is unmodulated (as described in the EN 300-220). Co-channel rejection (CCR, offset ≠ 0 kHz) is positive due to the DC cancellation process of the zero-IF architecture. In OOK mode, the polyphase filter efficiency is limited, thus limiting the adjacent channel rejection at 2xFo distance.
5.4.7 OUTPUT POWER FLATNESS

FIGURE 5-17: P_{out} FOR 869 MHz BAND OPERATION

FIGURE 5-18: P_{out} FOR 915 MHz BAND OPERATION

Note: As noted in Section 4.3.1 “SAW Filter Plot”, the 869 MHz SAW filter does not cover the entire European 863-870 MHz frequency band when used in a 50Ω environment. Therefore, the output power degradation at the lowest frequencies. For applications in the 863-860 MHz band, it is recommended that an appropriate SAW filter be implemented or that the SAW response is tuned by external matching. The SAW filter ripple references are the insertion loss of each SAW at 869 MHz and 915 MHz.
5.4.8 $P_{OUT}$ AND $I_{DD}$ VS. PA SETTING

**FIGURE 5-19:** $P_{OUT}$ AND $I_{DD}$ AT ALL PA SETTING – 869 MHz

**FIGURE 5-20:** $P_{OUT}$ AND $I_{DD}$ AT ALL PA SETTINGS – 915 MHz

Note: +10 dBm typical. Output power is achievable, even at SAW filter’s output.
5.4.9  \( P_{\text{OUT}} \) STABILITY OVER TEMPERATURE AND VOLTAGE

**FIGURE 5-21:**  \( P_{\text{OUT}} \) STABILITY

The output power is not sensitive to the supply voltage, and it decreases slightly when temperature rises.
5.4.10 TRANSMITTER SPECTRAL PURITY

FIGURE 5-22: 869 MHz SPECTRAL PURITY DC-1 GHz

FIGURE 5-23: 869 MHz SPECTRAL PURITY 1-6 GHz
5.4.11 OOK CHANNEL BANDWIDTH

The OOK bit rate ranges from 1.56 to 16.7 kbps. For the lowest bit rates, a channel spacing around 200 kHz is achievable.

**FIGURE 5-24: OOK SPECTRUM – 2 kbps**

**FIGURE 5-25: OOK SPECTRUM – 8 kbps**
FIGURE 5-26: OOK SPECTRUM – 16.7 kbps
5.4.12 FSK SPECTRUM IN EUROPE

Figure 5-27 illustrates the minimal spectral occupation achievable in the European band, ensure that the minimum frequency deviation that a MRF89XA receiver can accept is 33 kHz. If the companion receiver can accept smaller frequency deviations, the range of modulation bandwidth can be further decreased.

**FIGURE 5-27:** FSK – 1.56 KBPS – ±33 kHz

![Graph showing the spectral occupation and frequency deviation for FSK at 1.56 KBPS with a deviation of ±33 kHz.](image)

- The default configuration of the MRF89XA yields the bandwidth visible on Figure 5-28.

**FIGURE 5-28:** FSK – 25 KBPS – ±50 kHz

![Graph showing the spectral occupation and frequency deviation for FSK at 25 KBPS with a deviation of ±50 kHz.](image)

Figure 5-28 illustrates the maximal bit rate and frequency deviation that can fit in the 868 to 868.6 MHz European sub-band.
FIGURE 5-29: FSK – 40 KBPS – ±40 kHz

<table>
<thead>
<tr>
<th>Marker</th>
<th>Trace</th>
<th>Type</th>
<th>X Axis</th>
<th>Y Axis</th>
</tr>
</thead>
<tbody>
<tr>
<td>1R</td>
<td>(2)</td>
<td>Freq</td>
<td>868.0288 MHz</td>
<td>-38.73 dBm</td>
</tr>
<tr>
<td>1a</td>
<td>(2)</td>
<td>Freq</td>
<td>532.5 kHz</td>
<td>1.317 dB</td>
</tr>
</tbody>
</table>

Ref: 20 dBm Atten: 30 dB

Display Line: 37.00 dBm

Marker: Mkr1 Δ 532.5 kHz 1.317 dB
5.4.13 DIGITAL MODULATION SCHEMES

FCC Part 15.247 allows for systems employing digital modulation techniques to transmit up to 1 W, provided that the 6 dB bandwidth of the signal is at least 500 kHz and that the power spectral density does not exceed 8 dBm in any 3 kHz bandwidth.

The MRF89XA can meet these constraints while transmitting at the maximum output power of the device, typically 10 dBm. The built-in whitening process details are described in Section 3.11.4.2, Data Whitening.

**FIGURE 5-30: DTS 6 dB BANDWIDTH**

<table>
<thead>
<tr>
<th>Marker</th>
<th>Trace</th>
<th>Freq</th>
<th>X Ref</th>
<th>Amplitude</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(2)</td>
<td>914.300 MHz</td>
<td>10.84 dBm</td>
<td></td>
</tr>
<tr>
<td>2R</td>
<td>(2)</td>
<td>914.725 MHz</td>
<td>4.209 dBm</td>
<td></td>
</tr>
<tr>
<td>2a</td>
<td>(2)</td>
<td>905 kHz</td>
<td>-8.246 dB</td>
<td></td>
</tr>
</tbody>
</table>

**FIGURE 5-31: DTS POWER SPECTRAL DENSITY**

<table>
<thead>
<tr>
<th>Marker</th>
<th>Trace</th>
<th>Freq</th>
<th>X Ref</th>
<th>Amplitude</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(2)</td>
<td>914.300 MHz</td>
<td>7.714 dBm</td>
<td></td>
</tr>
<tr>
<td>2R</td>
<td>(2)</td>
<td>914.725 MHz</td>
<td>5.256 dBm</td>
<td></td>
</tr>
<tr>
<td>2a</td>
<td>(2)</td>
<td>905 kHz</td>
<td>7.706 dBm</td>
<td></td>
</tr>
</tbody>
</table>

Conditions:
- $P_{OUT} = +10.6$ dBm
- $f_{dev} = \pm 200$ kHz
- $BR = 100$ kbps (Chip rate=100 kCps, as data whitening is enabled)
- Packet mode, data whitening enabled

5.4.14 CURRENT STABILITY OVER TEMPERATURE AND VOLTAGE

**Figure 5-32** provides graphs for $I_D$ vs. Temperature and $V_{DD}$.
FIGURE 5-32: IDD vs. Temperature and VDD

Sleep Mode Current

FS Mode Current

TX Mode Current (Max Output Power)

Stand-by Mode Current

RX Mode Current

Legend:
- 85°C
- 25°C
- 0°C
- -40°C
6.0 PACKAGING INFORMATION

6.1 Package Details

This section provides the technical details of the packages.

<table>
<thead>
<tr>
<th>DIMENSIONS</th>
<th>INCHES</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.06</td>
<td>0.15</td>
</tr>
<tr>
<td>A1</td>
<td>0.00</td>
<td>0.00</td>
</tr>
<tr>
<td>A2</td>
<td>0.008</td>
<td>0.02</td>
</tr>
<tr>
<td>B</td>
<td>0.06</td>
<td>0.15</td>
</tr>
<tr>
<td>D</td>
<td>0.197</td>
<td>0.494</td>
</tr>
<tr>
<td>D1</td>
<td>0.118</td>
<td>0.299</td>
</tr>
<tr>
<td>E</td>
<td>0.197</td>
<td>0.494</td>
</tr>
<tr>
<td>E1</td>
<td>0.118</td>
<td>0.299</td>
</tr>
<tr>
<td>N</td>
<td>0.003</td>
<td>0.08</td>
</tr>
<tr>
<td>L</td>
<td>0.016</td>
<td>0.40</td>
</tr>
<tr>
<td>N</td>
<td>0.020</td>
<td>0.50</td>
</tr>
</tbody>
</table>

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
# APPENDIX A: FSK AND OOK RX FILTERS VS. BIT RATES

## TABLE A-1: FSK RX FILTERS VS. BIT RATE

<table>
<thead>
<tr>
<th>Bit Rate</th>
<th>Fdev (from FDEVREG)</th>
<th>Filter Setting (from FILCREG)</th>
<th>Fdev + BR/2 (from FDEVREG and BRSREG)</th>
<th>RX 3dB BW</th>
<th>Maximum Drift</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>± kHz</td>
<td>Hex</td>
<td>kHz</td>
<td>kHz</td>
<td>kHz</td>
</tr>
<tr>
<td>100</td>
<td>± 200</td>
<td>FF</td>
<td>250</td>
<td>400</td>
<td>306</td>
</tr>
<tr>
<td>66.67</td>
<td>± 133</td>
<td>E9</td>
<td>166.7</td>
<td>250</td>
<td>214</td>
</tr>
<tr>
<td>50</td>
<td>± 100</td>
<td>D6</td>
<td>125</td>
<td>175</td>
<td>158</td>
</tr>
<tr>
<td>40</td>
<td>± 80</td>
<td>B5</td>
<td>100</td>
<td>150</td>
<td>137</td>
</tr>
<tr>
<td>33.33</td>
<td>± 67</td>
<td>A4</td>
<td>83.3</td>
<td>125</td>
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<td>72</td>
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<td>20</td>
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<td>75</td>
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## TABLE A-2: OOK RX FILTERS VS. BIT RATE

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<th>Bit Rate</th>
<th>Fo + BR (from PFCREG and BRSREG)</th>
<th>Filter Setting (from FILCREG)</th>
<th>RX 3 dB BW</th>
<th>Maximum Drift</th>
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<td>Hex</td>
<td>Programmed</td>
<td>Actual</td>
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<td>16.67</td>
<td>± 176</td>
<td>C1</td>
<td>150</td>
<td>154</td>
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<td>12.5</td>
<td>± 122</td>
<td>C1</td>
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<td>154</td>
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<td>A0</td>
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<td>4.76</td>
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<td>± 102</td>
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<td>125</td>
<td>129</td>
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<td>± 102</td>
<td>A0</td>
<td>125</td>
<td>129</td>
</tr>
</tbody>
</table>

**Note 1:** To comply with any regulatory body like FCC for example with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. For regulated FSK and OOK settings, see MRF89XA device module data sheet from Microchip Website.
APPENDIX B: CRC COMPUTATION IN C# (CONVERTIBLE TO C)

```csharp
const ushort Polynome = 0x1021;
//Polynome = X^16+X^12+X^5+1

ushort ComputeCrc(ushort crc, byte data)
{
    for(int i = 0; i < 8; i++)
    {
        if(((crc & 0x8000) >> 8) ^ (data & 0x80)) != 0)
        {
            //shift left once crc ^= Polynome;   //XOR with polynomial
        }
        else
        {
            //next packetData reg bit
        }
    }
    return crc;
}

public ushort ComputeCrc(byte[] packet)
{
    ushort crc = 0x1D0F;
    for(int i = 0; i < packet.Length; i++)
    {
        crc = ComputeCrc(crc, packet[i]);
    }
    return (ushort)(~crc);
}
```
APPENDIX C: REVISION HISTORY

Revision A (January 2010)
This is the initial version of this document.

Revision B (June 2010)
Updates have been incorporated throughout the document, which required extensive revisions to all chapters.
This version also includes minor typographical and formatting changes throughout the data sheet text.

Revision C (November 2011)
Updates have been incorporated throughout the document, which required extensive revisions to all chapters.
Added Appendix B: “CRC Computation in C# (convertible to c)”.
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Telephone: (______) _________ - _________ FAX: (____) _________ - _________

Application (optional):

Would you like a reply? __ Y __ N

Device: MRF89XA Literature Number: DS70622C

Questions:

1. What are the best features of this document?

________________________________________________________________________

2. How does this document meet your hardware and software development needs?

________________________________________________________________________

3. Do you find the organization of this document easy to follow? If not, why?

________________________________________________________________________

4. What additions to the document do you think would enhance the structure and subject?

________________________________________________________________________

5. What deletions from the document could be made without affecting the overall usefulness?

________________________________________________________________________

6. Is there any incorrect or misleading information (what and where)?

________________________________________________________________________

7. How would you improve this document?

________________________________________________________________________
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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, for example, on pricing or delivery, refer to the factory or the listed sales office.

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Device MRF89XA: Ultra Low-Power, Integrated ISM Band Sub-GHz Transceiver

Temperature Range I = -40ºC to +85ºC (Industrial)

Package MQ = QFN (Quad Flat, No Lead)

T = Tape and Reel

Example:

a) MRF89XA-I/MQ: Industrial temperature, QFN package.
b) MRF89XAT-I/MQ: Industrial temperature, QFN package, tape and reel.