MRF49XA
Data Sheet
ISM Band Sub-GHz
RF Transceiver
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ISM Band Sub-GHz RF Transceiver

Features
- Fully Integrated Sub-GHz Transceiver
- Supports Proprietary Sub-GHz Wireless Protocols
- 4-Wire Serial Peripheral Interface (SPI) Compatible Interface
- CMOS/TTL Compatible I/Os
- Clock and Reset Signals for Microcontroller
- Integrated 10 MHz Oscillator Circuitry
- Integrated Low Battery Voltage Detector
- Supports Power-Saving modes
- Operating Voltage: 2.2V–3.8V
- Low-Current Consumption, Typically:
  - 11 mA in RX mode
  - 15 mA in TX mode
  - 0.3 μA in Sleep mode
- Industrial Temperature Range
- 16-Pin TSSOP Package

RF/Analog Features
- Supports ISM Band Sub-GHz Frequency Ranges (433 MHz, 868 MHz and 915 MHz)
- Modulation Technique: FSK with Frequency Hopping Spread Spectrum (FHSS) Capability
- Supports High Data Rates:
  - Digital mode 115.2 kbps, max.
  - Analog mode 256 kbps, max.
- Differential RF Input/Output:
  - -110 dBm Typical Sensitivity with 0 dBm Maximum Input Level
  - +7 dBm Typical Transmit Output Power
- High-Resolution Programmable Phase-Locked Loop (PLL) Synthesizer
- Integrated Power Amplifier
- Integrated Low Phase Noise Voltage Controlled Oscillator (VCO) Frequency
- Synthesizer and PLL Loop Filter
- Automatic Frequency Control (AFC)

Baseband Features
- Supports Programmable TX Frequency Deviation and RX Baseband Bandwidth (BBBW)
- Analog and Digital RSSI Outputs with Dynamic Range
- RX Synchronous Pattern Recognition
- 16-Bit RX Data FIFO
- Two 8-Bit TX Data Registers
- Low-Power Duty Cycle mode
- Advanced Adjacent Channel Rejection/Blocking Capability
- Internal Data and Clock Recovery
- Supports Data Filtering
- Data Quality Indicator (DQI)

Typical Applications
- Home/Industrial Automation
- Remote Control
- Wireless PC Peripherals
- Remote Keyless Entry
- Vehicle Sensor Monitoring
- Telemetry
- Data Logging Systems
- Remote Automatic Meter Reading
- Security Systems for Home/Industrial Environment
- Automobile Immobilizers
- Sports and Performance Monitoring
- Wireless Toy Controls
- Medical Applications
Pin Diagram: 16-Pin TSSOP

SDI  →  1  →  INT/DIO
SCK  →  2  →  RSSIO
CS   →  3  →  VDD
SDO  →  4  →  RFN
IRQ  →  5  →  RFP
FSK/DATA/FSEL →  6  →  Vss
RCLKOUT/FCAP/FINT →  7  →  RESET
CLKOUT  →  8  →  RFXTL/EXTREF

MRF49XA
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1.0 INTRODUCTION

Microchip’s MRF49XA is a fully integrated Sub-GHz RF transceiver. This low-power single chip Frequency Shift Keying (FSK) baseband transceiver supports:

- Zero-IF architecture
- Multi-channel and multi-band
- Synthesizer with PLL
- Power Amplifier (PA)
- Low Noise Amplifier (LNA)
- I/Q down converter mixers
- I/Q demodulator
- Baseband filters (BBFs) and amplifiers

The simplified functional block diagram of MRF49XA is shown in Figure 1-1. The MRF49XA is an ideal choice for low-cost, high-volume, low data rate (<256 kbps), two-way and short range wireless applications. This transceiver can be used in the unlicensed 433 MHz, 868 MHz and 915 MHz frequency bands, and for applications looking for FCC, IC or ETSI certification in the ISM band.

The MRF49XA has a low phase noise and provides an excellent adjacent channel interference, Bit Error Rate (BER) and larger communication coverage along with higher output power. The MRF49XA device’s AFC feature allows for the use of a low-accuracy, low-cost crystal. In order to minimize the total system cost, a communication link in most of the applications can be created using a low-cost, generic 10 MHz crystal, a bypass filter and an affordable microcontroller. The MRF49XA provides a clock signal for the microcontroller and avoids the need for a second crystal on the circuit board. The transceiver can be interfaced with many popular Microchip PIC® microcontrollers through a 4-wire SPI, interrupt (IRO) and Reset. The interface between the microcontroller and MRF49XA is shown in Figure 1-2.

The MRF49XA supports the following digital data processing features:

- PLL and I/Q VCO with Calibration
- Receiver Signal Strength Indicator
- Data Quality Indicator
- AFC
- Baseband Power Amplifier
- TX and RX Buffers

The receiver’s Baseband Bandwidth (BBBW) can be programmed to accommodate various deviations, data rates and crystal tolerance requirements.

The high-resolution PLL allows:

- The usage of multiple channels in any of the bands
- The rapid settling time allows for faster frequency hopping, bypassing multipath fading and interference to achieve robust wireless links

The transceiver is integrated with different Sleep modes and an internal wake-up timer to reduce the overall current consumption, and to extend the battery life. The device’s small size with low-power consumption makes it ideal for various short range radio applications.
FIGURE 1-1: FUNCTIONAL NODE BLOCK DIAGRAM

Antenna

Matching Circuitry

RFP

RFN

MRF49XA

RF Block

PA/LNA and PLL/CLK Block

Baseband Amplifier/Filter/Limiter

Data Processing Unit

Power Management

Memory

10 MHz

MCU Interface

SPI Signals

Other Handshaking Signals

FIGURE 1-2: MICROCONTROLLER TO MRF49XA INTERFACE

PIC® MCU

<table>
<thead>
<tr>
<th>INT</th>
<th>I/O/SS</th>
<th>SDO</th>
<th>SDI</th>
<th>SCK</th>
<th>I/O</th>
<th>I/O</th>
<th>I/O</th>
<th>OSC1</th>
<th>I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

MRF49XA

<table>
<thead>
<tr>
<th>IRO</th>
<th>CS</th>
<th>SDI</th>
<th>SDO</th>
<th>SCK</th>
<th>INT/DIO*</th>
<th>RESET*</th>
<th>FSK/DATA/FSEL*</th>
<th>CLKOUT*</th>
<th>RCLKOUT/FCAP/FINT*</th>
</tr>
</thead>
</table>

* Implies optional signals.
2.0 HARDWARE DESCRIPTION

The MRF49XA is an integrated, single chip ISM Band Sub-GHz Transceiver. A simplified architectural block diagram of the MRF49XA is shown in Figure 2-1.

The frequency synthesizer is clocked by an external 10 MHz crystal and generates the 433, 868 and 915 MHz radio frequency. The receiver with a Zero-IF architecture consists of the following components:

- LNA
- Down Conversion Mixers
- Channel Filters
- Baseband Limiting Amplifiers
- Receiver Signal Strength Indicator

The transmitter with a direct conversion architecture has a typical output power of +7 dBm. An internal transmit/receive switch combines the transmitter and receiver circuits into differential RFP and RFN pins. These pins are connected to the impedance matching circuitry (Balun) and to the external antenna connected to the device.

The device operates in the low-voltage range of 2.2V–3.8V, and in Sleep mode, it operates at a very low-current state, typically 0.3 μA.

The quality of the data is checked or validated using the RSSI and DQI blocks built into the transceiver. Data is buffered in transmitter registers and receiver FIFOs. The AFC feature allows the use of a low-accuracy and low-cost crystal. The CLKOUT is used to clock the external controller. The transceiver is controlled through a 4-wire SPI, interrupt (INT/DIO and IRO), FSK/DATA/FSEL, RCLKOUT/FCAP/FINT and RESET pins. See Table 2-1 for pin details.

The MRF49XA supports the following feature blocks:

- Clock Generation
- Data Filtering and Amplification
- Data Pattern Recognition and Timing
- Data Processing and Storage
- Independent Transmit and Receiver FIFO Buffers
- Registers

These features reduce the processing load, and hence, allows the use of low-cost 8-bit microcontrollers for data processing.
FIGURE 2-1: MRF49XA ARCHITECTURAL BLOCK DIAGRAM

- PLL and I/Q VCO with Calibration
- PA/LNA and PLL/CLK Block
- Baseband Amplifier/Filter/Limiter Block
- Self Calibration
- PLL and I/Q VCO with Calibration
- Data Filtering and Clock Recovery Unit
- Microcontroller Interface Block
- Power Supply Block
- Clock Block
- Low-Power Block
- Microcontroller Interface Block
- Data Processing Block
## TABLE 2-1: PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SDI</td>
<td>Digital Input</td>
<td>Serial data input interface to MRF49XA (SPI input signal).</td>
</tr>
<tr>
<td>2</td>
<td>SCK</td>
<td>Digital Input</td>
<td>Serial clock interface (SPI clock).</td>
</tr>
<tr>
<td>3</td>
<td>CS</td>
<td>Digital Input</td>
<td>Serial interface chip select (SPI chip/device select).</td>
</tr>
<tr>
<td>4</td>
<td>SDO</td>
<td>Digital Output</td>
<td>Serial data output interface from MRF49XA (SPI output signal).</td>
</tr>
<tr>
<td>5</td>
<td>IR0</td>
<td>Digital Output</td>
<td><strong>Interrupt Request Output:</strong> Receiver generates an active-low interrupt request for the microcontroller on the following events:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• The TXBREG (see Table 2-4) is ready to receive the next byte.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• The RXFIFOREG (see Table 2-4) has received the preprogrammed amount of bits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• RXFIFOREG overflow/TXBREG underrun.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Negative pulse on interrupt input pin (INT).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Wake-up timer time-out.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Supply voltage below the preprogrammed value is detected.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Power-on Reset (POR).</td>
</tr>
<tr>
<td>6</td>
<td>FSK/DATA/FSEL</td>
<td>Digital Input/Output</td>
<td><strong>Frequency Shift Keying:</strong> Transmit FSK data input (with internal pull-up resistor of 133 kΩ)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Data:</strong> When configured as DATA, this pin functions as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Data In: Manually modulates the data from the external host microcontroller when the TXBREG is disabled. If the TXBREG is enabled, this pin can be tied “high” or left unconnected. When reading the internal RXFIFOREG, this pin must be pulled “low”.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Data Out: Receives data in conjunction with RCLKOUT when the internal FIFO is not used.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>FIFO Select:</strong> Selects the FIFO and the first bit appears on the next clock when reading the RXFIFOREG. The FSEL pin has an internal pull-up resistor. This pin must be “high” when the TX register is enabled. In order to achieve minimum current consumption, keep this pin “high” in Sleep mode.</td>
</tr>
<tr>
<td>7</td>
<td>RCLKOUT/FCAP/FINT</td>
<td>Digital Input/Output</td>
<td><strong>Recovery Clock Output:</strong> Provides the clock recovered from the incoming data if:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• FTYPE bit of BBFCREG (see Table 2-10) is configured as digital filter and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• FIFO is disabled by configuring FIFOEN bit of GENCREG (see Table 2-10)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>Filter Capacitor:</strong> This pin is a raw baseband data if the FTYPE bit of BBFCREG is configured as a configuration filter. The pin can be used by the host microcontroller for data recovery.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td><strong>FIFO Interrupt:</strong> When the internal FIFO, FIFOEN bit of GENCREG is enabled, this pin acts as a FIFO full interrupt, indicating that the FIFO has been filled to its preprogrammed limit (see FFBC&lt;3:0&gt; bits in FIFOSTREG in Table 2-10).</td>
</tr>
<tr>
<td>8</td>
<td>CLKOUT</td>
<td>Digital Output</td>
<td><strong>Clock Output:</strong> The transceiver’s clock output can be used by the host microcontroller as a clock source. Refer Register 2 for more details.</td>
</tr>
</tbody>
</table>
### TABLE 2-1: PIN DESCRIPTION (CONTINUED)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>RFXTL/EXTREF</td>
<td>Analog Input</td>
<td><strong>RF Crystal</strong>: This pin is connected to a 10 MHz series crystal or to an external oscillator reference. The crystal is used as a reference for the PLL which generates the local oscillator frequency. It is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. <strong>External Reference Input</strong>: An external reference input, such as an oscillator, can be connected as a reference source. Connect the oscillator through a 0.01 μF capacitor.</td>
</tr>
<tr>
<td>10</td>
<td>RESET</td>
<td>Digital Input/Output</td>
<td>Active-low hardware pin. This pin has an open-drain Reset output with internal pull-up and input buffer. Refer to Section 3.1, Reset for more details.</td>
</tr>
<tr>
<td>11</td>
<td>Vss</td>
<td>Ground</td>
<td>Ground reference.</td>
</tr>
<tr>
<td>12</td>
<td>RFP</td>
<td>RF Input/Output</td>
<td>Differential RF input/output (+).</td>
</tr>
<tr>
<td>13</td>
<td>RFN</td>
<td>RF Input/Output</td>
<td>Differential RF input/output (-).</td>
</tr>
<tr>
<td>14</td>
<td>VDD</td>
<td>Power</td>
<td>RF power supply. Bypass with a capacitor close to the pin. See Section 2.1, Power and Ground Pins for more details.</td>
</tr>
<tr>
<td>15</td>
<td>RSSIO</td>
<td>Analog Input/Output</td>
<td><strong>Received Signal Strength Indicator Output</strong>: The analog RSSI output is used to determine the signal strength. The response and settling time depends on the external filter capacitor. Typically, a 4-10 nF capacitor provides optimum response time for most applications.</td>
</tr>
<tr>
<td>16</td>
<td>INT/DIO</td>
<td>Digital Input/Output</td>
<td><strong>Interrupt</strong>: This pin can be configured as an active-low external interrupt to the device. If a logic ‘0’ is applied to this pin, it causes the IRO pin to toggle, signaling an interrupt to the external microcontroller. The source of interrupt can be determined by reading the first four bits of STSREG (see Table 2-4). This pin can be used to wake-up the device from Sleep. <strong>Data Indicator Output</strong>: This pin can be configured to indicate valid data based on the actual internal settings.</td>
</tr>
</tbody>
</table>


2.1 Power and Ground Pins

The power supply bypassing is very essential for better handling of signal surges and noise in the power line. The large value decoupling capacitors should be placed at the PCB power input. The smaller value decoupling capacitors should be placed at every power point of the device and at bias points for the RF port. Poor bypassing leads to conducted interference which can cause noise and spurious signals to couple into the RF sections, thereby significantly reducing the performance.

The VDD pin requires two bypass capacitors to ensure sufficient bypass and decoupling. However, based on the selected carrier frequency, the bypass capacitor values vary. The recommended bypass capacitor values are listed in Table 2-2 and the type of capacitor to be used is listed in Table 2-3. The bypass capacitors are connected to pin 14, as shown in Figure 4-1. The trace length (VDD pin to bypass capacitors) should be made as short as possible.

<table>
<thead>
<tr>
<th>Band (MHz)</th>
<th>C1(μF)</th>
<th>C2 (nF)</th>
<th>C3 (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>433</td>
<td>2.2</td>
<td>10</td>
<td>220</td>
</tr>
<tr>
<td>868</td>
<td>2.2</td>
<td>10</td>
<td>47</td>
</tr>
<tr>
<td>915</td>
<td>2.2</td>
<td>10</td>
<td>33</td>
</tr>
</tbody>
</table>

2.2 RESET Pin

An external hardware Reset of MRF49XA can be performed by asserting the RESET (pin 10) to low. After releasing the pin, it takes slightly more than 0.25 ms for the transceiver to be released from the Reset. The pin is driven with an open-drain output, and hence, it is pulled down while the device is in POR. The RESET pin has an internal, weak, on-chip, pull-up resistor. The device will not accept commands during the Reset period.

The device enters the Reset mode if any of the following events take place:
- Power-on Reset
- Power Glitch Reset
- Software Reset
- RESET Pin

Software Reset can be issued by sending the appropriate control command to the device. The result of the command is similar to POR, but the duration of the Reset event is much less, typically 0.25 ms. The Software Reset works only when the Sensitive Reset mode is selected. See Section 3.1, Reset for details on Reset; for connection details, see Figure 4-1.

2.3 Power Amplifier

The PA has an open-collector differential output and can directly drive different PCB antennas, like loop or dipole, with a programmable output power level during signal transmission. However, certain types of antennas, like monopole, need an additional matching circuitry. A built-in, automatic antenna tuning circuit is used to avoid the manual tuning and trimming procedures during production process; the so called “hand effect”.

2.4 Low Noise Amplifier

The LNA has approximately 250Ω of differential input impedance which functions well with the proposed antenna (PCB/monopole) during signal transmission. The LNA, when connected to the 50Ω device, needs an external matching circuit (Balun) for correct matching and to minimize the noise figure of the receiver.

The LNA gain can be selected in four steps for different gain factors (between 0 dB and -20 dB relative to the highest gain) based on the required RF signal strength. This gain selection feature is useful in a noisy environment.
2.5 RFXTL/EXTREF and CLKOUT Pins

The MRF49XA has an internal, integrated crystal oscillator circuit, and therefore, a single RFXTL/EXTREF pin is used as a crystal oscillator. The crystal oscillator circuit, with internal loading capacitors, provides a 10 MHz reference signal for the PLL. The PLL, in turn, generates the local oscillator frequency. It is possible to "pull" the crystal to the accurate frequency by changing the load capacitor value. This reduces the external component count and simplifies the design. The crystal load capacitor is programmable from 8.5 pF–16 pF in 0.5 pF steps. Thus, the crystal oscillator circuit can accept a wide range of crystals from different manufacturers with different load capacitance requirements. The ability to vary the load capacitance also helps in fine tuning the final carrier frequency as the crystal itself is the PLL reference for the carrier. An external reference input, such as an oscillator, can be connected as a reference source. The oscillator can be connected through a 0.01 μF capacitor. Choosing better crystal results in a lesser TX to RX frequency offset and smaller deviation in BBBW. Hence, the recommended crystal accuracy should be ≤40 ppm. Deviation and BBBW are discussed in detail in Section 2.8, Baseband/Data Filters. The guidelines for selecting the appropriate crystal are explained in Section 3.6, Crystal Selection Guidelines.

The transceiver can provide a clock signal through the Clock Output (CLKOUT) pin to the microcontroller for accurate timing, and thus, eliminating the need for a second crystal. This also results in reducing the component count.

2.6 Phase-Locked Loop

The PLL circuitry determines the operating frequency of the device. This programmable PLL synthesizer requires only a single 10 MHz crystal reference source. The PLL maintains accuracy using the on-chip crystal controlled reference oscillator and provides maximum flexibility in performance to the designers. It is possible to change the crystal to the accurate frequency by changing the load capacitor value. The RF stability can be controlled by selecting a crystal with specifications which satisfy the application and by providing the functions required to generate the carriers, and by tuning each of the bands. For more details, see Section 3.6, Crystal Selection Guidelines. The PLL's high resolution allows the use of multiple channels in any of the bands. The on-chip PLL is able to perform manual and automatic calibration to compensate for the changes in temperature or operating voltage.

2.7 Automatic Frequency Control

The PLL in MRF49XA is capable of performing automatic fine adjustment for the carrier frequency by using an integrated AFC feature. The receiver uses the AFC feature to minimize the frequency offset between the TX/RX signals in discrete steps, which gives the advantage of:

- Narrower receiver bandwidth for increased sensitivity can be achieved
- Higher data rates can be achieved
- Usability of any locally available, low-accuracy and inexpensive crystals can be used

The MRF49XA can be programmed to automatically control the frequency or can be manually activated by a strobe signal.

2.8 Baseband/Data Filters

The BBFs are user-programmable. The receiver bandwidth can be set by programming the bandwidth of the BBFs. The receiver, when programmed, is set up according to the characteristics of the signal to be received. The baseband receiver has several programming options to optimize the communication for a variety of applications. The programmable functions are as follows:

- Baseband Analog Filter
- Baseband Digital Filter
- Receive Bandwidth
- Receive Data Rate
- Clock Recovery

The output data filtering can be performed using either an external capacitor or a digital filter based on the user application. The RCLKOUT/FCAP/FINT pin in MRF49XA provides the raw baseband data if configured as a configuration filter. It can be used by the host microcontroller to perform the data recovery.

2.9 Clock Recovery Circuit

The Clock Recovery Circuit (CLKRC) is used to render a synchronized clock source to recover the data using an external microcontroller. The CLKRC works by sampling the preamble on the received data. The preamble contains a sequence of 1 and 0 for the CLKRC to properly extract the data timing. In Slow mode, the CLKRC requires more sampling (12–16 bits), and hence, has a longer settling time before locking. In Fast mode, it uses less samples (6–8 bits) before locking, and thereby, the settling time is short which makes timing accuracy less critical. The RCLKOUT/FCAP/FINT pin provides the clock recovered from the incoming data if the baseband filter is configured as a digital filter.
2.10 Data Validity Blocks

2.10.1 RECEIVE SIGNAL STRENGTH INDICATOR

The MRF49XA provides the RSSI signal to the host microcontroller, and hence, supports the monitoring of analog and digital signal strengths. A digital RSSI output is provided to monitor the input signal level through an internal STATUS register. The digital RSSI goes high, if the received signal strength exceeds a given preprogrammed RSSI threshold level. The digital RSSI can be monitored by reading the STSREG. Alternatively, an analog RSSI signal is also available at pin 15 (RSSIO) to determine the signal strength. The analog RSSI settling time depends on the external filter capacitor. Typically, a 4–10 nF capacitor provides optimum response time for most of the applications. See Section 4.0, Application Details and Section 5.0, Electrical Characteristics for details on filter capacitors for analog RSSI. The typical relationship between analog RSSI voltage and RF input power is graphically represented in Figure 2-2.

2.10.2 DATA QUALITY INDICATOR

The Data Quality Indicator (DQI) is a special function which indicates the quality of the received signal and the link. The unfiltered received data is sampled and the number of spikes are counted in the received data for a specified time. If the input signals are of high value, it indicates the operating FSK transmitter of the high output signal within the baseband filter bandwidth from the local oscillator.

2.10.3 DATA INDICATOR OUTPUT

The Data Indicator Output (DIO) is an extension of DQI. The DIO pin can be configured to indicate valid data based on the actual internal settings. When an incoming signal is detected, the DIO uses the DQI clock recovery lock and digital RSSI signals to determine the validity of the incoming signal. The DIO searches for the valid data transitions at an expected data rate. The desired data rate and the acceptance criteria for valid data are user-programmable through the SPI port. The DIO signal is valid when using the internal receive FIFO or an external pin to capture baseband data.

The DIO has three modes of operation: Slow, Medium and Fast. Each mode is dependent on the type of signals it uses to determine the valid data and the number of incoming preamble bits present at the beginning of the packet. The DIO can be multiplexed with the INT pin for external usage.

FIGURE 2-2: ANALOG RSSI VOLTAGE vs. RF INPUT POWER
2.11 Power-Saving Blocks

2.11.1 LOW BATTERY VOLTAGE DETECTOR
The integrated low-battery voltage detector circuit monitors the supply voltage against a preprogrammed value and generates an interrupt on the IRO pin if it falls below the programmed threshold level. The detector circuit has a built-in 50 mV hysteresis.

2.11.2 WAKE-UP TIMER
The current consumption of the programmable wake-up timer is very low, typically 1.5 μA. It is programmable from 1 ms to several days with an accuracy level of ±10%. The calibration of the wake-up timer takes place at every start-up and every 30s thereafter, and is referenced with the crystal oscillator. The calibration is performed even in Sleep mode. The calibration process for the wake-up timer takes around 500 μs, and for proper calibration, the crystal oscillator must be running before the wake-up timer is enabled.

If any wake-up event occurs, including the wake-up timer, the wake-up logic generates an interrupt signal on the IRO pin which can be used to wake-up the microcontroller and this reduces the period that the microcontroller needs to be active. If the oscillator circuit is disabled, the calibration circuit turns it on for a brief period to perform the calibration in order to maintain accurate timing before returning to Sleep.

2.11.3 LOW DUTY CYCLE MODE
The MRF49XA can be made to enter into a Low Duty Cycle mode operation to decrease the average power consumption in Receive mode. The Low Duty Cycle mode is normally used in conjunction with the wake-up timer for its operation. The DCSREG may be configured so that when the wake-up timer brings the device out of Sleep mode, the receiver is turned on for a short time to sample for a signal. Then, the device returns to Sleep and this process repeats.

2.12 INT, IRO Pins and Interrupts
The Interrupt pin (INT) can be configured as an active-low external interrupt to MRF49XA which is provided from the host microcontroller.

The device generates an interrupt request for the host microcontroller by pulling the IRO pin low if the following events occur:
- TX register is ready to receive the next byte
- RX FIFO has received the preprogrammed amount of bits
- FIFO overflow/TX register underrun (TXUROW overflow in Receive mode and underrun in Transmit mode)
- Negative pulse on interrupt input pin, INT
- Wake-up timer time-out
- Supply voltage below the preprogrammed value is detected
- Power-on Reset

The Status bits should be read out to identify the source of interrupt. The interrupts are cleared by reading the STATUS register.

See Section 3.9, Interrupts for functional description of interrupts.

2.13 Transmit Register
The Transmit register in MRF49XA is configured as two, 8-bit shift registers connected in series to form a single 16-bit shift register. When the transmitter is enabled, it starts sending out data from the first register with respect to the set bit rate. After power-up and with the Transmit registers enabled, the transmitter preloads the TX latch with 0xAAAA. This can be used to generate a preamble before sending actual data.

In hardware, the FSK/DATA/FSEL has two functions:
- As Frequency Shift Keying pin, it basically takes care of transmitting the FSK data input. The pin has an internal pull-up resistor of 133 kΩ. This pin must be “high” when the TX register is enabled to take care of the transmission.
- As DATA (Data Out), this pin receives the data in conjunction with RCLKOUT when the internal FIFO is not used. When reading the internal RXFIFOREG, this pin must be pulled “low”.
### 2.14 Receive FIFO

The received data in MRF49XA is filled into a 16-bit First In First Out (FIFO) register. The FIFO is configured to generate an interrupt after receiving a defined number of bits. When the internal FIFO is enabled, the FIFO interrupt pin (RCLKOUT/FCAP/FINT) acts as a FIFO full interrupt, indicating that the FIFO has been filled to its preprogrammed limit. The receiver starts filling FIFO with data when it identifies the synchronous pattern through the synchronous pattern recognition circuit. During this process, the FINTDIO bit changes its state. The FIFO interrupt level is programmable from 1 to 16 bits. It is recommended to set the threshold to at least half the length of the register (8 bits) to ensure that the external host microcontroller has time to set up. The synchronous pattern recognition circuit prevents the FIFO from being filled up with noise, and hence, avoids overloading the external host microcontroller.

**Note:** The synchronous word is not accessible in the RX FIFO. The SYNBREG provides this information to the host microcontroller.

The FIFO read clock (SCK) must be $< \frac{\text{fXTAL}}{4}$ or $< 2.5 \text{ MHz}$ for 10 MHz on RFXTAL. The FSK/DATA/FSEL as the FIFO select pin, selects the FIFO and the first bit appears on the next clock when reading the RXFIFOREG.

In hardware, the FSK/DATA/FSEL pin is configured as DATA (Data In) and with internal TXBREG disabled; this manually modulates the data from the external host microcontroller. If the TXBREG is enabled, this pin can be tied “high” or can be left unconnected.

The internal synchronous pattern and the pattern length are user-programmable. If the Chip Select (CS) pin is low, the data bits on the SDI pin are shifted into the device on the rising edge of the clock on the SCK pin. The serial interface is initialized if the CS signal is high.

### 2.15 Serial Peripheral Interface

The MRF49XA communicates with the host microcontroller through a 4-wire SPI port as a slave device. An SPI compatible serial interface lets the user select, command and monitor the status of the MRF49XA through the host microcontroller. All registers consist of a command code, followed by a varying number of parameter or data bits. As the device uses word writes, the CS pin should be pulled low for 16 bits. Data bits on the SDI pin are shifted into the device upon the rising edge of the clock on the SCK pin whenever the CS pin is low.

The maximum clock frequency for the SPI bus is 20 MHz. The MRF49XA supports SPI mode 0,0 which requires the SCK to remain Idle in a low state. The CS pin must be held low to enable communication between the host microcontroller and the MRF49XA. The device’s timing specification details are given in Table 5-8.

#### Table 5-8

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data is received by the transceiver through the SDI pin and is clocked on the rising edge of SCK. The timing diagram is shown in Figure 5-1. MRF49XA sends out the data through the SDO pin and is clocked out on the falling edge of SCK. The Most Significant bit (MSb) is sent first (e.g., bit 15 for a 16-bit command) in any data. The POR circuit sets default values in all control and command registers.</td>
<td></td>
</tr>
</tbody>
</table>

**Note:** Special care must be taken when the microcontroller’s built-in hardware serial port is used. If the port cannot be switched to a 16-bit mode, then a separate I/O line should be used to control the CS pin to ensure a low level during the complete duration of the communication (command) or a software serial control interface should be implemented.

The SDO pin defaults to a low state when the CS pin is high (the MRF49XA is not selected). This pin has a tri-state buffer and uses a bus hold logic. For the SPI interface, see Figure 4-1.

The following parameters can be programmed and set through SPI:

- Frequency band
- Center frequency of the synthesizer
- Division ratio for the microcontroller clock
- Wake-up timer period
- Bandwidth of the baseband signal path
- Low supply voltage detector threshold

Any of these auxiliary functions can be disabled when not required. After power-on, all parameters are set to default values. The programmed values are retained during Sleep mode. The interface supports the read out of a status register which provides detailed information about the status of the transceiver and the received data.

**Note:** To test the SPI interface lines, set the LBD (Low Battery Detector) threshold below the actual VDD and the device must generate an interrupt.
2.16 Memory Organization

The memory in MRF49XA is implemented as static RAM and is accessible through the SPI port. Each memory location functionally addresses a register, control, status or data/FIFO fields, as shown in Table 2-10. The command/control registers provide control, status and device address for transceiver operations. The FIFOs serve as temporary buffers for data transmission and reception.

The commands to the device are sent serially. All 17 commands basically address the 17 registers affiliated to it. The registers consist of a command code, followed by control, data, status or parameter bits. The MSb is sent first in all of the commands (e.g., bit 15 for a 16-bit command). The POR circuit sets the default values in all control and command registers.

In general, MRF49XA registers are read only. Hence the chip status can only be read by the Status Read Register. During write, only appropriate byte is written to the desired register. It is not desired to read/write all registers and there is no way to read back the register.

### TABLE 2-4: CONTROL (COMMAND) REGISTER DESCRIPTION

<table>
<thead>
<tr>
<th>Sl. No.</th>
<th>Register Name</th>
<th>Register Description</th>
<th>Related Control Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>STSREG</td>
<td>Status Read Register</td>
<td>Receive register/FIFO, transmit register, interrupt, frequency control and signal strength, POR, wake-up timer, low battery detect, data quality, clock recovery</td>
</tr>
<tr>
<td>2</td>
<td>GENCREG</td>
<td>General Configuration Register</td>
<td>Frequency band select, enables TX and RX registers, crystal load capacitor bank value</td>
</tr>
<tr>
<td>3</td>
<td>AFCCREG</td>
<td>AFC Configuration Register</td>
<td>AFC locking range, mode, accuracy and enable</td>
</tr>
<tr>
<td>4</td>
<td>TXCREG</td>
<td>Transmit Configuration Register</td>
<td>Modulation polarity, modulation bandwidth, transmit power and deviation</td>
</tr>
<tr>
<td>5</td>
<td>TXBREG</td>
<td>Transmit Byte Register</td>
<td>Transmit data byte</td>
</tr>
<tr>
<td>6</td>
<td>CFSREG</td>
<td>Center Frequency Value Set Register</td>
<td>Transmit or receive frequency</td>
</tr>
<tr>
<td>7</td>
<td>RXCREG</td>
<td>Receive Control Register</td>
<td>Function of pin 16, DIO mode, RX BBBW, LNA gain, digital RSSI threshold</td>
</tr>
<tr>
<td>8</td>
<td>BBFCREG</td>
<td>Baseband Filter Configuration Register</td>
<td>Clock Recovery mode, data indicator parameter value and filter type</td>
</tr>
<tr>
<td>9</td>
<td>RXFIFOREG</td>
<td>Receiver FIFO Read Register</td>
<td>Receive data byte</td>
</tr>
<tr>
<td>10</td>
<td>FIFORSTREG</td>
<td>FIFO and Reset mode Configuration Register</td>
<td>FIFO interrupt level, FIFO start control and FIFO enable, POR Sensitivity mode, synchronous character length</td>
</tr>
<tr>
<td>11</td>
<td>SYNBREG</td>
<td>Synchronous Byte Configuration Register</td>
<td>Synchronous character pattern</td>
</tr>
<tr>
<td>12</td>
<td>DRSREG</td>
<td>Data Rate Value Set Register</td>
<td>Data rate prescalar set</td>
</tr>
<tr>
<td>13</td>
<td>PMCREG</td>
<td>Power Management Configuration Register</td>
<td>Enables receive and transmit chain, baseband circuit, synthesizer circuit, oscillator, wake-up timer, low battery detect and clock out</td>
</tr>
<tr>
<td>14</td>
<td>WTSREG</td>
<td>Wake-up Timer Value Set Register</td>
<td>Wake-up timer values for time interval</td>
</tr>
<tr>
<td>15</td>
<td>DCSREG</td>
<td>Duty Cycle Value Set Register</td>
<td>Duty Cycle mode and value</td>
</tr>
<tr>
<td>16</td>
<td>BCSREG</td>
<td>Battery Threshold Detect and Clock Output Value Set Register</td>
<td>Low battery detect threshold values and clock output frequency</td>
</tr>
<tr>
<td>17</td>
<td>PLLCREG</td>
<td>PLL Configuration Register</td>
<td>Clock out buffer speed, PLL bandwidth, dithering and delay</td>
</tr>
</tbody>
</table>
### 2.17 Control (Command) Register Details

**REGISTER 2-1: STSREG: STATUS READ REGISTER (POR: 0x0000)**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Mode</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>TXRXFIFO</td>
<td>Transmit</td>
<td>1 = Ready</td>
</tr>
<tr>
<td>14</td>
<td>POR</td>
<td>Power-on Reset</td>
<td>1 = POR has occurred</td>
</tr>
<tr>
<td>13</td>
<td>TXOWRXOF</td>
<td>Transmit Overwrite</td>
<td>1 = Underrun or overwrite</td>
</tr>
<tr>
<td>12</td>
<td>WUTINT</td>
<td>Wake-up Timer</td>
<td>1 = Timer overflow has occurred</td>
</tr>
<tr>
<td>11</td>
<td>LCEXINT</td>
<td>Logic Change on External Interrupt</td>
<td>1 = High-to-low transition has occurred</td>
</tr>
<tr>
<td>8</td>
<td>OFFSB&lt;3:0&gt;</td>
<td>Receive FIFO Overflow</td>
<td>1 = FIFO overflow</td>
</tr>
</tbody>
</table>

#### Legend:
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**Note:**
1. All register commands begin with logic ‘1’ and only the STATUS register read command begins with logic ‘0’.
2. This bit is multiplexed for Transmit or Receive mode.
3. See the FFBC bits (FIFORSTREG<3:0>) in Register 2-10.
4. To get accurate values, the AFC should be disabled during the read by clearing the FOFEN bit (AFCCREG<0>). The AFC offset value (OFFSB bits in the status word) is represented as a two’s complement number. The actual frequency offset can be calculated as the AFC offset value multiplied by the current PLL frequency step from CFSREG (FREQB<11:0>).
5. This bit is cleared after STSREG is read.
REGISTER 2-1: STSREG: STATUS READ REGISTER (POR: 0x0000)(1) (CONTINUED)

bit 10  LBTD: Low Battery Threshold Detect bit
Indicates whether the battery or supply voltage is below the preprogrammed threshold limit.
1 = Supply voltage is below threshold
0 = Normal supply voltage feed

bit 9  FIFOEM: FIFO Empty bit
Indicates whether the receive FIFO is empty or filled.
1 = FIFO is empty
0 = FIFO is filled

bit 8  ATRSSI: Antenna Tuning and Received Signal Strength Indicator bit
Transmit mode:
The bit indicates that the antenna tuning circuit has detected a strong RF signal.
1 = Strong RF signal present
0 = Weak or absence of RF signal
Receive mode:
The bit indicates that the incoming RF signal is above the preprogrammed digital RSSI limit.
1 = RF signal is above the threshold value set
0 = RF signal is less than the threshold value set

bit 7  DQDO: Data Quality Detect/Indicate Output bit
Indicates good data quality output.
1 = Quality data is detected
0 = Quality data is unavailable

bit 6  CLKRL: Clock Recovery Lock bit
Indicates clock recovery is locked.
1 = Clock recovery locked
0 = Clock recovery unlocked

bit 5  AFCCT: Automatic Frequency Control Cycle Toggle bit
For each AFC cycle run, this bit toggles between logic ‘1’ and logic ‘0’.
1 = AFC cycle has occurred
0 = No AFC in this cycle

bit 4  OFFSV: Offset Sign Value bit
Indicates the measured difference or frequency offset of any AFC cycle (sign of the offset value).
1 = Higher than the chip frequency
0 = Lower than the chip frequency

bit 3-0  OFFSB<3:0>: Offset bits
The offset value to be added to the frequency control parameter (internal PLL)(4).
1 = Result is negative
0 = Result is positive

Note 1: All register commands begin with logic ‘1’ and only the STATUS register read command begins with logic ‘0’.
2: This bit is multiplexed for Transmit or Receive mode.
3: See the FFBC bits (FIFORSTREG<3:0>) in Register 2-10.
4: To get accurate values, the AFC should be disabled during the read by clearing the FOFEN bit (AFCCREG<0>). The AFC offset value (OFFSB bits in the status word) is represented as a two’s complement number. The actual frequency offset can be calculated as the AFC offset value multiplied by the current PLL frequency step from CFSREG (FREQB<11:0>).
5: This bit is cleared after STSREG is read.

Note: See Appendix A: “Read Sequence and Packet Structures” for the STSREG read sequence.
REGISTER 2-2: GENCREG: GENERAL CONFIGURATION REGISTER (POR: 0x8008)

| bit 15-8 | | | | | | | |
| W-1 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 | W-0 |
| CCB<15:8> |

bit 7

| bit 6 | bit 5-4 | bit 3-0 |
| W-0 | W-0 | W-0 | W-0 | W-1 | W-0 | W-0 | W-0 |
| TXDEN | FIFOEN | FBS<1:0> | LCS<3:0> |

bit 0

Legend:
- r = reserved bit
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
  - ‘1’ = Bit is set
  - ‘0’ = Bit is cleared
  - x = Bit is unknown

bit 15-8: Command Code bits
The command code bits (10000000b) are serially sent to the microcontroller to identify the bits to be written in the GENCREG.

bit 7: TXDEN: TX Data Register Enable bit
1 = Internal TX Data register enabled
0 = Internal TX Data register disabled; no transmit

bit 6: FIFOEN: FIFO Enable bit
1 = Internal data FIFO enabled; the FIFO is used to store data during receive
0 = FIFO disabled; FSK/DATA/FSEL and RCLKOUT/FCAP/FINT are used to receive data

bit 5-4: FBS<1:0>: Frequency Band Select bits
These bits set the frequency band to be used in Sub-GHz range.
11 = 915 MHz
10 = 868 MHz
01 = 433 MHz
00 = Reserved

bit 3-0: LCS<3:0>: Load Capacitance Select bits
These bits set and vary the internal load capacitance for the crystal reference.
1111 = 16.0 pF
1110 = 15.5 pF
1101 = 15.0 pF
1100 = 14.5 pF
1011 = 14.0 pF
1010 = 13.5 pF
1001 = 13.0 pF
1000 = 12.5 pF
0111 = 12.0 pF
0110 = 11.5 pF
0101 = 11.0 pF
0100 = 10.5 pF
0011 = 10.0 pF
0010 = 9.5 pF
0001 = 9.0 pF
0000 = 8.5 pF

Note 1: If the internal TX data register is used, the DATA/FSK/FSEL pin must be pulled “high”.
2: If the data FIFO is used, the DATA/FSK/FSEL pin must be pulled “low”.
### REGISTER 2-3: AFCCREG: AUTOMATIC FREQUENCY CONTROL CONFIGURATION REGISTER

**(POR: 0xC4F7)**

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CCB&lt;15:8&gt;</td>
</tr>
</tbody>
</table>

### bit 15-8

**CCB<15:8>: Command Code bits**

The command code bits (11000100b) are serially sent to the microcontroller to identify the bits to be written in the AFCCREG.

### bit 7-6

**AUTOMS<1:0>: Automatic mode Selection bits (for AFC)**

These bits select the operation type (automatic/manual) for performing AFC based on the status of the MFCS bit.

- **11**: Keeps offset independent for the state of the DIO signal
- **10**: Keeps offset only while receiving (DIO = High)
- **01**: Runs and measures only once after each power-up cycle
- **00**: Auto mode off (controlled by microcontroller)

### bit 5-4

**ARFO<1:0>: Allowable Range for Frequency Offset bits**

These bits select the offset range allowable between transmitter and receiver frequencies.

- **11**: +3 FRES to -4 FRES
- **10**: +7 FRES to -8 FRES
- **01**: +15 FRES to -16 FRES
- **00**: No restriction

### bit 3

**MFCS: Manual Frequency Control Strobe bit**

This bit is the strobe signal which initiates the manual frequency control sample to calculate the offset error.

- **1**: A sample of a received signal is compared with a receiver Local Oscillator (LO) signal and an offset error is calculated. If bit 1 is enabled, the value is stored in the Offset register of the AFC block.
- **0**: Ready for the next sample

### bit 2

**HAM: High-Accuracy (Fine) mode bit**

- **1**: Switches the Frequency Control mode to High-Accuracy mode
- **0**: Frequency Control mode works in regular mode

### bit 1

**FOREN: Frequency Offset Register Enable bit**

- **1**: Enables the offset value calculated by the offset sample. The offset value is added to the frequency control word of the PLL which tunes the desired carrier frequency.
- **0**: Denies the addition of the offset value to the frequency control word of the PLL

### bit 0

**FOFEN: Frequency Offset Enable bit**

- **1**: Enables the frequency offset calculation using the AFC circuit
- **0**: Disables the frequency offset calculation using the AFC circuit

### Note 1:

The FRES is the frequency tuning resolution for each band. The FRES for each band is as follows:

- **433 MHz**: 2.5 kHz
- **868 MHz**: 5 kHz
- **915 MHz**: 7.5 kHz

### Note 2:

The offset error value is stored in the Offset register (FOREN bit should be enabled) in the AFC block and is added to the frequency control word of the PLL. Reset this bit before initiating another sample.

### Note 3:

In High-Accuracy (Fine) mode, the processing time is twice the regular mode, but the uncertainty of the measurement is significantly reduced.
REGISTER 2-4: TXCREG: TRANSMIT CONFIGURATION REGISTER (POR: 0x9800)

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCB&lt;15:9&gt;</td>
<td>MODPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **r** = reserved bit
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- ‘-’ = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**bit 15-9:** CCB<15:9>: Command Code bits

The command code bits (1001100b) are serially sent to the microcontroller to identify the bits to be written in the TXCREG.

**bit 8:** MODPLY: Modulation Polarity bit (for FSK)

When MODPLY is configured as high/low:

1 = Logic ‘0’ is the higher channel frequency and logic ‘1’ is the lower channel frequency (negative deviation)

0 = Logic ‘0’ is the lower channel frequency and logic ‘1’ is the higher channel frequency (positive deviation)

**bit 7-4:** MODBW<3:0>: Modulation Bandwidth bits

These bits set the FSK frequency deviation for transmitting the logic ‘1’ and logic ‘0’\(^{(1)}\).

- 1111 = 240 kHz
- 1110 = 225 kHz
- 1101 = 210 kHz
- 1100 = 195 kHz
- 1011 = 180 kHz
- 1010 = 165 kHz
- 1001 = 150 kHz
- 1000 = 135 kHz
- 0111 = 120 kHz
- 0110 = 105 kHz
- 0101 = 90 kHz
- 0100 = 75 kHz
- 0011 = 60 kHz
- 0010 = 45 kHz
- 0001 = 30 kHz
- 0000 = 15 kHz

**bit 3:** Reserved: Write as ‘0’

**Note 1:** The transmitter FSK modulation parameters are used for calculating the resulting output frequency, as shown in Equation 2-1.

2: The output transmit power range is relative to the maximum available power, which depends on the actual antenna impedance.
MRF49XA

REGISTER 2-4:  TXCREG: TRANSMIT CONFIGURATION REGISTER (POR: 0x9800) (CONTINUED)

bit 2-0  OTXPWR<2:0>: Output Transmit Power Range bits\(^{(2)}\)
These bits set the transmit output power range. The output power is programmable from 0 dB (Max.)
to -17.5 dB in -2.5 dB steps.
111 = -17.5 dB
110 = -15.0 dB
101 = -12.5 dB
100 = -10.5 dB
011 = -7.5 dB
010 = -5.0 dB
001 = -2.5 dB
000 = 0 dB

**Note 1:**  The transmitter FSK modulation parameters are used for calculating the resulting output frequency, as shown in Equation 2-1.

2:  The output transmit power range is relative to the maximum available power, which depends on the actual antenna impedance.

**EQUATION 2-1:**

\[
\begin{align*}
\hat{f}_{FSKout} &= f_0 + [(- 1) \text{SIGN } x (MB + 1) x (15 \text{ kHz})] \\
\text{where:} \\
f_0 &= \text{the Channel Center Frequency (see Register 2-6 for } f_0 \text{ Calculation)} \\
MB &= \text{the 4-bit Binary Number (MODBW<3:0>)} \\
\text{SIGN} &= \text{MODPLY } \text{xor FSK}
\end{align*}
\]
REGiSER 2-5: TXBREG: TRANSMIT BYTE RADIOE R (POR: 0xB8AA)

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-0</th>
<th>W-1</th>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CCB&lt;15:8&gt;</td>
<td>bit 15</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>W-1</th>
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<th>W-1</th>
<th>W-0</th>
<th>W-1</th>
<th>W-0</th>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TXDB&lt;7:0&gt;</td>
<td>bit 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- r = reserved bit
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 15-8  
CCB<15:8>: Command Code bits
The command code bits (10111000b) are serially sent to the microcontroller to identify the bits to be written in the TXBREG.

bit 7-0  
TXDB<7:0>: Transmit Data Byte bits
The transmit data bits hold the 8 bits that are to be transmitted. To use this register, set the bit, TXDEN = 1 (GENCREG<7>). If TXDEN is not set, use the FSK/DATA/FSEL pin to manually modulate the data.
REGISTER 2-6: CFSREG: CENTER FREQUENCY VALUE SET REGISTER (POR: 0xA680)

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-0</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CCB&lt;15:12&gt;</td>
<td></td>
<td></td>
<td>FREQB&lt;11:8&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>bit 15</td>
<td></td>
<td></td>
<td>bit 8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>FREQB&lt;7:0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>bit 7</td>
<td></td>
<td></td>
<td>bit 0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- r = reserved bit
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 15-12  
CCB<15:12>: Command Code bits
- The command code bits (1010b) are serially sent to the microcontroller to identify the bits to be written in the CFSREG.

bit 11-0  
FREQB<11:0>: Center Frequency Set bits
- These bits set the center frequency to be used during transmit or receive. The 12-bit value (FVAL) must be in a decimal range of 96 to 3903. The value outside this range results in the previous value being retained and used such that no frequency change occurs(1).

Note 1: To calculate the center frequency (F0), use Equation 2-2 and the values from Table 2-5. The CFSREG sets the frequency within the selected band for transmit or receive. Each band has a range of frequencies available for changing channels or frequency hopping. The selectable frequencies for each band are given in Table 2-6.

EQUATION 2-2:

\[ F_0 = 10 \times F_{A1} \times (F_{A0} + F_{VAL}/4000) \text{ MHz} \]

where:
- \( F_{VAL} = \) Decimal Value of FREQB<11:0> = 96 < \( F_{VAL} < 3903 \)
- Where \( F_{A0} \) and \( F_{A1} \) are constant values as given in Table 2-5 to calculate the Center Frequency.

TABLE 2-5: CENTER FREQUENCY VALUE

<table>
<thead>
<tr>
<th>Range</th>
<th>FA1</th>
<th>FA0</th>
</tr>
</thead>
<tbody>
<tr>
<td>433 MHz</td>
<td>1</td>
<td>43</td>
</tr>
<tr>
<td>868 MHz</td>
<td>2</td>
<td>43</td>
</tr>
<tr>
<td>915 MHz</td>
<td>3</td>
<td>30</td>
</tr>
</tbody>
</table>

TABLE 2-6: FREQUENCY BAND TUNING RESOLUTION

<table>
<thead>
<tr>
<th>Frequency Band (MHz)</th>
<th>Min. (MHz)</th>
<th>Max. (MHz)</th>
<th>Tuning Resolution (kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>400</td>
<td>430.2400</td>
<td>439.7575</td>
<td>2.5</td>
</tr>
<tr>
<td>800</td>
<td>860.4800</td>
<td>879.5150</td>
<td>5.0</td>
</tr>
<tr>
<td>900</td>
<td>900.7200</td>
<td>929.2725</td>
<td>7.5</td>
</tr>
</tbody>
</table>
REGISTER 2-7: RXCREG: RECEIVE CONTROL REGISTER (POR: 0x9080)

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
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</tr>
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<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 15</td>
<td>CCB&lt;15:11&gt;</td>
<td>FINTDIO</td>
<td>DIORT&lt;1:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 8</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 7</td>
<td>RXBW&lt;2:0&gt;</td>
<td>RXLNA&lt;1:0&gt;</td>
<td>DRSSIT&lt;2:0&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- r = reserved bit
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 15-11  **CCB<15:11>: Command Code bits**
The command code bits (10010b) are serially sent to the microcontroller to identify the bits to be written in the RXCREG.

bit 10 **FINTDIO: Function Interrupt/Data Indicator Output bit**
Sets the pin 16 function as the DIO or interrupt.
1 = DIO output
0 = INT input

bit 9-8  **DIORT<1:0>: Data Indicator Output Response Time bits**
If pin 16 is selected as DIO, these bits set the response time within which the transceiver detects and indicates the incoming synchronous bit pattern, and issues an interrupt to the host microcontroller.
11 = Continuous
10 = Slow
01 = Medium
00 = Fast

bit 7-5  **RXBW<2:0>: Receiver Baseband Bandwidth bits**
These bits set the bandwidth of demodulated data. The bandwidth can accommodate different data rates and deviations during frequency keying.
111 = Reserved
110 = 67 kHz
101 = 134 kHz
100 = 200 kHz
011 = 270 kHz
010 = 340 kHz
001 = 400 kHz
000 = Reserved

bit 4-3  **RXLNA<1:0>: Receiver LNA Gain bits**
These bits, when set to different values, can accommodate environments with high interferences. The LNA gain also affects the true RSSI value.
11 = -20 dB
10 = -14 dB
01 = -6 dB
00 = 0 dB
bit 2-0  DRSSIT<2:0>: Digital RSSI Threshold bits

These bits can be set to indicate the incoming signal strength above a preset limit. The result enables or disables the DQDO bit (STSREG<7>).

111 = Reserved
110 = Reserved
101 = -73 dB
100 = -79 dB
011 = -85 dB
010 = -91 dB
001 = -97 dB
000 = -103 dB
REGISTER 2-8: BBFCREG: BASEBAND FILTER CONFIGURATION REGISTER (POR: 0xC22C)

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-1</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CCB<15:8>:** Command Code bits

The command code bits (11000010b) are serially sent to the microcontroller to identify the bits to be written in the BBFCREG.

**bit 7**  
**ACRLC**: Automatic Clock Recovery Lock Control bit

1 = Configures the clock recovery lock control as automatic. In this setting, the clock recovery starts in Fast mode and automatically switches to Slow mode after locking

0 = Clock recovery lock is controlled in Manual mode

**bit 6**  
**MCRLC**: Manual Clock Recovery Lock Control bit

1 = Configures the clock recovery lock control to Fast mode. Fast mode requires a preamble of at least 6-8 bits to determine the clock rate and then it locks.

0 = Configures the clock recovery lock control to Slow mode. Slow mode takes a bit longer period and requires a preamble of at least 12-16 bits to determine the clock rate and then it locks. Slow mode requires more accurate bit timing. See Register 2-12 for the relationship between data rate and clock recovery.

**bit 5**  
**Reserved**: Write as ‘1’

**bit 4**  
**FTYPE**: Filter Type bit

1 = Configures the baseband filter as an analog RC low-pass filter

0 = Configures the baseband filter as a digital filter

(1) The digital filter is a digital version of a simple RC low-pass filter followed by a comparator with hysteresis. The time constant for the digital filter is automatically calculated based on the bit rate set in the DRSREG. The bit rate in this mode should not exceed 115 kbps. In analog RC filter, the demodulator output is fed to the RCLKOUT/FCAP/FINT pin over a 10 kΩ resistor. The filter cutoff frequency is set by the external capacitor connected to this pin and VSS. Table 2-6 shows the optimum filter capacitor values for different data rates.

**Note 1:** The digital filter parameter for the DQI should be set to less than four to report good signal quality if the bit rate is close to the deviation. Usually, if the data rate falls less than the deviation, a higher threshold parameter is permitted and might report a good signal quality.

**bit 3**  
**Reserved**: Write as ‘1’

**bit 2-0**  
**DQTI<2:0>:** Data Quality Threshold Indicator bits

The threshold parameter for the DQI should be set to less than four to report good signal quality if the bit rate is close to the deviation. Usually, if the data rate falls less than the deviation, a higher threshold parameter is permitted and might report a good signal quality.

2: The DQI parameter is calculated using Equation 2-3. The DQI parameter in BBFCREG should be chosen according to the following rules:

- The parameter should be > 4, otherwise, noise might be treated as a valid FSK signal.
- The maximum value is 7.
EQUATION 2-3:

\[ DQI_{par} = 4 \times \frac{\text{Deviation} - \text{TX/RXoffset}}{\text{Bit Rate}} \]

<table>
<thead>
<tr>
<th>Data Rate</th>
<th>Filter Capacitor Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2 kbps</td>
<td>12 nF</td>
</tr>
<tr>
<td>2.4 kbps</td>
<td>8.2 nF</td>
</tr>
<tr>
<td>4.8 kbps</td>
<td>6.8 nF</td>
</tr>
<tr>
<td>9.6 kbps</td>
<td>3.3 nF</td>
</tr>
<tr>
<td>19.2 kbps</td>
<td>1.5 nF</td>
</tr>
<tr>
<td>38.4 kbps</td>
<td>680 pF</td>
</tr>
<tr>
<td>57.6 kbps</td>
<td>270 pF</td>
</tr>
<tr>
<td>115.2 kbps</td>
<td>150 pF</td>
</tr>
<tr>
<td>256 kbps</td>
<td>100 pF</td>
</tr>
</tbody>
</table>
REGISTERS 2-9: RXFIFOREG: RECEIVER FIFO READ REGISTER (POR: 0xB000)

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-0</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
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<tbody>
<tr>
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<td></td>
</tr>
</tbody>
</table>

bit 15: CCB<15:8>

bit 7: RXDB<7:0>

Legend:
- r = reserved bit
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 15-8  CCB<15:8>: Command Code bits

The command code bits (10110000b) are serially sent to the microcontroller to identify the bits to be written in the RXFIFOREG.

bit 7-0  RXDB<7:0>: Receiver Data Byte bits

These are the recovered data bits stored in the FIFO. The controller can read 8 bits from the receiver FIFO over the SPI bus. The FIFOEN bit (GENCREG<6>) should be set to receive these bits.
REGISTER 2-10:  FIFORSTREG: FIFO AND RESET MODE CONFIGURATION REGISTER  
(POR: 0xCA80)

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-1</th>
<th>W-0</th>
<th>W-1</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

bit 15-8  
**CCB<15:8>:** Command Code bits  
The command code bits (11001010b) are serially sent to the microcontroller to identify the bits to be written in the FIFORSTREG.  

bit 7-4  
**FFBC<3:0>:** FIFO Fill Bit Count bits  
Sets the received bits before generating an external interrupt to the host microcontroller to indicate the receive FIFO is ready to be read. The maximum fill level is 15\(^1\).  

bit 3  
**SYCHLEN:** Synchronous Character Length bit  
This bit sets the synchronous character length to byte or word long\(^2\).  
1 = Byte long. User-programmable SCL0 byte is used.  
0 = Word long. The character is composed of the SCL1 and SCL0 bytes. The SCL1 byte value is fixed and is not configurable. The SCL0 byte value is user-programmable through the SYNBREG.  

bit 2  
**FFSC:** FIFO Fill Start Condition bit  
This bit sets the condition at which the FIFO starts filling with data.  
1 = The FIFO will continuously fill irrespective of noise or good data  
0 = The FIFO will fill when it recognizes the synchronous character pattern as defined internally  

bit 1  
**FSCF:** FIFO Synchronous Character Fill bit  
1 = The FIFO starts filling with data when it detects the synchronous character pattern as defined in the FFSC bit  
0 = The FIFO fill stops  
To restart the synchronous character pattern recognition, just clear and set this bit\(^2\).  

bit 0  
**DRSTM:** Disable (Sensitive) Reset mode bit  
1 = Disables\(^3\)  
0 = Enables System Reset for any glitches above 0.2V in the power supply  

Note 1:  
On register overrun, the data will be lost. Therefore, the developer must take into account the processing time required to read-out data before a register overrun. It is recommended to set the fill value to half of the desired number of bits to be read to ensure sufficient time for additional processing. See Register 2-1 for the description of the TXRXFIFO and TXUROW bits, and Register 2-9 for details on polling and interrupt driven FIFO reads from the SPI bus.  

2:  
For synchronous character length selection, see Table 2-8.  
3:  
For Reset mode selection, see Table 2-9.
### TABLE 2-8: SYNCHRONOUS CHARACTER SELECTION

<table>
<thead>
<tr>
<th>SYCHLEN</th>
<th>SCL1</th>
<th>SCL0</th>
<th>Synchronous Character</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NA</td>
<td>0xD4</td>
<td>0xD4 (byte long)</td>
</tr>
<tr>
<td>0</td>
<td>0x2D</td>
<td>0xD4</td>
<td>0x2DD4 (word long)</td>
</tr>
</tbody>
</table>

### TABLE 2-9: RESET MODE SELECTION

<table>
<thead>
<tr>
<th>DRSTM</th>
<th>Reset mode</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Normal Reset</td>
<td>Reset is triggered when VDD is below 250 mV</td>
</tr>
<tr>
<td>0</td>
<td>Sensitive Reset</td>
<td>Reset is triggered when VDD is below 1.6V and VDD glitch is greater than 600 mV</td>
</tr>
</tbody>
</table>

**Note:** See Appendix A: “Read Sequence and Packet Structures” for FIFO packet structures.
## REGISTER 2-11: SYNBREG: SYNCHRONOUS BYTE CONFIGURATION REGISTER

**(POR: 0xCED4)**

<table>
<thead>
<tr>
<th></th>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-1</th>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CCB&lt;15:8&gt;</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>bit 15</strong></td>
<td>W-1</td>
<td>W-1</td>
<td>W-0</td>
<td>W-0</td>
<td>W-1</td>
<td>W-0</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>bit 8</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SYNCB&lt;7:0&gt;</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>bit 7</strong></td>
<td>W-1</td>
<td>W-1</td>
<td>W-0</td>
<td>W-1</td>
<td>W-0</td>
<td>W-0</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>bit 0</strong></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

### Legend:
- **r** = reserved bit
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as '0'
- **-n** = Value at POR
  - ‘1’ = Bit is set
  - ‘0’ = Bit is cleared
  - **x** = Bit is unknown

**bit 15-8  **  **CCB<15:8>:**  **Command Code bits**
The command code bits (11001110b) are serially sent to the microcontroller to identify the bits to be written in the SYNBREG.

**bit 7-0  **  **SYNCB<7:0>:**  **Synch Byte Configuration bits**
The SYNBREG assigns the value to SCL0 of the synchronous character in the FIFORSTREG. The value is valid for a byte or word long synchronous character.
**REGISTER 2-12: DRSREG: DATA RATE VALUE SET REGISTER (POR: 0xC623)**

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
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<tbody>
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<td></td>
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<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

**Legend:**
- `r` = reserved bit
- `R` = Readable bit
- `W` = Writable bit
- `U` = Unimplemented bit, read as '0'
- `-n` = Value at POR
- `'1'` = Bit is set
- `'0'` = Bit is cleared
- `x` = Bit is unknown

**Column 15-8:**
- **CCB<15:8>:** Command Code bits
  - The command code bits (11000110b) are serially sent to the microcontroller to identify the bits to be written in the DRSREG.

**Column 7:**
- **DRPE:** Date Rate Prescaler Enable bit
  - `1` = Enables the prescaler to obtain smaller values of expected data rates. The prescaler value when enabled is approximately 1/8 of the actual data rate.
  - `0` = Disables the prescaler

**Column 6-0:**
- **DRPV<6:0>:** Data Rate Parameter Value bits
  - These bits represent the decimal value of the 7-bit parameter which is used to calculate the expected data rate.

**Note 1:** To calculate the expected data rate, use Equation 2-4. To calculate the DRPV<6:0> decimal value for a given bit rate, use Equation 2-5. If the prescaler is not used, the data rates range from 2.694 kbps–344.828 kbps. With the prescaler enabled, the data rates range from 337 bps to 43.103 kbps. The Slow Clock Recovery mode requires more accurate bit timing when setting the data rate. Equation 2-6 is used to calculate the data rate accuracy for Fast and Slow modes.

**EQUATION 2-4:**

\[
DREx (kbps) = \frac{10000}{[29 \times (DRPV<6:0> + 1) \times (1 + DRPE \times 7)]}
\]

where:
- `DRPV<6:0>` is the Decimal Value from 0 to 127 and the Prescaler (DRPE) is ‘1’ (if ON) or ‘0’ (if OFF).

**EQUATION 2-5:**

\[
DRPV<6:0> = \frac{10000}{[29 \times (1 + DRPE \times 7) \times DREx]} - 1
\]

where:
- `DREx` is the Expected Data Rate.

**EQUATION 2-6:**

- Slow mode Accuracy (SMA) = \(\Delta DR/DR < 1/(29 \times LN)\)
- Fast mode Accuracy (FMA) = \(\Delta DR/DR < 3/(29 \times LN)\)

where:
- `LN` is the longest number of expected 1’s or 0’s in the data stream.
- `\Delta DR` is the difference in the actual data rate versus the set data rate in the transmitter.
- `DR` is the expected data rate set using `DRPV<6:0>`.
REGISTER 2-13: PMCREG: POWER MANAGEMENT CONFIGURATION REGISTER (POR: 0x8208)

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-1</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>bit 15</td>
<td>bit 8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXCEN</td>
<td>BBCEN(1)</td>
<td>TXCEN</td>
<td>SYEN</td>
<td>OSCEN</td>
<td>LBDEN</td>
<td>WUTEN(3)</td>
<td>CLKOEN</td>
</tr>
<tr>
<td>bit 7</td>
<td>bit 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Legend:
- \( r \) = reserved bit
- \( R \) = Readable bit
- \( W \) = Writable bit
- \( U \) = Unimplemented bit, read as ‘0’
- \( \text{-n} \) = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- \( x \) = Bit is unknown

bit 15-8  **CCB<15:8>: Command Code bits**
The command code bits\( (10000010b) \) are serially sent to the microcontroller to identify the bits to be written in the PMCREG.

bit 7  **RXCEN**: Receiver Chain Enable bit
The receiver chain consists of a baseband circuit, synthesizer and crystal oscillator.
- 1 = Enables receiver chain
- 0 = Disables receiver chain

bit 6  **BBCEN**: Baseband Circuit Enable bit\(^{(1)}\)
The baseband circuit, synthesizer and oscillator work together to demodulate and recover the data transmitted to the synthesizer (SYEN bit). The OSCEN bit must be enabled along with the baseband circuits in order to receive data.
- 1 = Enables baseband circuit
- 0 = Disables baseband circuit

bit 5  **TXCEN**: Transmit Chain Enable bit
The transmit chain consists of power amplifier, synthesizer, oscillator and transmit register.
- 1 = Enables the transmitter chain and starts transmission (if the TX register is enabled)
- 0 = Disables transmitter chain

bit 4  **SYEN**: Synthesizer Enable bit
The synthesizer consists of a PLL, oscillator and VCO for controlling the channel frequency.
- 1 = Enables the synthesizer
- 0 = Disables the synthesizer

bit 3  **OSCEN**: Crystal Oscillator Enable bit
- 1 = Enables the crystal oscillator
- 0 = Disables the crystal oscillator

bit 2  **LBDEN**: Low Battery Detector Enable bit
The battery detector can be programmed to 32 different threshold levels\(^{(2)}\).
- 1 = Enables the battery voltage detector circuit
- 0 = Disables the battery voltage detector circuit

bit 1  **WUTEN**: Wake-up Timer Enable bit\(^{(3)}\)
- 1 = Enables the wake-up timer circuit
- 0 = Disables the wake-up timer circuit

**Note 1:** This bit can be disabled to reduce current consumption.

2: See BCSREG (Register 2-16) for programming details.

3: See WTSREG (Register 2-14) for details on programming the wake-up timer value.

4: If the CLKOEN bit is cleared by enabling the clock output, the oscillator continues to run even if the OSCEN bit is cleared. The device will not fully enter into the Sleep mode.
bit 0  **CLKOEN:** Clock Output Enable bit
On-chip Reset or power-up clock output is enabled so that a processor can execute any special setup
sequences as required by the designer\(^2\).
\(1\) = Disables the clock output
\(0\) = Enables the clock output\(^4\)

**Note 1:** This bit can be disabled to reduce current consumption.

2: See BCSREG (Register 2-16) for programming details.

3: See WTSREG (Register 2-14) for details on programming the wake-up timer value.

4: If the CLKOEN bit is cleared by enabling the clock output, the oscillator continues to run even if the
OSCEN bit is cleared. The device will not fully enter into the Sleep mode.
REGISTER 2-14: WTSREG: WAKE-UP TIMER VALUE SET REGISTER (POR: 0xE196)

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCB&lt;15:13&gt;</td>
<td>W-0</td>
<td>W-0</td>
<td>W-0</td>
<td>W-0</td>
<td>W-0</td>
<td>W-0</td>
<td>W-0</td>
</tr>
</tbody>
</table>

Legend:
- \( r \) = reserved bit
- \( R \) = Readable bit
- \( W \) = Writable bit
- \( U \) = Unimplemented bit, read as ‘0’
- \( -n \) = Value at POR
  - ‘1’ = Bit is set
  - ‘0’ = Bit is cleared
  - \( x \) = Bit is unknown

bit 15-13  \( \text{CCB}<15:13> \): Command Code bits
The command code bits (111b) are serially sent to the microcontroller to identify the bits to be written in the WTSREG.

bit 12-8  \( \text{WTEV}<4:0> \): Wake-up Timer Exponential Value bits
These bits define the exponential value to be used to set up the time interval. The value must be a decimal equivalent between 0 and 29\(^1\).

bit 7-0  \( \text{WTMV}<7:0> \): Wake-up Timer Multiplier Exponential Value bits
These bits define the multiplier value to be used to set up the time interval. The value must be a decimal equivalent between 0 and 255\(^1\).

Note 1: The WTSREG sets the wake-up interval for the device. After setting the wake-up time, the WUTEN bit (PMCREG<1>) must be cleared and set at the end of every wake-up cycle. The wake-up duration can be calculated using Equation 2-7.

EQUATION 2-7:

\[
\text{WUTIME (ms)} = [1.03 \times \text{WTMV}<7:0> \times 2^{\text{WTEV}<4:0>}] + 0.5 \text{ ms}
\]

where:
- \( \text{WTMV}<7:0> \) = Decimal Value between 0 to 255
- \( \text{WTEV}<4:0> \) = Decimal Value between 0 to 29
## REGISTER 2-15: DCSREG: DUTY CYCLE VALUE SET REGISTER (POR: 0xC80E)

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CCB&lt;15:8&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **r** = reserved bit
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- **x** = Bit is unknown

**bit 15 - 8:** CCB<15:8>: Command Code bits
The command code bits (11001000b) are serially sent to the microcontroller to identify the bits to be written in the DCSREG.

**bit 7 - 1:** DCMV<6:0>: Duty Cycle Multiplier Value bits
These bits are used to calculate the duty cycle or on time of the receiver after the wake-up timer has brought the MRF49XA out of Sleep mode.

**bit 0:** DCMEN: Duty Cycle mode Enable bit
1 = Enables the Duty Cycle mode
0 = Disables the Duty Cycle mode

**Note 1:** For operation in Duty Cycle mode, the receiver must be disabled (RXCEN = 0) and the wake-up timer must be enabled (WUTEN = 1) in PMCREG. The registers, DCSREG and WTSREG, can be used to reduce the current consumption of the receiver. The DCSREG can be set up so that when the wake-up timer brings the MRF49XA out of Sleep mode, the receiver is turned on for a short period to sample the signal presence before returning to Sleep. The process in the Duty Cycle mode starts over. The duty cycle uses the multiplier value of the wake-up timer, in parts for its calculation, as shown in Equation 2-8.

### EQUATION 2-8:

\[
DC = \frac{[(DCMV<7:1> \times 2 + 1)]}{[WTMV<7:0> \times 100\%]} 
\]

where:
- **WTMV** is WTMV<7:0> bits of the WTSREG.
REGISTER 2-16: BCSREG: BATTERY THRESHOLD DETECT AND CLOCK OUTPUT VALUE SET REGISTER (POR: 0xC000)

<table>
<thead>
<tr>
<th>W-1</th>
<th>W-1</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
<th>W-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- **r** = reserved bit
- **R** = Readable bit
- **W** = Writable bit
- **U** = Unimplemented bit, read as ‘0’
- **-n** = Value at POR
  - ‘1’ = Bit is set
  - ‘0’ = Bit is cleared
  - x = Bit is unknown

**bit 15-8**  **CCB<15:8>:** Command Code bits
The command code bits (11000000b) are serially sent to the microcontroller to identify the bits to be written in the BCSREG.

**bit 7-5**  **COFSB<2:0>:** Clock Output Frequency Set bits
These bits set the output clock frequency which can be used to run an external host microcontroller.
- 111 = 10 MHz
- 110 = 5 MHz
- 101 = 3.33 MHz
- 100 = 2.5 MHz
- 011 = 2 MHz
- 010 = 1.66 MHz
- 001 = 1.25 MHz
- 000 = 1 MHz

**bit 4**  **Reserved:** Write as ‘0’

**bit 3-0**  **LBDVB<3:0>:** Low Battery Detect Value bits
These bits set the decimal value to calculate the battery detect threshold voltage level (1,2).

**Note 1:** When the battery level goes down by 50 mV below this value, the LBTD bit (STSREG<10>) is set, indicating that the battery level is below the programmed threshold. This is useful in monitoring discharge-sensitive batteries, such as Lithium cells. The low battery detect can be enabled by setting the LBDEN bit (PMCREG<2>) and can be disabled by clearing the bit.

**2:** The low battery threshold value is programmable from 2.2V – 3.8V by using Equation 2-9.

**EQUATION 2-9:**

\[
\text{Threshold Voltage Value} = 2.25 + [0.1 \times (\text{LBDVB}<3:0>)]
\]

where:
- LBDVB<3:0> is the Decimal Value from 0 to 15.
### REGISTER 2-17: PLLCREG: PLL CONFIGURATION REGISTER (POR: 0xCC77)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>15-8</th>
<th>7-0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>CCB&lt;15:8&gt;:</strong> Command Code bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>The command code bits (11001100b) are serially sent to the microcontroller to identify the bits to be written in the PLLCREG.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td><strong>Unimplemented:</strong> Write as '0'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6-5</td>
<td><strong>CBTC&lt;1:0&gt;:</strong> Clock Buffer Time Control bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>These bits control the rise and fall time for the clock buffer which is dependant on the output clock frequency from the BCSREG.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>11 = 5 MHz - 10 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10 = 3.3 MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>01 = 2.5 MHz or less</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>00 = 2.5 MHz or less</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td><strong>Reserved:</strong> Masked to '1'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td><strong>PDDS:</strong> Phase Detector Delay Switch bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Enables the phase detector delay function</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Disables the phase detector delay function</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td><strong>PLLDD:</strong> PLL Dithering Disable bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = Disables PLL dithering</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = Enables PLL dithering</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td><strong>Reserved:</strong> Write as '1'</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td><strong>PLLBWB:</strong> PLL Bandwidth bit</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Enabling the bit configures higher data rates, faster settling and reduced phase noise; thus, resulting in a better RF performance.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 = -102 dBc/Hz, &gt; 90 kbps (max 256 kbps)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 = -107 dBc/Hz, &lt; 90 kbps (max 86.2 kbps)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### TABLE 2-10: CONTROL/COMMAND REGISTER MAP

<table>
<thead>
<tr>
<th>Reg. Name</th>
<th>Bit 15</th>
<th>Bit 14</th>
<th>Bit 13</th>
<th>Bit 12</th>
<th>Bit 11</th>
<th>Bit 10</th>
<th>Bit 9</th>
<th>Bit 8</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Value on POR</th>
</tr>
</thead>
<tbody>
<tr>
<td>STSREG</td>
<td>TXRXFIFO</td>
<td>POR</td>
<td>TXOWRXOF</td>
<td>WUTINT</td>
<td>LCEXINT</td>
<td>LBTD</td>
<td>FIFOEM</td>
<td>ATRSSI</td>
<td>DQDO</td>
<td>CLKRL</td>
<td>AFCCT</td>
<td>OFFS</td>
<td>OFFS&lt;3:0&gt;</td>
<td>OFFS&lt;5:0&gt;</td>
<td>0x0000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GENCREG</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>TXDEN</td>
<td>FIFOEN</td>
<td>FBS&lt;1:0&gt;</td>
<td>LCS&lt;3:0&gt;</td>
<td>0x8008</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AFCCREG</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>AUTOMS&lt;1:0&gt;</td>
<td>ARFO&lt;1:0&gt;</td>
<td>MFCS</td>
<td>HAM</td>
<td>FOREN</td>
<td>FOEN</td>
<td>0xC4F7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TXCREG</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>MODPLY</td>
<td>MODBW&lt;3:0&gt;</td>
<td>OFFS&lt;5:0&gt;</td>
<td>0x3900</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TXBREG</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x88AA</td>
<td></td>
</tr>
<tr>
<td>CFSREG</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0xA680</td>
<td></td>
</tr>
<tr>
<td>RXCREG</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x9080</td>
<td></td>
</tr>
<tr>
<td>BBFCREG</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>ACRLC</td>
<td>MCRLC</td>
<td>—</td>
<td>FTYPE</td>
<td>—</td>
<td>0</td>
<td>0x22C</td>
<td></td>
</tr>
<tr>
<td>RXFIFOREG</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x9000</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FIFORSTREG</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>FFBC&lt;3:0&gt;</td>
<td>SYCHLEN</td>
<td>FFSC</td>
<td>FSCF</td>
<td>DRSTM</td>
<td>0xCA80</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYNBREG</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>0xCED4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRSPREG</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>DRPE</td>
<td>DRPV&lt;6:0&gt;</td>
<td>0x623</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PMCREG</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>RXCEN</td>
<td>BBCEN</td>
<td>TXCEN</td>
<td>SYEN</td>
<td>OSCEN</td>
<td>LBDEN</td>
<td>WUTEN</td>
<td>CLKEN</td>
</tr>
<tr>
<td>WTSREG</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>RXCEN</td>
<td>BBCEN</td>
<td>TXCEN</td>
<td>SYEN</td>
<td>OSCEN</td>
<td>LBDEN</td>
<td>WUTEN</td>
<td>CLKEN</td>
</tr>
<tr>
<td>DCSREG</td>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>DCMV&lt;6:0&gt;</td>
<td>DCM&lt;6:0&gt;</td>
<td>0x80E0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BCSREG</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>COFSB&lt;2:0&gt;</td>
<td>—</td>
<td>—</td>
<td>LBDVB&lt;3:0&gt;</td>
<td>0x3D00</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PLLCREG</td>
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<td>0</td>
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<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>—</td>
<td>CBTC&lt;1:0&gt;</td>
<td>1</td>
<td>PDDS</td>
<td>PLLDD</td>
<td>—</td>
<td>PLLBWB</td>
<td>0xCC77</td>
</tr>
</tbody>
</table>
3.0 FUNCTIONAL DESCRIPTION

The MRF49XA is a low-power, Zero-IF, multi-channel FSK transceiver which operates in the 433, 868 and 915 MHz frequency bands. All the RF and baseband functions and processes are integrated in the MRF49XA. The device for its operation requires only a single, 10 MHz crystal as a reference source and an external, low-cost host microcontroller. The MRF49XA supports the following functions:

- Reset
- PA and LNA
- Synthesizer (PLL, VCO and Oscillator)
- I/Q Mixers and Demodulators
- BBFs and Amplifiers
- Received Signal Strength Indicator
- Low Battery Detector
- Wake-up Timer/Low Duty Cycle mode
- DQI

The MRF49XA is the best option for FHSS applications requiring frequency agility to meet Federal Communications Commission (FCC), Industry Canada (IC) or European Telecommunications Standards Institute (ETSI) requirements. The communication link can be created by just using the MRF49XA along with a low-cost microcontroller. The device uses the different power-saving modes to reduce the overall current consumption, and thereby, extends the battery life of the system or application.

3.1 Reset

The MRF49XA supports four types of Reset:

- Power-on Reset
- Power Glitch Reset
- Software Reset
- Reset Pin

3.1.1 POWER-ON RESET

The MRF49XA has a built-in Power-on Reset circuitry which automatically resets all control registers when power is applied. A delay of 100 ms is recommended after a power-up sequence in order to allow the VDD to reach the correct voltage level and to get stabilized to recognize an active-low Reset. In Reset mode, the device does not accept the control commands through the SPI.

After power-up, the supply voltage starts to rise above 0V. The Reset block has an internal ramping voltage reference level (Reset ramp signal) which rises at a 100 mV/ms (typical) rate. The device remains in the Reset state until the voltage difference between the actual VDD and the internal Reset ramp signal is higher than the Reset threshold voltage level (typically 600 mV). The device remains in Reset mode as long as the VDD voltage level is less than 1.6V (typical), irrespective of the voltage difference between the VDD and the internal ramp signal. Figure 3-1 graphically shows the POR example for VDD with respect to time conditions.

FIGURE 3-1: POWER-ON RESET EXAMPLE
3.1.2 POWER GLITCH RESET

Spikes or glitches are found on the VDD line if the power supply filtering is not satisfactory, or the internal resistance of the power supply is very high. So, in this case, the Sensitive Reset mode needs to be enabled. Here, the device Reset occurs due to the transients present on the VDD line.

The internal Reset block has two basic modes of operation:

• Sensitive Reset mode
• Normal Reset mode

**Sensitive Reset mode:** Enabling the Sensitive Reset, a Reset is generated if:

- the positive going edge of the VDD has a rising rate greater than 100 mV/ms, and
- the voltage difference between the internal ramp signal and the VDD reaches the Reset threshold voltage (600 mV).

The Sensitive Reset mode is the default mode which can be changed using the DRSTM bit (FIFORSTREG<0>). Figure 3-2 shows the Sensitive Reset mode.

**Normal Reset mode:** The device enters this mode, when the power glitch detection circuit is disabled. Figure 3-3 shows the Normal Reset mode.

**Note:** Negative change in the supply voltage does not cause a Reset event unless the VDD level reaches the Reset threshold voltage (i.e., 250 mV in Normal Reset mode, 1.6V in Sensitive Reset mode).

If the Sensitive mode is disabled and the power supply is turned off, the VDD requires 250 mV to trigger a Power-on Reset when the supply voltage is reapplied. If the decoupling capacitors retain their charges for a longer duration, there might be no Reset after power-up as the power glitch detector is disabled.

**Note:** The Reset event reinitializes the internal registers, and thus, the Sensitive mode is enabled again.

FIGURE 3-2: SENSITIVE RESET ENABLED

![Diagram showing Sensitive Reset enabled](image-url)
3.1.3 SOFTWARE RESET

The Software Reset is initiated using the host microcontroller. The 0xFE00 command triggers this Reset only if the Sensitive Reset mode is enabled. The hardware automatically clears the bit(s) to their power-on state. The Software Reset command is the same as POR, but the duration of the Reset event is much less than the actual POR (0.25 ms, typical).

3.1.4 RESET PIN

The MRF49XA has an open-drain Reset output with an internal pull-up and input buffer (active-low). The host microcontroller resets the MRF49XA by asserting the RESET pin to low (see Figure 3-4). All control registers are reset to their POR values. The RESET pin consists of an internal weak pull-up resistor. In order to allow the RF circuitry to start-up and get stabilized, a delay of around 0.25 ms is recommended for accessing the MRF49XA after a hardware Reset.

The registers associated with Reset are:
- STSREG (see Register 2-1)
- FIFORSTREG (see Register 2-10)
- WTSREG (see Register 2-14)

FIGURE 3-3: SENSITIVE RESET DISABLED

FIGURE 3-4: RESET PIN INTERNAL CONNECTION
3.2 VDD Line Filtering

During the Reset event (caused by power-on, glitch on the supply line or Software Reset), the VDD line should be kept clean. Noise or a periodic disturbing signal superimposed on the supply voltage may prevent the device from getting out of the Reset state. To avoid this, adequate filters should be made available on the power supply lines to keep the distorting signal level below 100 mVp-p, in the DC-50 kHz range for 200 ms, from VDD ramp start. The usage of regulators or SMPS may sometimes introduce switching noise on the VDD line, so follow the power supply manufacturer’s recommendations on how to decrease the ripple of regulator IC and/or how to shift the switching frequency while using SMPS.

The registers associated with power line filtering are:

- STSREG (see Register 2-1)
- FIFORSTREG (see Register 2-10)
- WTSREG (see Register 2-14)
3.3 Power and Low Noise Amplifiers

The PA is an open-collector, differential output with programmable output power which can directly drive a loop or dipole antenna, and with proper matching, can also drive a monopole antenna. An automatic antenna tuning circuit configured in the PA avoids the manual tuning during production and this offsets “hand effects”.

The registers associated with the PA are:

- TXCREG (see Register 2-4)
- PMCREG (see Register 2-13)

The input LNA has selectable gain (0 dB, -6 dB, -14 dB and -20 dB) which is useful in environments with strong interferers. The LNA has 250Ω of differential input impedance, which requires a matching circuit when connected to 50 Ω devices.

The registers associated with the LNA are:

- RXCREG (see Register 2-7)
- PMCREG (see Register 2-13)

3.4 Crystal Oscillator and Clock Output

The MRF49XA has a single pin crystal oscillator circuit, which provides a 10 MHz reference signal for the on-chip PLL. The clock frequency is programmable from eight predefined frequencies, each being a prescaled value of a 10 MHz crystal reference. A programmable crystal load capacitor has been internally configured to reduce the external component count and to have a much simplified design. The internal load capacitor is programmable from 8.5 pF – 16 pF in 0.5 pF steps as defined GENCREG. This provides the advantage of accepting a wide range of crystals from different manufacturers with different load capacitance requirements. For load capacitance values, see Table 3-1. These values are programmable through the BCSREG (see Register 2-16).

The crystal oscillator circuit is sensitive to parasitic capacitance for start-up. A small amount of parasitic capacitance is needed to facilitate oscillation. To achieve this, create a ground plane around the crystal and widen the connection to the MRF49XA. This is to adjust the reference frequency and to compensate for stray capacitance that might be introduced due to PCB layout. If the layout is not possible, a 0.5 pF – 1 pF capacitor, soldered across the crystal, will initiate the start-up. Also, see Section 3.6, Crystal Selection Guidelines for selecting the right crystal.

### TABLE 3-1: PROGRAMMABLE LOAD CAPACITANCE VALUE

<table>
<thead>
<tr>
<th>CAP3</th>
<th>CAP2</th>
<th>CAP1</th>
<th>CAP0</th>
<th>Load Capacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>8.5</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>9</td>
</tr>
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<td>1</td>
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<td>10.5</td>
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<td>0</td>
<td>11.5</td>
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<td>1</td>
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<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>16</td>
</tr>
</tbody>
</table>

The crystal oscillator provides a reference signal to the RF synthesizer, baseband circuits and digital signal processing parts. If receiver or transmitter blocks are used frequently, it is recommended to leave the oscillator running because the crystal might need a few milliseconds to start and stabilize. The stabilization time mainly depends on the crystal parameters.

The CLKOEN bit (PMCREG<0>) is used to enable or disable the clock output.

3.4.1 CLOCK TAIL FEATURE

The MRF49XA provides the clock signal for the microcontroller for accurate timing, and thus, removes the need for a second crystal for any board design. When the microcontroller turns off the crystal oscillator by clearing the OSCEN bit (PMCREG<3>), the MRF49XA provides a fixed number (192) of further clock pulses for the microcontroller to switch itself to Idle or Sleep mode (Low-Power Consumption modes). To use this feature, STSREG must be read before the OSCEN bit is set to ‘0’. If STSREG is not read, then the clock output will not shut down. If the CLKOUT pin is not used, it is suggested to turn off the output buffer from PMCREG.

**Note:** Leaving blocks needlessly turned on increases the current consumption, and thus, reduces the battery life.

The microcontroller clock source (if the clock is not supplied by the MRF49XA) should be stable enough over temperature and voltage ranges to ensure a minimum of 16 bits time delay under all operating circumstances.
3.4.2 AUTO CRYSTAL OSCILLATOR

When an interrupt occurs, irrespective of the OSCEN bit setting, the crystal oscillator automatically turns on to supply a clock signal to the microcontroller. After clearing all interrupts and reading the STSREG, the crystal oscillator is automatically turned off. The clock tail feature provides enough clock pulses for the microcontroller to enter the Low-Power mode. Due to this automatic feature, it is not possible to turn off the crystal by clearing the OSCEN bit if any interrupt is active. For example, after power-on, the POR interrupt must be cleared by reading STSREG and then writing '0' to the OSCEN bit puts the part in Sleep mode. It is necessary to clear all interrupts before turning the OSCEN bit off as the extra current required for running the crystal oscillator can shorten the battery life significantly.

On disabling the clock output (CLKOEN = 1), both the clock tail and auto crystal oscillator usage features are turned off. Only the OSCEN bit controls the crystal oscillator (considering that both RXCEN and TXCEN bits are cleared); the interrupts have no effect on it.

The registers associated with the crystal oscillator and clock are:

- STSREG (see Register 2-1)
- AFCCREG (see Register 2-3)
- PMCREG (see Register 2-13)
- BCSREG (see Register 2-16)
- PLLCREG (see Register 2-17)

3.5 Phase-Locked Loop

The synthesizer consists of a PLL, oscillator and VCO for controlling the channel frequency. The synthesizer must be enabled when either the transmitter or the receiver is enabled. For faster RX/TX switching, the synthesizer block must be kept on. Enabling the transmitter using the TXCEN bit (PMCREG<5>) will turn on the PA, and since the synthesizer is already up and running, the PA immediately produces the TX signal at the output. The oscillator must also be enabled to provide the reference frequency for the PLL. On power-up, the synthesizer performs the calibration automatically. The synthesizer also has an internal start-up calibration procedure. If there are significant changes in voltage or temperature, recalibration should be performed by simply disabling the synthesizer and re-enabling it. When set, the SYNEN bit (PMCREG<4>) enables the synthesizer.

The PLL circuit automatically performs the fine adjustment of carrier frequency. This way, the receiver can minimize the offset between a transmit and receive frequency. The frequency control function can be enabled or disabled through AFCCREG. The range of offset can be programmed and the offset value is calculated and added to the frequency control word within the PLL to incrementally change the carrier frequency. The MRF49XA can be programmed to automatically change and control the carrier frequency. The carrier frequency can also be manually activated by a strobe signal.

The oscillator provides the reference signal to the RF synthesizer to set up the transmit or receive frequency. The crystal oscillator also provides a reference signal to the RF, baseband circuits and microcontroller interface.

The PLL Configuration register configures the following:

- Output clock buffer slew rate
- Crystal start-up time
- Phase detector delay
- PLL dithering
- PLL bandwidth

The dithering reduces the noise error when calculating the fractional-N synthesizer code. When the PLLDD bit (PLLCREG<2>) is cleared, dithering is enabled and the settling time is slightly increased. The PLL bandwidth can accommodate higher data rates above 90 kbps. The reduced PLL bandwidth allows faster settling time and reduced phase noise, and thus, results in a better RX performance. See Register 2-17 for details on PLL setting and configuration.

The registers associated with the PLL are:

- STSREG (see Register 2-1)
- AFCCREG (see Register 2-3)
- PMCREG (see Register 2-13)
- BCSREG (see Register 2-16)
- PLLCREG (see Register 2-17)
3.6 Crystal Selection Guidelines

The crystal oscillator of MRF49XA requires a 10 MHz Parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF – 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF – 20 pF, so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF, and a worst case 7 pF Shunt Capacitance (Cs) value is expected for the crystal, the oscillator is able to start-up with any crystal having less than 100Ω Equivalent Series Loss Resistance (ESR). However, the low Cs and ESR values ensure the faster oscillator start-up.

The Crystal Frequency (fref) is used as the reference of the PLL, which generates the Local Oscillator Frequency (fLO). Therefore, fLO is directly proportional to fref. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable local oscillator frequency error.

Whenever a low-frequency error is essential for the application, it is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the “midrange”; for example, 16 pF. The “pull-ability” of the crystal is defined by its Motional Capacitance (Cm) and shunt capacitance.

FIGURE 3-5: MAXIMUM CRYSTAL TOLERANCES INCLUDING TEMPERATURE AND AGING (ppm)

<table>
<thead>
<tr>
<th>Bit Rate: 2.4 kbps</th>
<th>Deviation [± kHz]</th>
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</thead>
<tbody>
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</tr>
<tr>
<td>868 MHz</td>
<td>10</td>
</tr>
<tr>
<td>915 MHz</td>
<td>10</td>
</tr>
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</table>

<table>
<thead>
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<th>Deviation [± kHz]</th>
</tr>
</thead>
<tbody>
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</tr>
<tr>
<td>868 MHz</td>
<td>8</td>
</tr>
<tr>
<td>915 MHz</td>
<td>8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
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<th>Deviation [± kHz]</th>
</tr>
</thead>
<tbody>
<tr>
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<td>Do Not Use</td>
</tr>
<tr>
<td>868 MHz</td>
<td>Do Not Use</td>
</tr>
<tr>
<td>915 MHz</td>
<td>Do Not Use</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit Rate: 115.2 kbps</th>
<th>Deviation [± kHz]</th>
</tr>
</thead>
<tbody>
<tr>
<td>433 MHz</td>
<td>Do Not Use</td>
</tr>
<tr>
<td>868 MHz</td>
<td>Do Not Use</td>
</tr>
<tr>
<td>915 MHz</td>
<td>Do Not Use</td>
</tr>
</tbody>
</table>
3.7 Automatic Frequency Control

The AFC block operates in two modes and these modes depend on the strobe signals which are governed by the MFCS bit (AFCCREG<3>). The two operating modes are as follows:

- Manual mode
- Automatic mode

**Manual mode:** In this mode, the microcontroller provides the manual frequency control strobe signal. See Register 2-3 (AFCCREG) for more details. One measurement cycle can compensate for around 50% – 60% of the actual frequency offset. Two measurement cycles can compensate for 80% and three measurement cycles can compensate for 92% of the actual frequency offset. The AFCCT bit (STSREG<5>) is used to determine when the actual measurement cycle has been completed.

**Automatic mode:** In this mode, the strobe signal from the microcontroller is not required to update the Frequency Offset register block, as shown in Figure 3-6. The AFC circuit is automatically enabled when the DIO indicates the potential incoming signal during the entire measurement cycle and measures the same result in two subsequent cycles. Without AFC, the transmitter and the receiver need to be tuned precisely to the same frequency. The RX/TX frequency offset can lower the range. The units must be adjusted carefully during the production. To avoid drift, a stable and efficient crystal must be used or the output power needs to be increased to compensate for yield loss.

The AFC block calculates the TX/RX offset using the OFFSB bits (STSREG<3:0>). This value is used to pull the RX synthesizer close to the transmitter frequency. The benefits of the AFC feature are:

- Low-cost crystal can be used
- Temperature or aging drift will not cause range loss
- Production alignment is not needed

Figure 3-6 depicts the AFC circuit for frequency offset correction.

The Automatic mode Selection bits, AUTOMS<1:0> (AFCCREG<7:6>), select the type of operation (automatic or manual) for performing the AFC based on the status of the MFCS bit (AFCCREG<3>). There are four types of operation modes for controlling the frequency:

1. (AUTOMS1 = 0, AUTOMS0 = 0): Automatic operation of AFC is off. The MFCS bit is controlled by the microcontroller.
2. (AUTOMS1 = 0, AUTOMS0 = 1): The circuit measures the frequency offset only once after power-up. Hence, extended TX to RX distance can be achieved. In the actual application, when the user applies a battery, the circuit measures and compensates for the frequency offset caused by the crystal tolerances. This method allows the use of a low-cost quartz crystal in the application and provides protection against interference.
3. (AUTOMS1 = 1, AUTOMS0 = 0): The frequency offset is automatically calculated and the center frequency is corrected when the DIO is high. When DIO goes low, the calculated value is dropped.

The two methods recommended for improving the accuracy of the AFC calculation are as follows:

- The transmit package should start with a low effective baud rate pattern (i.e., 00110011b) as it is easier to receive. The circuit automatically measures the frequency offset during this initial pattern and changes the receiving frequency accordingly. The remaining part of the package will be received by the corrected frequency settings.
- The transmitter sends the first part of the packet with a higher deviation step than required during normal operation to help reception. After the frequency shift correction, the deviation can be reduced.

In both methods, when the DIO indicates poor receiving conditions (i.e., when DIO goes low), the output register is automatically cleared. This mode (Drop Offset mode) is used when the receiver communicates with more than one transmitter.

4. (AUTOMS1 = 1, AUTOMS0 = 1): This mode (Keep Offset mode) is similar to Drop Offset mode, but is recommended for use when the receiver communicates with only one transmitter. After a complete measuring cycle, the measured value is kept independent of the state of the DIO signal. In this mode, the DRSSI limit should be carefully selected to minimize the range hysteresis.

The AFC Offset Value (OFFSB<3:0> bits in the status word) is represented as a two’s complement number. The actual frequency offset is calculated as the AFC offset value multiplied by the current PLL frequency step (see Register 2-6 for more details).

The actual RX/TX offset can be monitored by using the status word (i.e., AFCCCT bit) included in the status word of the receiver. By reading out the status word, the actual measured offset frequency can be derived. To get accurate values, the AFC has to be disabled during read by clearing the FOFEN bit (AFCCREG<0>).

The registers associated with AFC are:

- STSREG (see Register 2-1)
- AFCCREG (see Register 2-3)
- CFSREG (see Register 2-6)
- RXCREG (see Register 2-7)
- PLLCREG (see Register 2-17)
FIGURE 3-6: AFC CIRCUIT FOR FREQUENCY OFFSET CORRECTION

Baseband Signal IN

Digital AFC Core Logic

Digital Limiter
If IN > MaxDEV then, OUT = MaxDEV
If IN < MinDEV then, OUT = MinDEV
ELSE, OUT = IN

7-Bit Frequency Offset Register

12-Bit ADDER

Corrected Frequency Parameter to Synthesizer

Parameter from Frequency Control Word

Signals for Auto Operation modes

Auto Operation AUTO<1:0>
Enable Calculation FIFOEN
Range Limit ARFO<1:0>
Strobe MFCS
Output Enable FOREN
3.8 Initialization

Certain control register values must be initialized for the basic operations of MRF49XA. These values differ from the Power-on Reset values and provide improved operational parameters. These settings are normally made once after a Reset. After initialization, the MRF49XA device features can be configured for the application. Here, accessing a register is implied as a command to the MRF49XA device through the SPI port. The steps to be followed for the initialization of MRF49XA using the control registers are as follows:

1. Set FIFORSTREG.
2. Enable synchronous latch from FIFORSTREG.
3. Program frequency band and crystal load capacitance from GENCREG.
4. Enable AFC function from AFCCREG.
5. Set center frequency through CFSREG for transmit or receive frequency.
6. Set data rate through DRSREG.
7. Enable required functions (transmit, receive, etc.) from PMCREG.
8. Configure RXCREG.
9. Configure TXCREG.
10. Tune in the antenna.
11. Turn off the transmitter and turn on the receiver.
12. Enable FIFO for data reception.
13. Set FIFORSTREG.
14. Enable synchronous latch from FIFORSTREG.
15. Read STSREG.

The following steps should be followed to tune in the antenna section:

1. Turn on the transmitter section from PMCREG.
2. Wait for 5 ms for the oscillator to get stabilized.

The registers associated with initialization are:

- STSREG (see Register 2-1)
- GENCREG (see Register 2-2)
- AFCCREG (see Register 2-3)
- TXCREG (see Register 2-4)
- CFSREG (see Register 2-6)
- RXCREG (see Register 2-7)
- FIFORSTREG (see Register 2-10)
- DRSREG (see Register 2-12)
- PMCREG (see Register 2-13)

3.9 Interrupts

The advanced interrupt handler circuit is implemented in the MRF49XA to reduce the power consumption. As mentioned, the Sleep mode is the lowest power consumption mode in which the mode clock and all functional blocks of the chip are disabled. However, the WUT and LBD circuits can be active if enabled. In case of any interrupt, the device wakes up, switches to the Active mode and an interrupt signal generated on the iRO pin of the device indicates the change in state or occurrence of an interrupt to the host microcontroller. The source of the interrupt is determined by reading the status word of the device (see Register 2-1).

The receiver generates an active-low interrupt request for the microcontroller at the following events:

- TXBREG is ready to receive the next byte
- RXFIFOREG has received the preprogrammed amount of bits
- RXFIFOREG overflow/TXBREG underrun
- Negative pulse on Interrupt Input pin (INT)
- Wake-up Timer Time-out (WUTINT)
- Supply voltage below the preprogrammed value is detected
- Power-on Reset
3.9.1 SETTING INTERRUPTS

The device’s interrupt pin (IRO) signals one of eight interrupt events to the host microcontroller. The interrupt source in the microcontroller is read out from the transceiver through the SDO pin. The interrupt sources that are available are briefly described in the following subsections.

3.9.1.1 TXRXFIFO: Transmit Register or Receive FIFO bit

1. Transmit mode: Transmit Register Ready bit
   This interrupt is generated when the Transmit register is empty. It is valid only when the TXDEN bit (GENCREG<7>) is set and the TXCEN bit (PMCREG<5>) is enabled.

2. Receive mode: Receive FIFO Empty bit
   This interrupt is generated when the bit level in the RXFIFOREG has reached the preprogrammed level. An interrupt is triggered when the number of received data bits in the receiver FIFO reaches the threshold set by the FFBC bits (FIFORSTREG<7:4>). This is valid only when the FIFOEN bit (GENCREG<6>) is set and the RXCEN bit (PMCREG<7>) is enabled.

3.9.1.2 POR: Power-on Reset Interrupt

The POR interrupt is generated when a change on the VDD line triggers an internal Reset circuit or a Software Reset was issued. For details, see Section 3.1, Reset.

3.9.1.3 TXOWRXOF: Transmit Overwrite Receive Overflow bit

1. Transmit mode: Transmit Register Underrun or Overwrite bit
   This interrupt is generated when the automatic Baud Rate Generator (BRG) has completed the transmission of a byte in TXBREG before the register write. It is valid only when the TXDEN bit (GENCREG<7>) is set and the TXCEN bit (PMCREG<5>) is enabled.

2. Receive mode: Receive FIFO Overflow bit
   This interrupt is generated when the bits received are more than the FIFO capacity (16 bits). This is valid only when the FIFOEN bit (GENCREG<6>) is set and the RXCEN bit (PMCREG<7>) is enabled.

3.9.1.4 WUTINT: Wake-up Timer Interrupt

This interrupt occurs when the time specified by the wake-up timer has elapsed. It is valid only when the WUTEN bit (PMCREG<1>) is set. The device periodically wakes up and switches to Receive mode. If valid FSK data is received, the device sends an interrupt to the microcontroller and continues filling the RXFIFO. After the completion of transmission, the FIFO is read out completely and all other interrupts are cleared. The device returns to the Low-Power Consumption mode.

3.9.1.5 LCEXINT: Logic Low-Level Change on External Interrupt

Follows the level of the INT pin if configured as an external interrupt by clearing the FINTDIO bit (RXCREG<15>).

3.9.1.6 LBTD: Low Battery Threshold Detect

This interrupt occurs when VDD goes below the programmable low battery detector threshold level configured by the LBDVB bits (BCSREG<3:0>). It is valid only when the LBDEN bit (PMCREG<2>) is set.

3.9.2 CLEARING INTERRUPTS

If any of the interrupt sources gets active, the IRO changes to logic low level and the corresponding interrupt bit in the status byte goes high. Clearing an interrupt implies:

• releasing the IRO pin to return to logic high, and
• clearing the corresponding interrupt bit in the STSREG

The clearing of each of the interrupts is briefly described in the following subsections.

3.9.2.1 TXRXFIFO

1. Transmit mode
   The IRO pin and its status bit remain active until the register is written (if underrun does not occur until the register write) or the transmitter and the TX latch are switched off.

2. Receive mode
   The IRO pin and its status bit remain active until the FIFO is read (receive FIFO interrupt threshold number of bits have been read). The receiver is switched off or the RXFIFO is switched off.

3.9.2.2 POR

The IRO pin and its status bit are cleared by reading the Status Read register.
3.9.2.3 TXOWRXOF

1. Transmit mode

In this mode, the TXOWRXOF and TXRXFIFO bits are always set together. The IRQ pin and its status bit remain active until the transmitter and the TX latch are switched off.

2. Receive mode

In this mode, the TXOWRXOF and TXRXFIFO bits are always set together and can be cleared by reading the STSREG. The IRQ pin and its status bit remain active until the FIFO is read (a FIFO interrupt threshold number of bits have been read), the receiver is switched off or the RX FIFO is switched off.

3.9.2.4 WUTINT

The IRQ pin and its status bit are cleared by reading the STSREG.

3.9.2.5 LCSEXINT

The IRQ pin and its status bit follow the level of the INTE pin.

3.9.2.6 LBTD

The IRQ pin is released by reading the status bit of STSREG, but the status bit remains active until the VDD is below the threshold value.

The MRF49XA interrupt generation logic is shown in Figure 3-7. A better way of interrupt handling is to first read the STSREG on an interrupt and then decide the action based on the status byte/word. It is important to note that any of the interrupt sources can wake-up the MRF49XA from Sleep mode. This means that the crystal oscillator starts to supply a clock signal to the microcontroller even if the microcontroller has its own clock source. The MRF49XA will not enter Sleep mode if any of the interrupt remains active, irrespective of the state of the OSCEN bit in PMCREG. This way, the microcontroller can always have a clock signal to process the interrupt.

To prevent high-current consumption, which results in short battery life, it is highly recommended to process and clear interrupts before entering Sleep mode. The functions which are not necessary should be turned off to avoid unwanted interrupts. Before finalizing the microcontroller (application) code, a thorough testing must be conducted to make sure that all interrupt sources are handled before putting the transceiver in Sleep mode.

The OSCEN bit controls the crystal oscillator (considering that the RXCEN and TXCEN bits are cleared) if the CLKOEN bit (PMCREG<0>) is set. The interrupts have no effect on it.

On interrupt, the crystal oscillator turns on automatically to supply a clock signal to the microcontroller, irrespective of the OSCEN bit setting. The clock tail feature provides sufficient clock pulses for the microcontroller to enter the Low-Power Consumption mode. Due to this automatic feature, it is not possible to turn off the crystal by clearing the OSCEN bit if any interrupt is active.

For example, after power-on, the POR interrupt must be cleared by a status read, and then by writing ‘0’ in the OSCEN bit, puts the device into Sleep mode.

Note: Before turning the OSCEN bit off, clear all the interrupts, because the additional current required for running the crystal oscillator can shorten the battery life significantly.

The registers associated with interrupts are:
- STSREG (see Register 2-1)
- GENCREG (see Register 2-2)
- RXCREG (see Register 2-7)
- PMCREG (see Register 2-13)
- BCSREG (see Register 2-16)

Note: Before turning the OSCEN bit off, clear all the interrupts, because the additional current required for running the crystal oscillator can shorten the battery life significantly.
FIGURE 3-7: MRF49XA INTERRUPT GENERATION LOGIC

TXRXFIFO  TXCEN
TXRXFIFO  RXCEN
RESET  (Ext./Int.)
TXOWRXOF  TXCEN
TXOWRXOF  RXCEN
WUTINT  WUTEN
LCEXINT (INT)  FINTDIO
LBTID  LBDEN

IRO
3.10  Baseband/Data Filtering

The baseband receiver has several programming options to optimize the communication for a wide range of applications. The programmable functions are as follows:

- Baseband Analog Filter
- Baseband Digital Filter
- Receive Bandwidth
- Receive Data Rate
- Clock Recovery

A suitable bandwidth should be used to achieve various FSK deviation, data rate and crystal tolerance requirements. The filter structure is a 7th order, Butterworth low-pass with 40 dB suppression at twice the bandwidth frequency. Offset cancellation is done by using a high-pass filter, with a cutoff frequency below 7 kHz, in order to achieve the best possible frequency response in baseband and a good flat response in the pass band. Figure 3-8 shows the full baseband amplifier transfer function. This optimizes the chip area, cost and channel separation.

![Full Baseband Amplifier Transfer Function (BW = 67 kHz)](image)

The receive bandwidth is programmable from 67 kHz to 400 kHz to accommodate various FSK modulation deviations. If the deviation is known for a given transmitter, good results are obtained with a bandwidth of at least twice the transmitter FSK deviation.

**EXAMPLE 3-1: FREQUENCY DEVIATION AND BBBW CALCULATION**

- Data Rate – 9.6 kbps
- Crystal Accuracy – 40 ppm
- Frequency Band – 915 MHz
- \( f_{\text{error}} \) by the Crystal: 40 \times \frac{915000}{1000000} = 36.6 kHz

\[
\text{Deviation} = \text{Data Rate} + 2 \times f_{\text{error}} + 10 = 9.6 + 2 \times 36.6 + 10 = 92.8 \text{ kHz}
\]

The closest possible deviation is 90 kHz.

\[
\text{BBBW} = \text{Deviation} \times 2 - 10 \text{ kHz} = 90 \times 2 - 10 = 170 \text{ kHz}
\]

The closest possible BBBW is 200 kHz.

The FSK modulated deviation for this example is shown in Figure 3-9.
The baseband filtering type can also be selected between an analog filter and a digital filter.

3.10.1 ANALOG FILTERING MODE

For analog filtering, a simple RC low-pass filter is used, along with a Schmitt Trigger circuit. The demodulator output is fed to the RCLKOUT/FCAP/FINT pin over a 10 kΩ resistor. The filter cut-off frequency is set by the external capacitor connected to this pin and VSS. A 10 kΩ resistor and the Schmitt Trigger are integrated on the chip. An external capacitor for the RC filter has to be chosen in accordance with the required bit rate. The receiver can handle up to 256 kbps of data rate in analog operation. The receive data rate is programmable from 337 bps to 256 kbps. An internal prescaler can be used to give better resolution when setting up the receive data rate. The prescaler is optional and can be disabled through DRSREG. The analog filtering does not use the FIFO and the clock. The clock is not provided for the demodulated data, and hence, there is no need for setting the correct bit rate.

3.10.2 DIGITAL FILTERING MODE

A digital filter is used with a clock frequency at 29 times the data rate. For digital filtering, the synchronized clock to the data is provided by the CLKRC. By using this clock, the received data can fill the FIFO. If the FIFO is not used, the recovered clock can be accessed through RCLKOUT/FCAP/FINT pin.

The CLKRC operates in three modes: Automatic mode, Slow mode and Fast mode. All three modes are configurable through BBFCREG. Each mode is dependent on the type of signals it uses to determine the valid data and also the number of incoming preamble bits present at the beginning of the packet. In Automatic mode, the CR CLKRC automatically switches between the Fast and Slow mode. The noise immunity of the CLKRC is very high in Slow mode; however, it has slower settling time and requires more accurate data timing than in Fast mode.

The registers associated with baseband filtering are:

- STSREG (see Register 2-1)
- RXCREG (see Register 2-7)
- BBFCREG (see Register 2-8)
- PMCREG (see Register 2-13)
3.11 Data Quality Indicator

The DQI is the digital processing part of the radio connected to the demodulating and functions when the receiver is on. This reports the reception of an FSK modulated RF signal. The DQI parameter setting defines how clean the incoming data stream would be stated as good data (valid FSK signal). The DIO signal goes high if the internally calculated data quality value exceeds the DIO threshold parameter, for five consecutive data bits, for both high and low periods.

The DQI parameter (i.e., Data Quality Threshold Indicator (DQTI) bit) value is calculated using the formula given in Equation 3-1.

**EQUATION 3-1:**

\[ DQI_{par} = 4 \times \frac{\text{Deviation} - \text{TX/RXoffset}}{\text{Bit Rate}} \]

The DQI parameter in BBFCREG should be chosen according to the following rules:

- The parameter should be > 4; otherwise, noise might be treated as a valid FSK signal
- The maximum value is 7

Even during the on-time calculation in the Low Duty Cycle mode, depending on the data quality threshold indicator, the device needs to receive a few valid data bits before the DQI signal indicates good signal condition (see Register 2-8). Selecting a short on-time can prevent the crystal oscillator from starting, or the DQI signal will not go high, even when the quality of the received signal is good.

The DIO is an extension of the DQI. When incoming data is detected, it uses the DQI signal, the clock recovery lock signal and the digital RSSI signal to determine if the incoming data is valid. The desired data rate and the acceptance criteria for valid data are user-programmable through the SPI port.

The DIO has three modes of operation: Slow, Medium and Fast. Each mode is dependent on the signals it uses to determine the valid data and also on the number of incoming preamble bits present at the beginning of the packet.

The DIO can be disabled by the user so that only raw data from the comparator comes out, or it can be set to accept only a preset range of data rates and data quality. The DIO saves the battery power and the time for a host microcontroller because it will not wake-up the microcontroller unless there is valid data present. See Register 2-7 (RXCREG) for setup details.

The DIO signal is valid when using the internal receive FIFO or an external pin to capture baseband data. DIO can be multiplexed to pin 16 for external usage. **Figure 3-10** depicts the DIO logic block diagram.
The DIO signal response time setting is configured through RXCREG and has the following modes of operation:

- **Default mode**: The DIO is permanently connected to logic high. It always stays high independent of the receiving parameters.
- **Slow mode**: The DIO signal goes high if the digital RSSI, DQI and Clock Recovery Lock (CR_LOCK) signals are present. It stays high until any of these signals are present and goes low when all three input signals are low.
- **Medium mode**: The DIO signal is active when the CR_LOCK and the DRSSI or the DQI signals are high. It goes low when either the CR_LOCK becomes inactive or the DRSSI or DQI signals go low.
- **Fast mode**: The DIO signal follows the level of the DQI signal.

The registers associated with DQI are:
- STSREG (see Register 2-1)
- RXCREG (see Register 2-7)
- BBFCREG (see Register 2-8)

### 3.12 Programmable Synchronous Byte

The internal synchronous pattern and the pattern length are user-programmable. The MRF49XA is configured to use a synchronous character to indicate the valid incoming data. The synchronous character selection is done through the FIFORSTREG. The character is divided into two bytes: SCL1 and SCL0. The SCL0 byte is user-configurable, whereas SCL1 is fixed to 2Dh and is non-programmable. The synchronous character can also be configured as a byte character or a word character. A byte character uses only SCL0, whereas the word character uses both SCL1 and SCL0. Since SCL0 is user-configurable, it is advantageous while operating under interferences and also while identifying the related transmitters.

The registers associated with the programmable synchronous byte are:
- FIFORSTREG (see Register 2-10)
- PMCREG (see Register 2-13)

### 3.13 Received Signal Strength Indicator

The Received Signal Strength Indicator (RSSI) estimates the received signal power within the bandwidth of ISM channels. The MRF49XA provides both analog RSSI and digital RSSI. A digital RSSI output is provided to monitor the input signal level. The signal goes high if the received signal strength exceeds a given preprogrammed level. The digital RSSI threshold is programmable through RXCREG, and is read and monitored only through STSREG. When an incoming signal is stronger than the preprogrammed threshold, the digital RSSI bit in the STSREG is set. The settling time of digital RSSI depends on the external filter capacitor.

The DRSSIT value is a 3-bit binary value ranging from 0 to 8. Table 3-2 shows the mapping between the DRSSIT value versus the received power level. The number of symbols to average can be changed by programming the DRSSIT bits (RXCREG<2:0>).

The digital RSSI is basically a sensitive comparator behind an analog RSSI block. The comparator threshold can be set using the three bits and the comparator output can be read out through the Status Read register. The curve in Figure 3-11 shows the analog RSSI output voltage versus signal strength.

The analog RSSI level is linear with input signal levels between -103 dBm and -73 dBm. The RSSIO pin in MRF49XA is used as an analog RSSI output and better results can be achieved by using this pin with a sensitive comparator.

These bits can be set to indicate the incoming signal strength above a preset limit. The result enables or disables the DQDO bit (STSREG<7>). The RSSI threshold depends on the LNA gain and the real RSSI threshold can be calculated by using the formula as given in Equation 3-2.

**EQUATION 3-2:**

\[
\text{RSSI}_{th} = \text{RSSI}_{setth} + G_{LNA}
\]

In Transmit mode, the ATRSSI bit (STSREG<8>) indicates that the antenna tuning circuit has detected a relatively strong RF signal.

In Receive mode, the ATRSSI bit indicates that the incoming RF signal is above the preprogrammed digital RSSI threshold.
3.13.1 RELATIONSHIP BETWEEN RSSI AND CLOCK RECOVERY

The DIO signal response time setting is configured through RXCREG and has the following modes of operation:

- Normal mode
- Slow mode
- Medium mode
- Fast mode

These operation modes are configurable through BBFCREG.

In Medium mode, the DIO signal is active when the CR_LOCK and the DRSSI or the DQI signals are high. The DIO goes low when either the CR_LOCK turns inactive, or the DRSSI or DQI signals go low. For more details on DQI, see Section 3.11, Data Quality Indicator.

3.13.2 RELATIONSHIP BETWEEN RSSI AND AFC

The Keep Offset mode of automatic configuration of AFC (i.e., AUTOMS1 = 1, AUTOMS0 = 1) is recommended to be used when a receiver operates with only one transmitter. After a complete measuring cycle, the measured value is kept independent from the state of the DIO signal. In this mode, the DRSSI limit should be carefully selected to minimize the range hysteresis.

The registers associated with RSSI are:
- STSREG (see Register 2-1)
- GENCREG (see Register 2-2)
- RXCREG (see Register 2-7)
- PMCREG (see Register 2-13)
3.14 Power Management

The Power Management Configuration register enables/disables the following functions:

- Receiver
- Transmitter
- Baseband Circuit
- Synthesizer
- Crystal Oscillator
- Low Battery Detect Circuit
- Wake-up Timer
- Clock Output

Figure 3-12 shows the functions that are enabled using PMCREG.

Receiver: The RXCEN bit, when set, enables the entire receiver chain. The receiver chain consists of a baseband circuit, synthesizer and crystal oscillator.

Transmitter: The TXCEN bit, when set, enables the entire transmit chain. The transmit chain consists of a power amplifier, synthesizer, oscillator and transmit register. When the transmit chain and Transmit register are enabled, any data in the Transmit register is shifted out and a transmission is started.

Baseband Circuit: The BBCEN bit, when set, enables the baseband circuit. The baseband circuit, synthesizer and oscillator work together to demodulate and recover the data transmitted to the synthesizer (SYNEN bit). If baseband circuits are enabled, then the oscillator (OSCEN bit) must be enabled in order to receive data. The BBCEN bit can be disabled to reduce current consumption.

Synthesizer: The SYNEN bit, when set, enables the synthesizer. The synthesizer is comprised of a PLL, oscillator and VCO for controlling the channel frequency. This bit must be enabled when either the transmitter or the receiver is enabled. The oscillator must also be enabled to provide the reference frequency for the PLL. On power-up, the synthesizer automatically performs the calibration. If there are significant changes in voltage or temperature, recalibration can be performed by disabling and re-enabling the synthesizer.

Crystal Oscillator: The OSCEN bit, when set, enables the oscillator circuit. The oscillator provides the reference signal to the synthesizer when setting the transmit or receive frequency of use.

Low Battery Detect Circuit: The LBDEN bit, when set, enables the battery voltage detect circuit. The battery detector can be programmed to 32 different threshold levels. See Register 2-16 (BCSREG) for programming details.

Wake-up Timer: The WUTEN bit, when set, enables the wake-up timer. See Register 2-14 (WTSREG) for details on programming the wake-up timer interval.

Clock Output: The CLKOEN bit, when set, enables the oscillator clock output. On device Reset or power-up, the clock output is enabled so that a processor can begin execution of any special setup sequences as required by the designer. See Register 2-16 (BCSREG) for programming details.

Note: If bit 0 is cleared, and with the clock output enabled, the oscillator continues to run even if the OSCEN bit is cleared. The device will not fully enter Sleep mode.

The RF front end is comprised of the LNA and the mixer. The synthesizer block has two main components: the VCO and the PLL. The baseband section consists of a baseband amplifier, low-pass filter, limiter and I/Q demodulator.

The synthesizer also has an internal start-up calibration procedure. If quick RX/TX switching is needed, leave this block on. Enabling the transmitter using the TXCEN bit (PMCREG<5>) will turn on the PA, and since the synthesizer is already up and running, the PA immediately produces the TX signal at the output.

To decrease the TX/RX turnaround time, keep the baseband section on. Switching to Receive mode means disabling the PA and enabling the RF front end. Since the baseband block is already on, the internal start-up calibration is skipped, and thus, the turnaround time is shorter. The BBCEN, SYNEN and OSCEN bits are provided to optimize the TX to RX or RX to TX turnaround time.

The crystal oscillator provides a reference signal to the RF synthesizer, baseband circuit and digital signal processor. If the receiver or the transmitter is frequently used, it is recommended to leave the oscillator running as the crystal might need a few milliseconds to start. The start timing mainly depends on the crystal parameters.

Note: Leaving blocks unnecessarily turned on increases the current consumption, and thus, decreases the battery life.
From PMCREG, the following points are applicable when using the bit functionalities:

- The chip enters Receive mode if both the TXCEN and RXCEN bits are set.
- **FSK/DATA/FSEL** input is equipped with an internal pull-up resistor. To achieve minimum current consumption, do not pull this input to logic low in Sleep mode.
- To enable the RF synthesizer, the crystal oscillator must be turned on.
- To turn on the baseband circuits, the RF synthesizer and the crystal oscillator must be enabled.
- Setting the RXCEN bit automatically turns on the crystal oscillator, synthesizer, baseband circuits and RF front end.
- Setting the TXCEN bit automatically turns on the crystal oscillator, synthesizer and RF power amplifier.

The clock tail and automatic crystal enable/disable features help in reducing the power consumption and are discussed in detail in Section 3.4, Crystal Oscillator and Clock Output.

The registers associated with power management are:

- STSREG (see Register 2-1)
- GENCREG (see Register 2-2)
- RXCREG (see Register 2-7)
- PMCREG (see Register 2-13)
FIGURE 3-12: LOGIC CONNECTIONS BETWEEN POWER CONTROL BITS

- **Enable Power Amplifier**
- **Start TX**
- **Clear TX Latch (if TX latch is used)**
- **Enable RF Synthesizer** (Crystal Synthesizer must be ON)
- **Enable RF Front End**
- **Enable Baseband Circuits** (RF Synthesizer must be ON)
- **Enable Crystal Oscillator**
- **Enable Crystal Oscillator**
- **Enable Power Amplifier**
- **Enable RF Synthesizer**
- **Start TX**
- **Clear TX Latch**
- **Enable Crystal Oscillator**
- **Enable Baseband Circuits**
- **Enable RF Front End**
- **Enable Digital Signal Processing**
- **Enable I/Q Demod.**
3.15 Low Duty Cycle Mode

In Low Duty Cycle mode, the receiver periodically wakes up for a short period and checks for the valid FSK transmission in progress. The FSK transmission is detected in the frequency range determined by CFSREG and the baseband filter bandwidth is determined by the RXCREG. The on time is automatically extended until the DQI indicates a good received signal condition.

The following facts need to be considered while calculating the duty cycle on-time:

- The crystal oscillator, the synthesizer and the PLL need time to start (see Table 5-7).
- Depending on the DQTI, the device needs to receive few valid data bits before the DQI signal indicates a good signal condition (see Register 2-8).

Selecting a short on-time can prevent the crystal oscillator from starting, or the DQI signal will not go high even when the received signal has a good quality. The MRF49XA is normally configured to work in FIFO mode. However, when the device periodically wakes up from Sleep mode, it switches to the Receive mode. If valid FSK data is received, the device sends an interrupt to the microcontroller and continues filling the RXFIFO. On completion of transmission, the FIFO is read out completely and all other interrupts are cleared. The device then returns to the Low-Power Consumption mode. Figure 3-13 depicts the Low-Power Duty Cycle mode sequence.

The low duty cycle is calculated by using the DCMV (DCSREG<7:1>) and WTMV (WTSREG<7:0>) bits, as shown in Equation 3-3. The time cycle is determined by the WTSREG.

\[
DC = \frac{(DCMV<7:1> \times 2 + 1)}{WTMV<7:0>} \times 100\%
\]

Note: In Duty Cycle mode, the RXCEN bit must be cleared and the WUTEN bit must be set in PMCREG.

The registers associated with Low Duty Cycle mode are:

- STSREG (see Register 2-1)
- GENCREG (see Register 2-2)
- RXCREG (see Register 2-7)
- BBFCREG (see Register 2-8)
- PMCREG (see Register 2-13)
- WTSREG (see Register 2-14)

![Figure 3-13: Low-Power Duty Cycle Mode Sequence](image-url)
3.16  Sleep, Wake-up and Battery Operations

The advanced interrupt handler circuit is configured in the transmitter to reduce the power consumption. As mentioned, the Sleep mode is the lowest power consumption mode in which the clock and all functional blocks of the device are disabled. In case of any interrupt, the device wakes up, switches to Active mode and an interrupt signal generated on the IRO pin indicates the change in state to the host microcontroller. The source of the interrupt can be determined by reading the status word of the device (see Register 2-1).

To reduce current consumption, the MRF49XA should be placed in the low-power consuming Sleep mode. In Sleep mode, the 10 MHz main oscillator is turned off, disabling the RF and baseband circuitry. Data is retained in the control and FIFO registers and the transceiver is accessible through the SPI port.

The MRF49XA will not enter Sleep mode if any of the interrupt remains active, irrespective of the state of the OSCEN bit in the PMCREG. This way, the microcontroller can always have a clock signal to process the interrupt. To prevent high-current consumption, which results in shorter battery life, it is highly recommended to process and clear interrupts before entering Sleep mode. The functions which are not necessary should be turned off to avoid unwanted interrupts.

To minimize the current consumption, the MRF49XA supports different power-saving modes, along with an integrated wake-up timer. Active mode can be reinitialized by the following ways:

- By applying the wake-up events' negative logical pulse on INT pin
- Wake-up timer time-out
- Low supply voltage detection
- On-chip FIFO filled up
- On receiving a request through the serial interface

To make the MRF49XA device enter into Sleep mode, certain control register values must be initialized. The sequence to program the control registers for entering into Sleep and Wake-up modes is as follows:

For Sleep mode:
1. Check the IRO bit status
2. Read STSREG
3. Configure GENCREG
4. Configure PMCREG for oscillator and clock buffering

For Wake-up mode:
1. Enter in TX/RX mode or
2. Enable crystal or
3. Set the INT pin

The device has the ability to wake itself up from Sleep mode through a wake-up timer. The WTSREG sets the wake-up interval for the MRF49XA. After setting the wake-up interval, the WUTEN bit (PMCREG<1>) should be cleared and set at the end of every wake-up cycle.

The Wake-up Duration Time (WUTIME) is calculated as shown in Equation 3-4.

**EQUATION 3-4:**

\[
WUTIME = 1.03 \times WTMOV<7:0> \times 2^{WTEV<4:0>} + 0.5 \text{ ms}
\]

where:
- \( WTMOV<7:0> \) = Decimal Value between 0 to 255
- \( WTEV<4:0> \) = Decimal Value between 0 to 29

Note: WUTIME is measured in ms.

The Battery Threshold Detect feature is useful in monitoring the discharge-sensitive batteries, such as Lithium cells. The LBDEN bit (PMCREG<2>) is used to enable or disable the low battery detect feature.

The BCSREG configures the following:
- Output clock frequency
- Low battery detect threshold

The low battery threshold value is programmable from 2.2V to 3.8V and is calculated by using Equation 3-5.

**EQUATION 3-5:**

\[
\text{Threshold Voltage Value} = 2.25 + 0.1 \times \text{LBDVB}<3:0>
\]

where:
- \( \text{LBDVB}<3:0> \) is the Decimal Value from 0-15

When the battery level falls 50 mV below this value, the LBTD bit (STSREG<10>) is set, indicating that the battery level is below the programmed threshold.

The registers associated with power-saving modes are:
- STSREG (see Register 2-1)
- GENCREG (see Register 2-2)
- TXCREG (see Register 2-4)
- RXCREG (see Register 2-7)
- PMCREG (see Register 2-13)
- WTSREG (see Register 2-14)
- BCSREG (see Register 2-16)
3.17 TX Register Buffered Data Transmission

In Data Transmission mode (enabled by the TXDEN bit (GENCREG<7>)), the TX data is clocked into one of the two 8-bit data registers. The transmitter starts to send the data from the first register (with the given bit rate) when the TXCEN bit (PMCREG<5>) is set. The initial value of the data registers (0xAA) can be used to generate preamble. During this mode, the SDO pin is monitored to check whether the register is ready (SDO is high) to receive the next byte from the microcontroller. The block diagrams of the Transmit register, before and during transmit, are shown in Figure 3-14 and Figure 3-15, respectively.

The transmitter FSK modulation parameters are used for calculating the resulting output frequency, as shown in Equation 3-6.

\[
\text{fFSKOUT} = f_0 + (-1)^{\text{SIGN}} \times (\text{MB} + 1) \times (15 \text{ kHz})
\]

where:
- \(f_0\) is the Channel Center Frequency (see Register 2-6 for \(f_0\) calculation)
- MB is the 4-bit Binary Number (MODBW<3:0>)
- SIGN = MODPLY XOR FSK

FIGURE 3-14: TX REGISTER BLOCK DIAGRAM (BEFORE TRANSMIT)
FIGURE 3-15: TX REGISTER BLOCK DIAGRAM (DURING TRANSMIT)

TXCEN = 1 (During TX)

8-Bit Shift Register

SDI

CLK

SDO

TX_DATA

SEL

10 Y

11 MUX

8-Bit Shift Register

SDI

CLK

SDO

SEL

10 Y

11 MUX

Note: The data registers' content is initialized by clearing the TXCEN bit.
The device transmit sequence should be performed as follows:

1. Enable the TX register by setting TXDEN = 1.
2. The TX register is automatically filled with 0xAAAA, which can be used to generate preamble.
3. Enable the transmitter by setting TXCEN = 1.
4. The synthesizer and the PLL turns on, calibrates itself and the PA is automatically enabled.
5. The TX data transmission starts.
6. On completion of byte transmission, the IRO pin goes high and the SDO pin goes low simultaneously. The IRO pulse shows that the first 8 bits (the first byte by default, 0xAA) have been transmitted. There are still 8 bits in the transmit register.
7. The microcontroller recognizes the interrupt and writes a data byte to the TXBREG.
8. Repeat steps 6 and 7 until the last data byte is reached.
9. Using the same method, transmit a dummy byte. The value of this dummy byte can be anything.
10. The next high-to-low transition on the IRO line (or low-to-high on the SDO pin) shows that the transmission of the data bytes has ended. The dummy byte is still in the TX latch.
11. Turn off the transmitter by setting the bit, TXCEN = 0. This event probably happens while the dummy byte is being transmitted. Since the dummy byte contains no useful information, this corruption will not cause any problem.
12. Clearing the TXDEN bit clears the register underrun interrupt. The IRO pin goes high and the SDO pin goes low.

The transmit sequence is illustrated in Figure 3-16. For details on transmit pin function configuration, see Table 3-3. The TXDEN bit is in the GENCREG register and enables the Transmit Data register.

The transmit sequence can be performed without sending a dummy byte (step 1), but after loading the last data byte to the transmit register, the PA turn off should be delayed for at least 16 bits time. The microcontroller clock source (if the clock is not supplied by the transceiver) should be stable enough over temperature and voltage ranges to ensure this minimum delay under all operating circumstances.

When the dummy byte is used, the whole process is driven by interrupts. Changing the TX data rate has no effect on the algorithm and no accurate delay measurement is needed. Figure 3-17 shows the multi-byte transmit write sequence.

The registers associated with transmission are:
- STSREG (see Register 2-1)
- GENCREG (see Register 2-2)
- TXCREG (see Register 2-4)
- TXBREG (see Register 2-5)
- PMCREG (see Register 2-13)

### TABLE 3-3: TRANSMIT PIN FUNCTION VS. OPERATION MODE

<table>
<thead>
<tr>
<th>Mode</th>
<th>Bit Setting</th>
<th>Function</th>
<th>Pin 6</th>
<th>Pin 7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmit</td>
<td>TXDEN = 0</td>
<td>Internal TX Data register disabled</td>
<td>TX data input</td>
<td>Not used</td>
</tr>
<tr>
<td></td>
<td>TXDEN = 1</td>
<td>Internal TX Data register enabled</td>
<td>FSEL input (TX Data register can be accessed)</td>
<td></td>
</tr>
</tbody>
</table>
FIGURE 3-16: TX REGISTER USAGE

Enabling the transmitter preloads the TX latch with 0xAAAA. Do not switch the TXCEN off here, because the TX Byte 1 is not transmitted out, it is only stored in the internal register.

SPI Commands (CS, SCK, SDI)

TXDEN = 1

TXCEN = 1

TX Byte 1

Dummy TX Byte

TXCEN = 0

TXDEN = 0

Synt.

PA

Ttx_xtal_on(1)

TXCEN Enable Synthesizer/PA

0xAA

Fraction of the dummy byte

0xAA TX Byte1

Note 1: Ttx_xtal_on is the start-up time of PLL + PA with a running crystal oscillator.

2: SDO is a tri-state of CS.

FIGURE 3-17: MULTIPLE BYTE WRITE WITH TRANSMIT REGISTER

CS

SCK

SDI

Transmit Register Write

TX BYTE 1

TX BYTE 2

TX BYTE n

SDO

(Register interrupt in TX mode*)

* The device is in Transmit (TX) mode when the RXCEN bit is cleared using the PMCREG.
3.18 RX FIFO Buffered Data Read

In the Receive Operating mode, the incoming data is clocked into a 16-bit FIFO buffer. The receive pin function configuration required for the FIFO operation is given in Table 3-4. The FIFOEN bit is in the GENCREG register and enables the receive FIFO. The receiver starts to fill the FIFO when the FINTDIO bit and the synchronous pattern recognition circuit indicates the potential real incoming data. This prevents the FIFO from being filled with noise and avoids the overloading on the external microcontroller.

The internal synchronous pattern and the pattern length are user-programmable. If the Chip Select (CS) pin is low, the data bits on the SDI pin are shifted into the device on the rising edge of the clock on the SCK pin. The serial interface is initialized every time if the CS signal is high. Figure 3-18 shows a simple receiver FIFO read over SPI lines.

In general, MRF49XA registers are read only. The RXFIFO and the chip status can be read. During write only appropriate byte is written to the desired register. Hence it is not desired to read/write all registers and there is no way reading back any of the other registers. To test the SPI interface lines, the best is to set the LBD (Low Battery Detector) threshold below the actual VDD and the device must generate an interrupt.

FIGURE 3-18: RECEIVER FIFO READ

![Diagram of RX FIFO Read]

Note: The transceiver is in Receive (RX) mode when the RXCEN bit is set using the PMCREG.
3.18.1 INTERRUPT MODE
The user can define the FIFO interrupt level (the number of received bits) which generates the FINT when the level is exceeded. In this case, the Status bits report the changed FIFO status.

3.18.2 POLLING MODE
When the FSEL signal is low, the FIFO output is connected directly to the SDO pin and its contents are clocked out by the SCK pin. Set the FIFO interrupt level to 1. In this case, as long as FINT indicates received bits in the FIFO, the microcontroller continues to take the bits away. When FINT goes low, no more bits need to be taken.

An SPI read command (Receiver FIFO Read Command) is also available to read out the contents of the FIFO. See Figure 3-19 for a simple receiver FIFO read, in Polling mode, on SPI lines.

### TABLE 3-4: RECEIVE PIN FUNCTION VS. OPERATION MODE

<table>
<thead>
<tr>
<th>Mode</th>
<th>Bit Setting</th>
<th>Function</th>
<th>Pin 6</th>
<th>Pin 7</th>
</tr>
</thead>
<tbody>
<tr>
<td>Receive</td>
<td>FIFOEN = 0</td>
<td>Receiver FIFO Disabled</td>
<td>RX Data Output</td>
<td>RX Data Clock Output</td>
</tr>
<tr>
<td>FIFOEN = 1</td>
<td>Receiver FIFO Enabled</td>
<td>FSEL Input (RX data FIFO can be accessed)</td>
<td>FINT Output</td>
<td></td>
</tr>
</tbody>
</table>

### FIGURE 3-19: FIFO READ EXAMPLE WITH FINT POLLING

![FIFO Read Example with FINT Polling](image)

**Note:** During FIFO access, f_SCK cannot be higher than f_{ref}/4, where f_{ref} is the crystal oscillator frequency. If the duty cycle of the clock signal is not 50%, the shorter period of the clock pulse should be at least 2/f_{ref}.

The registers associated with reception are:
- STSREG (see Register 2-1)
- GENCREG (see Register 2-2)
- RXCREG (see Register 2-7)
- FIFORSTREG (see Register 2-10)
- PMCREG (see Register 2-13)
3.19 RX-TX Frequency Alignment Method

The RX-TX frequency offset occurs due to the differences in the actual reference frequency. To minimize this error, the same crystal type and the same PCB layout should be used for the crystal placement on the RX and TX PCBs. Also, see Section 3.6, Crystal Selection Guidelines.

To verify the possible RX-TX offset, it is recommended to measure the CLK output of both transceivers with a high level of accuracy. Do not measure the output at the RFXTL pin as the measurement process itself might change the reference frequency. As the carrier frequencies are derived from the reference frequency, having identical reference frequencies, and nominal frequency settings at the TX and RX side, there should be no offset if the CLK signals have identical frequencies.

The crystal oscillator load capacitor bank value is to fine-tune the oscillator and minimize the offset. So the process is to measure the clock output and parallel change the value to minimize the offset.

The actual RX-TX offset can be monitored by using the AFC status data included in the STSREG of the receiver. By reading out the STSREG, the actual measured offset frequency can be reported. In order to get accurate values, the AFC has to be disabled during the read by clearing the FOFEN bit in AFCCREG.

The registers associated with RX-TX alignment procedures are:

- STSREG (see Register 2-1)
- AFCCREG (see Register 2-3)
- RXCREG (see Register 2-7)
- PMCREG (see Register 2-13)
4.0 APPLICATION DETAILS

The application circuit of MRF49XA with a balun circuit is shown in Figure 4-1.

FIGURE 4-1: APPLICATION CIRCUIT

4.1 Antenna/Balun

A balun circuit for a 50\(\Omega\) antenna is shown in Figure 4-2. If low tolerance components (i.e., ±5\%) are used with an appropriate ground, the impedance remains close to the 50\(\Omega\) measurement.

FIGURE 4-2: BALUN CIRCUIT
4.2 Antenna Design Considerations

The MRF49XA is designed to drive a differential output, such as a dipole antenna or a loop antenna. The loop antenna is ideally suited for applications where compact size is required. The dipole is typically not a good option for compact designs due to its inherent size at resonance, and its space requirements around the ground plane, to be an efficient antenna. A monopole antenna can be used, along with a balun, or by using the matching circuit.

4.3 RF Transmitter Matching

The RF pins are of high impedance and differential value. The optimum differential load for the RF port at a given frequency band is shown in Table 4-1. These load values in the table are expected by the RF port pins to have as an antenna load for maximum power transfer. Antennas that are suited for such values would be a Loop, Dipole and Folded Dipole. For all antenna applications, either a bias, choke inductor or coils must be included during transmission since the RF outputs are of open-collector type.

TABLE 4-1: FREQUENCY BAND – ANTENNA ADMITTANCE/IMPEDANCE

<table>
<thead>
<tr>
<th>MRF49XA</th>
<th>Admittance (ms)</th>
<th>Impedance (Ω)</th>
<th>Inductance (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>433 MHz</td>
<td>2–j5.9</td>
<td>52+j152</td>
<td>62</td>
</tr>
<tr>
<td>868 MHz</td>
<td>1.2–j11.9</td>
<td>7.8+j83</td>
<td>15.4</td>
</tr>
<tr>
<td>915 MHz</td>
<td>1.49–j12.8</td>
<td>9+j77</td>
<td>13.6</td>
</tr>
</tbody>
</table>

4.4 General PCB Layout Design

The guidelines in this section help the users in high-frequency PCB layout design. The printed circuit board is usually comprised of two or four basic FR4 layers. The two-layer printed circuit board has mixed signal/power/RF and common ground routed in both the layers.

The four-layer printed circuit board is comprised of the following layers:
- Signal layout
- RF ground
- Power line routing
- Common ground

The four-layer PCB is shown in Figure 4-4.

FIGURE 4-3: TWO BASIC COPPER FR4 LAYERS

FIGURE 4-4: FOUR BASIC COPPER FR4 LAYERS
The following guidelines explain the requirements of the above mentioned layers.

- It is important to keep the original PCB thickness, since any change will affect antenna performance (see total thickness of dielectric) or microstrip lines’ characteristic impedance.
- For good transmit and receive performance, the trace lengths at RF pins must be kept as short as possible. Using small, surface mount components (in 0402/0603 package) yields good performance and keeps the RF circuit small. RF connections should be short and direct.
- Except for the antenna layout, avoid sharp corners since they can act as an antenna. Round corners will eliminate possible future EMI problems.
- Digital lines are prone to be very noisy when handling periodic waveforms and fast clockswitching rates. Avoid RF signal layout close to any of the digital lines.
- A VIA filled ground patch underneath the IC transceiver is mandatory.
- Power supply must be distributed to each pin in a star topology and low-ESR capacitors must be placed at each pin for proper decoupling noise.
- Thorough decoupling on each power pin is beneficial for reducing in-band transceiver noise, particularly when this noise degrades performance. Usually, low value caps (27 pF – 47 pF) combined with large value caps (100 nF) will cover a large spectrum of frequency.
- Passive component (inductors) should be in the high-frequency category and the Self Resonant Frequency (SRF) should be at least two times higher than the operating frequency.

- The additional trace length affects the crystal oscillator by adding parasitic capacitance to the overall load of the crystal. To minimize this, place the crystal as close as possible to the RF device.
- Setting short and direct connections between the components on board minimizes the effects of “frequency pulling” that might be introduced by stray capacitance. It even allows the internal load capacitance of the chip to be more effective in properly loading the crystal oscillator circuit.
- Long run tracks of clock signal may radiate and cause interference. This can degrade receiver performance and add harmonics or unwanted modulation to the transmitter.
- Keep clock connections as short as possible and surround the clock trace with an adjacent ground plane pour. Pouring helps in reducing any radiation or crosstalk due to long run traces of the clock signal.
- Low value decoupling capacitors, typically 0.01 μF – 0.1 μF, should be placed for VDD of the chip and for bias points of the RF circuit.
- High value decoupling capacitors, typically 2.2 μF – 10 μF, should be placed at the point where power is applied to the PCB.
- Power supply bypassing is necessary. Poor bypassing contributes to conducted interference which can cause noise and spurious signals to couple into the RF sections, significantly reducing performance.
4.5 MRF49XA Schematic and Bill of Materials

4.5.1 SCHEMATIC

FIGURE 4-5: MRF49XA SCHEMATIC

<table>
<thead>
<tr>
<th>Freq.</th>
<th>C1</th>
<th>L1</th>
<th>L2</th>
<th>L3</th>
<th>C5</th>
<th>C6</th>
<th>C7</th>
</tr>
</thead>
<tbody>
<tr>
<td>433 MHz</td>
<td>220 pF</td>
<td>300 nH</td>
<td>33 nH</td>
<td>47 nH</td>
<td>2.7 pF</td>
<td>68 pF</td>
<td>5.1 pF</td>
</tr>
<tr>
<td>868 MHz</td>
<td>47 pF</td>
<td>100 nH</td>
<td>8.2 nH</td>
<td>22 nH</td>
<td>1.2 pF</td>
<td>27 pF</td>
<td>2.7 pF</td>
</tr>
<tr>
<td>915 MHz</td>
<td>33 pF</td>
<td>100 nH</td>
<td>8.2 nH</td>
<td>22 nH</td>
<td>1.2 pF</td>
<td>27 pF</td>
<td>2.7 pF</td>
</tr>
</tbody>
</table>
### 4.5.2 BILL OF MATERIALS

#### TABLE 4-2: MRF49XA: 433 MHz BILL OF MATERIALS

<table>
<thead>
<tr>
<th>Designator</th>
<th>Value</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer PN</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>200 pF</td>
<td>Capacitor, Ceramic, 50V, C0G, SMT 0603</td>
<td>Murata</td>
<td>GRM1885C1H201JA01D</td>
</tr>
<tr>
<td>C5</td>
<td>2.7 pF</td>
<td>Capacitor, Ceramic, 50V, C0G, SMT 0603</td>
<td>Murata</td>
<td>GRM1885C1H2R7CZ01D</td>
</tr>
<tr>
<td>C6</td>
<td>68 pF</td>
<td>Capacitor, Ceramic, 50V, C0G, SMT 0603</td>
<td>Murata</td>
<td>GRM1885C1H680JA01D</td>
</tr>
<tr>
<td>C7</td>
<td>5.1 pF</td>
<td>Capacitor, Ceramic, 50V, C0G, SMT 0603</td>
<td>Murata</td>
<td>GRM1885C1H5R1DZ01D</td>
</tr>
<tr>
<td>L1</td>
<td>390 nH</td>
<td>Inductor, Ceramic, 5%, SMT 0603</td>
<td>Murata</td>
<td>LQW18ANR39J00D</td>
</tr>
<tr>
<td>L2</td>
<td>33 nH</td>
<td>Inductor, Multilayer, 5%, SMT 0603</td>
<td>TDK Corporation</td>
<td>MLG1608B33NJ</td>
</tr>
<tr>
<td>L3</td>
<td>47 nH</td>
<td>Inductor, Multilayer, 5%, SMT 0603</td>
<td>TDK Corporation</td>
<td>MLG1608B47NJ</td>
</tr>
<tr>
<td>C4</td>
<td>1000 pF</td>
<td>Capacitor, Ceramic, 50V, 10%, SMT 0603, X7R</td>
<td>Murata</td>
<td>GRM188R71H102KA01D</td>
</tr>
<tr>
<td>C2</td>
<td>10000 pF</td>
<td>Capacitor, Ceramic, 50V, 10%, SMT 0603, X7R</td>
<td>Murata</td>
<td>GRM188R71H103KA01D</td>
</tr>
<tr>
<td>C3</td>
<td>2.2 μF, 10V</td>
<td>Capacitor, Tantalum, 10%, SMT 3216-18 (A)</td>
<td>Kemet</td>
<td>T491A225K010AT</td>
</tr>
<tr>
<td>U1</td>
<td>—</td>
<td>MRF49XA Transceiver</td>
<td>Microchip</td>
<td>MRF49XA-I/ST</td>
</tr>
<tr>
<td>X1</td>
<td>10 MHz</td>
<td>Crystal, ±10 ppm, 10 pF, SMT 5 x 3.2 mm</td>
<td>Abracon</td>
<td>ABM3B-10.000MHZ-12-R80-B-1-U-T</td>
</tr>
<tr>
<td>Designator</td>
<td>Value</td>
<td>Description</td>
<td>Manufacturer</td>
<td>Manufacturer PN</td>
</tr>
<tr>
<td>------------</td>
<td>-------</td>
<td>-------------</td>
<td>--------------</td>
<td>----------------</td>
</tr>
<tr>
<td>C1</td>
<td>33 pF</td>
<td>Capacitor, Ceramic, 50V, C0G, SMT 0603</td>
<td>Murata</td>
<td>GRM1885C1H330JA01D</td>
</tr>
<tr>
<td>C5</td>
<td>1.2 pF</td>
<td>Capacitor, Ceramic, 50V, C0G, SMT 0603</td>
<td>Murata</td>
<td>GRM1885C1H1R2CZ01D</td>
</tr>
<tr>
<td>C6</td>
<td>27 pF</td>
<td>Capacitor, Ceramic, 50V, C0G, SMT 0603</td>
<td>Murata</td>
<td>GRM1885C1H270JA01D</td>
</tr>
<tr>
<td>C7</td>
<td>2.7 pF</td>
<td>Capacitor, Ceramic, 50V, C0G, SMT 0603</td>
<td>Murata</td>
<td>GRM1885C1H2R7CZ01D</td>
</tr>
<tr>
<td>L1</td>
<td>100 nH</td>
<td>Inductor, Multilayer, 5%, SMT 0603</td>
<td>TDK Corporation</td>
<td>MLG1608BR10J</td>
</tr>
<tr>
<td>L2</td>
<td>8.2 nH</td>
<td>Inductor, Multilayer, 5%, SMT 0603</td>
<td>TDK Corporation</td>
<td>MLG1608B8N2D</td>
</tr>
<tr>
<td>L3</td>
<td>22 nH</td>
<td>Inductor, Multilayer, 5%, SMT 0603</td>
<td>TDK Corporation</td>
<td>MLG1608B22NJ</td>
</tr>
<tr>
<td>C4</td>
<td>1000 pF</td>
<td>Capacitor, Ceramic, 50V, 10%, SMT 0603, X7R</td>
<td>Murata</td>
<td>GRM188R71H102KA01D</td>
</tr>
<tr>
<td>C2</td>
<td>10000 pF</td>
<td>Capacitor, Ceramic, 50V, 10%, SMT 0603, X7R</td>
<td>Murata</td>
<td>GRM188R71H103KA01D</td>
</tr>
<tr>
<td>C3</td>
<td>2.2 μF, 10V</td>
<td>Capacitor, Tantalum, 10%, SMT 3216-18 (A)</td>
<td>Kemet</td>
<td>T491A225K010AT</td>
</tr>
<tr>
<td>U1</td>
<td>—</td>
<td>MRF49XA Transceiver</td>
<td>Microchip</td>
<td>MRF49XA-I/ST</td>
</tr>
<tr>
<td>X1</td>
<td>10 MHz</td>
<td>Crystal, ±10 ppm, 10 pF, SMT 5 x 3.2 mm</td>
<td>Abracon</td>
<td>ABM3B-10.000MHZ-12-R80-B-1-U-T</td>
</tr>
</tbody>
</table>
5.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Temperature under bias ...................................................................................................................................... -40°C to +85°C
Storage temperature ........................................................................................................................................... -55°C to +125°C
Lead temperature (soldering, max 10s) .................................................................................................................. +260°C
Voltage on VDD with respect to VSS .................................................................................................................. -0.3V to 6V
Voltage on any combined digital and analog pin with respect to VSS (except RFP, RFN and VDD) ........................................... -0.3V to (VDD + 0.3V)
Voltage on open-collector outputs (RFP, RFN)†............................................................................................. -0.5V to (VDD + 1.5V)
Input current into pin (except VDD and VSS) ..................................................................................................... -25 mA to 25 mA
Electrostatic discharge with human body model ................................................................................................ 1000V

Note: At maximum, voltage on RFP and RFN cannot be higher than 7V.

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
### TABLE 5-1: RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temperature</td>
<td>-40</td>
<td>—</td>
<td>+85</td>
<td>°C</td>
</tr>
<tr>
<td>Supply Voltage for RF, Analog and Digital Circuits</td>
<td>2.2</td>
<td>—</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>Supply Voltage for Digital I/O</td>
<td>2.2</td>
<td>3.3</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td>DC Voltage on Open-Collector Outputs (RFP, RFN)</td>
<td>VDD–1.5</td>
<td>—</td>
<td>VDD+1.5</td>
<td>V</td>
</tr>
<tr>
<td>AC Peak Voltage on Open-Collector Outputs (RFP, RFN)</td>
<td>VDD–1.5</td>
<td>—</td>
<td>VDD+1.5</td>
<td>V</td>
</tr>
</tbody>
</table>

**Note 1:** At minimum, VDD – 1.5V cannot be lower than 1.2V.

**Note 2:** At maximum, VDD + 1.5V cannot be higher than 5.5V.

### TABLE 5-2: CURRENT CONSUMPTION\(^{(1)}\)

<table>
<thead>
<tr>
<th>Chip mode Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sleep</td>
<td>—</td>
<td>0.3</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>Idle</td>
<td>—</td>
<td>0.6</td>
<td>1.2</td>
<td>mA</td>
</tr>
<tr>
<td>TX Power output – 0 dBm, 50Ω load, 433 MHz</td>
<td>—</td>
<td>15</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td>868 MHz</td>
<td>—</td>
<td>16</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td>915 MHz</td>
<td>—</td>
<td>17</td>
<td>—</td>
<td>mA</td>
</tr>
<tr>
<td>TX At maximum output power, 433 MHz</td>
<td>—</td>
<td>22</td>
<td>26</td>
<td>mA</td>
</tr>
<tr>
<td>868 MHz</td>
<td>—</td>
<td>23</td>
<td>27</td>
<td>mA</td>
</tr>
<tr>
<td>915 MHz</td>
<td>—</td>
<td>24</td>
<td>28</td>
<td>mA</td>
</tr>
<tr>
<td>RX 433 MHz</td>
<td>—</td>
<td>11</td>
<td>13</td>
<td>mA</td>
</tr>
<tr>
<td>868 MHz</td>
<td>—</td>
<td>12</td>
<td>14</td>
<td>mA</td>
</tr>
<tr>
<td>915 MHz</td>
<td>—</td>
<td>13</td>
<td>15</td>
<td>mA</td>
</tr>
<tr>
<td>Low Battery Voltage Detector Current Consumption</td>
<td>—</td>
<td>—</td>
<td>0.5</td>
<td>1.7</td>
</tr>
<tr>
<td>Wake-up Timer Current Consumption</td>
<td>—</td>
<td>—</td>
<td>1.5</td>
<td>3.5</td>
</tr>
</tbody>
</table>

**Note 1:** Typical Values: TA = 25°C, VDD = 3.3V.

### TABLE 5-3: I/O PIN INPUT SPECIFICATIONS\(^{(1)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>IIL</td>
<td>Input Low Leakage Current (^{(2)})</td>
<td>VIL = 0V</td>
<td>-1</td>
<td>—</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>IIH</td>
<td>Input High Leakage Current</td>
<td>VIH = VDD, VDD = 3.8V</td>
<td>-1</td>
<td>—</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td>VOL</td>
<td>Digital Low Output Voltage</td>
<td>IOL = 2 mA</td>
<td>—</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>Digital Low Output</td>
<td>IOH = -2 mA</td>
<td>VDD–0.4</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>VLBTB</td>
<td>Low Battery Threshold Detect</td>
<td>Programmable in 0.1V steps</td>
<td>2.25</td>
<td>—</td>
<td>3.75</td>
<td>V</td>
</tr>
</tbody>
</table>

**Note 1:** Typical Values: TA = 25°C, VDD = 3.3V.

**Note 2:** Negative current is defined as the current sourced by the pin.
### TABLE 5-4: RECEIVER AC CHARACTERISTICS\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Receiver Sensitivity</td>
<td>433 MHz band(^{(2)})</td>
<td>—</td>
<td>-112</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>868 MHz band(^{(2)})</td>
<td>—</td>
<td>-110</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>915 MHz band(^{(2)})</td>
<td>—</td>
<td>-109</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>Maximum RF Input Power</td>
<td>LNA: High Gain</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>RF Input Capacitance</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>pF</td>
</tr>
<tr>
<td>Receiver Spurious Emission</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>-60</td>
<td>dBm</td>
</tr>
<tr>
<td>Receiver BW</td>
<td>mode 0</td>
<td>—</td>
<td>67</td>
<td>—</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>Mode 1</td>
<td>—</td>
<td>134</td>
<td>—</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>Mode 2</td>
<td>—</td>
<td>200</td>
<td>—</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>Mode 3</td>
<td>—</td>
<td>270</td>
<td>—</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>Mode 4</td>
<td>—</td>
<td>340</td>
<td>—</td>
<td>kHz</td>
</tr>
<tr>
<td></td>
<td>Mode 5</td>
<td>—</td>
<td>400</td>
<td>—</td>
<td>kHz</td>
</tr>
<tr>
<td>RSSI Range</td>
<td>—</td>
<td>—</td>
<td>46</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>RSSI Error</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>±6</td>
<td>dB</td>
</tr>
<tr>
<td>RSSI Power Supply Dependency</td>
<td>When input signal level is lower than</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>mV/V</td>
</tr>
<tr>
<td></td>
<td>-54 dBm and greater than -100 dBm</td>
<td>—</td>
<td>+35</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>Filter Capacitor for Analog RSSI</td>
<td>—</td>
<td>1</td>
<td>—</td>
<td>—</td>
<td>nF</td>
</tr>
<tr>
<td>RSSI Programmable Level Steps</td>
<td>—</td>
<td>—</td>
<td>6</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Digital RSSI Response Time</td>
<td>Until the RSSI signal goes high after</td>
<td>—</td>
<td>500</td>
<td>—</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>the input signal exceeds the</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>preprogrammed limit, CARRSI = 4.7 nF</td>
<td>—</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input IP3</td>
<td>In band interferers in high bands (868</td>
<td>—</td>
<td>-21</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>MHz, 915 MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IIP3 (LNA – 6 dB gain)</td>
<td>In band interferers in low band (433</td>
<td>—</td>
<td>-15</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>MHz)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IIP3 (LNA – 6 dB gain)</td>
<td>Out of band interferers, (</td>
<td>f - f_0</td>
<td>&gt; 4 MHz)</td>
<td>—</td>
<td>-12</td>
</tr>
<tr>
<td>FSK Bit Rate</td>
<td>With internal digital filters supported</td>
<td>0.6</td>
<td>—</td>
<td>115.2</td>
<td>kbps</td>
</tr>
<tr>
<td></td>
<td>by design</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSK Bit Rate</td>
<td>With internal analog filters supported</td>
<td>—</td>
<td>—</td>
<td>256</td>
<td>kbps</td>
</tr>
<tr>
<td></td>
<td>by design</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>AFC Locking Range</td>
<td>(\Delta f_{fsk}): FSK deviation in</td>
<td>—</td>
<td>0.8 –</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>the received signal</td>
<td></td>
<td>(\Delta f_{fsk})</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Typical Values: \(TA = 25^\circ C, V_{DD} = 3.3V\).

**Note 2:** BER = 10E – 3, BW = 67 kHz, \(\Delta f = 30 kHz\), Baud Rate = 1.2 kbps, digital filter with AFC disabled.
### TABLE 5-5: TRANSMITTER AC CHARACTERISTICS(1)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Carrier Frequency</td>
<td>433 MHz band, 2.5 kHz resolution</td>
<td>430.24</td>
<td>—</td>
<td>439.75</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>868 MHz band, 5.0 kHz resolution</td>
<td>860.48</td>
<td>—</td>
<td>879.51</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td>915 MHz band, 7.5 kHz resolution</td>
<td>900.72</td>
<td>—</td>
<td>929.27</td>
<td>MHz</td>
</tr>
<tr>
<td>Maximum RF Output Power</td>
<td>433 MHz @ 50Ω load</td>
<td>—</td>
<td>7</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>868 MHz @ 50Ω load</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td>915 MHz @ 50Ω load</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>dBm</td>
</tr>
<tr>
<td>RF Output Power Control Range</td>
<td>In steps of 8 P&lt;sub&gt;max&lt;/sub&gt; – 17.5</td>
<td>—</td>
<td>—</td>
<td>P&lt;sub&gt;max&lt;/sub&gt;</td>
<td>dBm</td>
</tr>
<tr>
<td>TX Gain Control Resolution</td>
<td>Programmed in 8 steps</td>
<td>—</td>
<td>2.5</td>
<td>—</td>
<td>dB</td>
</tr>
<tr>
<td>Harmonic Suppression</td>
<td>At maximum power, 50Ω load</td>
<td>—</td>
<td>—</td>
<td>-35</td>
<td>dB</td>
</tr>
<tr>
<td>Open-Collector Output DC Current</td>
<td>Programmable</td>
<td>0.5</td>
<td>—</td>
<td>6</td>
<td>mA</td>
</tr>
<tr>
<td>Spurious Emission f&lt;sub&gt;f&lt;sub&gt;sp&lt;/sub&gt;&lt;/sub&gt;</td>
<td>At maximum power, 50Ω load</td>
<td>—</td>
<td>—</td>
<td>-55</td>
<td>dBc</td>
</tr>
<tr>
<td>Output Capacitance (Set by the Automatic Antenna Tuning Circuit)</td>
<td>433 MHz band</td>
<td>2</td>
<td>2.6</td>
<td>3.2</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td>868 MHz band</td>
<td>2.1</td>
<td>2.7</td>
<td>3.3</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td>915 MHz band</td>
<td>2.1</td>
<td>2.7</td>
<td>3.3</td>
<td>pF</td>
</tr>
<tr>
<td>Quality Factor of the Output Capacitance</td>
<td>433 MHz band</td>
<td>13</td>
<td>15</td>
<td>17</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>868 MHz band</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>915 MHz band</td>
<td>8</td>
<td>10</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>Output Phase Noise</td>
<td>100 kHz from carrier</td>
<td>—</td>
<td>-80</td>
<td>—</td>
<td>dBc/Hz</td>
</tr>
<tr>
<td></td>
<td>1 MHz from carrier</td>
<td>—</td>
<td>-103</td>
<td>—</td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>FSK Bit Rate</td>
<td>Internal TX Data register</td>
<td>—</td>
<td>—</td>
<td>172</td>
<td>kbps</td>
</tr>
<tr>
<td>FSK Bit Rate</td>
<td>TX data connected to the FSK input</td>
<td>—</td>
<td>—</td>
<td>256</td>
<td>kbps</td>
</tr>
<tr>
<td>FSK Frequency Deviation</td>
<td>Programmable in 15 kHz steps</td>
<td>15</td>
<td>—</td>
<td>240</td>
<td>kHz</td>
</tr>
</tbody>
</table>

**Note 1:** Typical Values: TA = 25°C, V<sub>DD</sub> = 3.3V.

### TABLE 5-6: PLL PARAMETERS AC CHARACTERISTICS(1)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Condition/Note</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL Reference Frequency</td>
<td>Crystal related timing and frequency parameters change according to the PLL reference frequency</td>
<td>9</td>
<td>10</td>
<td>11</td>
<td>MHz</td>
</tr>
<tr>
<td>PLL Lock Time</td>
<td>Frequency error &lt;1 kHz after 10 MHz step</td>
<td>—</td>
<td>30</td>
<td>—</td>
<td>μs</td>
</tr>
<tr>
<td>PLL Start-up Time</td>
<td>With a running crystal oscillator and based on the design</td>
<td>—</td>
<td>200</td>
<td>300</td>
<td>μs</td>
</tr>
</tbody>
</table>

**Note 1:** Typical Values: TA = 25°C, V<sub>DD</sub> = 3.3V.
TABLE 5-7: OTHER TIMING PARAMETERS AC CHARACTERISTICS\(^{(1)}\)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Condition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transmitter Switch On Time</td>
<td>Synthesizer off, crystal oscillator on with 10 MHz step</td>
<td></td>
<td>250</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Receiver Switch On Time</td>
<td>Synthesizer off, crystal oscillator on with 10 MHz step</td>
<td></td>
<td>250</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Transmitter to Receiver Switch Time</td>
<td>Synthesizer and crystal oscillator on during TX/RX change with 10 MHz step</td>
<td></td>
<td>150</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Receiver to Transmitter Switch Time</td>
<td>Synthesizer and crystal oscillator on during RX/TX change with 10 MHz step</td>
<td></td>
<td>150</td>
<td></td>
<td>μs</td>
</tr>
<tr>
<td>Crystal Load Capacitance (See Crystal Selection Guide)</td>
<td>Programmable in 0.5 pF steps, tolerance ±10%</td>
<td>8.5</td>
<td>—</td>
<td>16</td>
<td>pF</td>
</tr>
<tr>
<td>Crystal Oscillator Start-up Time</td>
<td>Default capacitance bank setting, crystal ESR &lt;50Ω Crystal load capacitance = 16 pF(^{(2)})</td>
<td></td>
<td>2</td>
<td>7</td>
<td>ms</td>
</tr>
<tr>
<td>Internal POR Time-out</td>
<td>After VDD has reached 90% of the final value(^{(3)})</td>
<td></td>
<td>—</td>
<td>100</td>
<td>ms</td>
</tr>
<tr>
<td>Wake-up Timer Clock Accuracy</td>
<td>Crystal oscillator must be enabled to ensure proper calibration at the start-up(^{(2)})</td>
<td></td>
<td>±10</td>
<td>—</td>
<td>%</td>
</tr>
<tr>
<td>Digital Input Capacitance</td>
<td></td>
<td></td>
<td>—</td>
<td>2</td>
<td>pF</td>
</tr>
<tr>
<td>Digital Output Rise/Fall Time</td>
<td>15 pF pure capacitive load</td>
<td></td>
<td></td>
<td>10</td>
<td>ns</td>
</tr>
</tbody>
</table>

**Note 1:** Typical Values: \(TA = 25°C, VDD = 3.3V\).

2: The crystal oscillator start-up time depends on the capacitance seen by the oscillator. Low capacitance and low-ESR crystal are recommended with low parasitic PCB layout design.

3: During the Power-on Reset period, commands are not accepted by the chip. In case of Software Reset (see WTSREG (Register 2-14)), the Reset time-out is typically 0.25 ms.
5.1 Timing Specification and Diagram

**TABLE 5-8: SPI TIMING SPECIFICATION**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum Value (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(t_{CH})</td>
<td>Clock High Time</td>
<td>25</td>
</tr>
<tr>
<td>(t_{CL})</td>
<td>Clock Low Time</td>
<td>25</td>
</tr>
<tr>
<td>(t_{SS})</td>
<td>Select Setup Time ((CS) falling edge to SCK rising edge)</td>
<td>10</td>
</tr>
<tr>
<td>(t_{SH})</td>
<td>Select Hold Time (SCK falling edge to (CS) rising edge)</td>
<td>10</td>
</tr>
<tr>
<td>(t_{SHI})</td>
<td>Select High Time</td>
<td>25</td>
</tr>
<tr>
<td>(t_{DS})</td>
<td>Data Setup Time (SDI transition to SCK rising edge)</td>
<td>5</td>
</tr>
<tr>
<td>(t_{DH})</td>
<td>Data Hold Time (SCK rising edge to SDI transition)</td>
<td>5</td>
</tr>
<tr>
<td>(t_{OD})</td>
<td>Data Delay Time</td>
<td>10</td>
</tr>
</tbody>
</table>

**FIGURE 5-1: SPI TIMING DIAGRAM**
5.2 Typical Performance Characteristics

FIGURE 5-2: CHANNEL SELECTIVITY AND BLOCKING\(^{(1,2)}\)

Note 1: LNA gain maximum, filter bandwidth 67 kHz, data rate 9.6 kbps, AFC switched off, FSK deviation ±45 kHz, \(V_{DD} = 2.7\) V.

2: The ETSI limit given in the figure is drawn by taking -106 dBm at 9.6 kbps typical sensitivity into account and corresponds to receiver class 2 requirements.
FIGURE 5-3: BER CURVES IN 433 MHz BAND

FIGURE 5-4: BER CURVES IN 868 MHz BAND
Table 5-9 shows the optimal receiver BBBW and transmitter deviation frequency (ΔfFSK) settings for different data rates, considering no TX/RX offset frequency. If the TX/RX offset (for example, due to crystal tolerances) has to be taken into account, increase the BW accordingly.

### TABLE 5-9: RX BW AND TX DEVIATION FREQUENCY FOR DIFFERENT BAUD RATES

<table>
<thead>
<tr>
<th>Baud Rate</th>
<th>1.2 kbps</th>
<th>2.4 kbps</th>
<th>4.8 kbps</th>
<th>9.6 kbps</th>
<th>19.2 kbps</th>
<th>38.4 kbps</th>
<th>57.6 kbps</th>
<th>115.2 kbps</th>
</tr>
</thead>
<tbody>
<tr>
<td>ΔTX in kHz</td>
<td>ΔfFSK – 45</td>
<td>ΔfFSK – 45</td>
<td>ΔfFSK – 45</td>
<td>ΔfFSK – 45</td>
<td>ΔfFSK – 90</td>
<td>ΔfFSK – 90</td>
<td>ΔfFSK – 120</td>
<td></td>
</tr>
</tbody>
</table>
FIGURE 5-5: RECEIVER SENSITIVITY OVER AMBIENT TEMPERATURE
(433 MHz, 2.4 kbps, ΔfFSK: 45 kHz, BW: 67 kHz)

FIGURE 5-6: RECEIVER SENSITIVITY OVER AMBIENT TEMPERATURE
(868 MHz, 2.4 kbps, ΔfFSK: 45 kHz, BW: 67 kHz)
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

**Legend:** XX...X  Product-specific information
Y  Year code (last digit of calendar year)
YY  Year code (last 2 digits of calendar year)
WW  Week code (week of January 1 is week '01')
NNN  Alphanumeric traceability code
\(^{e3}\) Pb-free JEDEC designator for Matte Tin (Sn)
*  This package is Pb-free. The Pb-free JEDEC designator \(^{e3}\) can be found on the outer packaging for this package.

**Note:** In the event, the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.
6.2 Package Details

This section provides the technical details of the packages.

16-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
16-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

<table>
<thead>
<tr>
<th>Units</th>
<th>MILLIMETERS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Dimension Limits</td>
</tr>
<tr>
<td>Number of Pins</td>
<td>N</td>
</tr>
<tr>
<td>Pitch</td>
<td>e</td>
</tr>
<tr>
<td>Overall Height</td>
<td>A</td>
</tr>
<tr>
<td>Molded Package Thickness</td>
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<td>Footprint</td>
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<tr>
<td>Foot Angle</td>
<td>Ø</td>
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<tr>
<td>Lead Thickness</td>
<td>c</td>
</tr>
<tr>
<td>Lead Width</td>
<td>b</td>
</tr>
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</table>

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-068A Sheet 2 of 2
16-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

RECOMMENDED LAND PATTERN

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<tr>
<td>Optional Center Pad Length</td>
<td>Y2</td>
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<tr>
<td>Optional Center Pad Width</td>
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<tr>
<td>Clearance Between Contact Pads</td>
<td>G1</td>
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<tr>
<td>Contact Pad To Center Pad</td>
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<td>Contact Pad Spacing</td>
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<td>Contact Pad Width (X16)</td>
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<tr>
<td>Contact Pad Length (X16)</td>
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<td>Distance Between Pads</td>
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<td>Overall Width</td>
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Notes:
1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2068A
APPENDIX A: READ SEQUENCE AND PACKET STRUCTURES

Figure 1 shows the STSREG read sequence with FIFO read as an example.

FIGURE A-1: STSREG READ SEQUENCE

![STSREG Read Sequence Diagram]

Note:
1. Applicable when the RXCEN bit is set using the PMCREG.
2. Applicable when the RXCEN bit is cleared using the PMCREG.
3. These bits are internally latched and the other bits are only multiplexed out.

TABLE A-1: RECOMMENDED FIFO PACKET STRUCTURES

<table>
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<tr>
<th>Length</th>
<th>Preamble</th>
<th>Synchronous Word/Network ID</th>
<th>Payload</th>
<th>CRC</th>
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<tr>
<td>Minimum Length</td>
<td>4-8 bits (0x0A or 0x05)</td>
<td>0xD4 (programmable)</td>
<td>—</td>
<td>4-bit-1 byte</td>
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<tr>
<td>Recommended Length</td>
<td>8-12 bits (e.g., 0xAA or 0x55)</td>
<td>0x2DD4 (D4 is programmable)</td>
<td>—</td>
<td>2 bytes</td>
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APPENDIX B: REVISION HISTORY

Revision A (March 2009)
This is the initial released version of this document.

Revision B (June 2009)
Major updates are done throughout the document.

Revision C (November 2011)
Minor corrections such as figures, language and formatting updates are incorporated throughout the document.
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Preliminary

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5. What deletions from the document could be made without affecting the overall usefulness?

6. Is there any incorrect or misleading information (what and where)?

7. How would you improve this document?
# MRF49XA

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**Example:**

a) MRF49XA-I/ST: Industrial temperature, TSSOP package.

b) MRF49XAT-I/ST: Industrial temperature, TSSOP package, tape and reel.

- **Device:** MRF49XA: Sub-GHz RF Transceiver
- **Temperature Range:** \(-40^\circ\)C to \(+85^\circ\)C (Industrial)
- **Package:** ST = TSSOP (Lead Plastic Thin Shrink Small Outline, No Lead)
- **T = Tape and Reel**
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