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NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a “DS” number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is “DSXXXXX”, where “XXXXX” is the document number and “A” is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE on-line help. Select the Help menu, and then Topics to open a list of available on-line help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the SMPS AC/DC Reference Design. Items discussed in this chapter include:

• Document Layout
• Conventions Used in this Guide
• Warranty Registration
• Recommended Reading
• The Microchip Web Site
• Development Systems Customer Change Notification Service
• Customer Support
• Document Revision History

DOCUMENT LAYOUT

This document describes how to use the SMPS AC/DC Reference Design as a development tool to emulate and debug firmware on a target board. The manual layout is as follows:

• Chapter 1. Introduction – This chapter introduces the SMPS AC/DC Reference Design and provides an overview of its features and background information.
• Chapter 2. Hardware Design – This chapter provides a functional overview of the SMPS AC/DC Reference Design and identifies the major hardware components.
• Chapter 3. Software Design – This chapter provides a functional overview of the software used in the hardware design and identifies the major software components.
• Chapter 4. System Operation – This chapter provides information on the system operation and setup for the SMPS AC/DC Reference Design.
• **Appendix A. Board Layouts and Schematics** – This appendix provides detailed technical drawings and schematic diagrams of the SMPS AC/DC Reference Design.

• **Appendix B. Source Code** – This appendix provides information on obtaining the source code referenced in this document.

• **Appendix C. References** – This appendix provides detailed information on all external references used throughout this document.
CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

<table>
<thead>
<tr>
<th>DOCUMENTATION CONVENTIONS</th>
<th>Description</th>
<th>Represents</th>
<th>Examples</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arial font:</td>
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<tr>
<td>Italic characters</td>
<td>Referenced books</td>
<td>MPLAB® IDE User’s Guide</td>
<td></td>
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<tr>
<td>Emphasized text</td>
<td>...is the only compiler...</td>
<td></td>
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<td>Initial caps</td>
<td>A window</td>
<td>the Output window</td>
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<td></td>
<td>A dialog</td>
<td>the Settings dialog</td>
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<td></td>
<td>A menu selection</td>
<td>select Enable Programmer</td>
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<td>Quotes</td>
<td>A field name in a window or dialog</td>
<td>“Save project before build”</td>
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<tr>
<td>Underlined, italic text with right angle bracket</td>
<td>A menu path</td>
<td>File&gt;Save</td>
<td></td>
</tr>
<tr>
<td>Bold characters</td>
<td>A dialog button</td>
<td>Click OK</td>
<td></td>
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<tr>
<td></td>
<td>A tab</td>
<td>Click the Power tab</td>
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<tr>
<td>N'Rnnnn</td>
<td>A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.</td>
<td>4'b0010, 2'hF1</td>
<td></td>
</tr>
<tr>
<td>Text in angle brackets &lt; &gt;</td>
<td>A key on the keyboard</td>
<td>Press &lt;Enter&gt;, &lt;F1&gt;</td>
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<td>Courier New font:</td>
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<tr>
<td>Plain Courier New</td>
<td>Sample source code</td>
<td>#define START</td>
<td></td>
</tr>
<tr>
<td>Filenames</td>
<td>autoexec.bat</td>
<td></td>
<td></td>
</tr>
<tr>
<td>File paths</td>
<td>c:\mcc18\h</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Keywords</td>
<td>_asm, _endasm, static</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Command-line options</td>
<td>-Opa+, -Opa-</td>
<td></td>
<td></td>
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<tr>
<td>Bit values</td>
<td>0, 1</td>
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<tr>
<td>Constants</td>
<td>0xFF, ‘A’</td>
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<tr>
<td>Italic Courier New</td>
<td>A variable argument</td>
<td>file.o, where file can be any valid filename</td>
<td></td>
</tr>
<tr>
<td>Square brackets [ ]</td>
<td>Optional arguments</td>
<td>mcc18 [options] file [options]</td>
<td></td>
</tr>
</tbody>
</table>
| Curly brackets and pipe character: { | Choice of mutually exclusive arguments; an OR selection | errorlevel {0|1} | }
| Ellipses...              | Replaces repeated text | var_name [, var_name...] | |
|                          | Represents code supplied by user | void main (void) { ... } | |
WARRANTY REGISTRATION

Please complete the enclosed Warranty Registration Card and mail it promptly. Sending in the Warranty Registration Card entitles users to receive new product updates. Interim software releases are available at the Microchip web site.

RECOMMENDED READING

This user's guide describes how to use SMPS AC/DC Reference Design. Other useful documents are listed below. The following Microchip documents are available and recommended as supplemental reference resources.

Readme Files
For the latest information on using other tools, read the tool-specific Readme files in the Readmes subdirectory of the MPLAB® IDE installation directory. The Readme files contain update information and known issues that may not be included in this user’s guide.

Application Notes
The following related SMPS application notes are available for download from the Microchip website:

- AN1106 “Power Factor Correction in Power Conversion Applications Using the dsPIC® DSC” (DS01106)
- AN1114 “Switch Mode Power Supply (SMPS) Topologies (Part I)” (DS01114)
- “Switch Mode Power Supply (SMPS) Topologies (Part II)” - scheduled for release in early 2008

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- **Emulators** – The latest information on Microchip in-circuit emulators. This includes the MPLAB ICE 2000 and MPLAB ICE 4000.
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- **MPLAB® IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB SIM simulator, MPLAB IDE Project Manager and general editing and debugging features.
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- Field Application Engineer (FAE)
- Technical Support
- Development Systems Information Line

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at: http://support.microchip.com

DOCUMENT REVISION HISTORY

Revision A (February 2008)

- Initial release of this document.
Chapter 1. Introduction

This chapter provides an introduction to the SMPS AC/DC Reference Design and includes the following major topics:

- System Specifications
- Block Diagram
- Multi-Phase Synchronous Buck Converter
- Listing of I/O Signals for Each Block, Type of Signal and Expected Signal Levels

1.1 SYSTEM SPECIFICATIONS

This reference design describes the design of an off-line Switch Mode Power Supply (SMPS) design using an SMPS dsPIC® DSC.

The SMPS AC/DC Reference Design unit works with universal input range and produces three outputs. The continuous output rating of the unit is 350 watts. This reference design is based on a modular structure having three major block sets as shown in Figure 1-2. Figure 1-3 shows a more detailed block diagram with all functional blocks as implemented on the SMPS AC/DC Reference Design.

The Power Factor Circuit converts the universal AC input voltage to constant high-voltage DC, and maintains the sinusoidal input current at high power factor. The Phase-Shift Zero Voltage Transition circuit converts high-voltage DC to intermediate low-voltage DC with isolation from the input AC mains, at high efficiency. The Multi-Phase Synchronous and Single-Phase Synchronous buck circuit converts intermediate low-voltage DC to very low-voltage DC at high current at high efficiency. The input and output specifications are as follows (this unit is designed to operate at 0°C to 50°C ambient temperatures at full load of operation):

- Input:
  - Input Voltage: 85 VAC - 264 VAC
  - Input Frequency: 45 Hz - 65 Hz
- Outputs:
  - Output voltage 1 \( (V_{o1}) = 12V\)
  - Output Load 1 \( (I_{o1}) = 0A - 29.27A\)
  - Output voltage 2 \( (V_{o2}) = 3.3V\)
  - Output Load 2 \( (I_{o2}) = 0A - 69A\)
  - Output voltage 3 \( (V_{o3}) = 5V\)
  - Output Load 1 \( (I_{o3}) = 0A - 23A\)
A conventional Switch Mode Power Supply (SMPS) must implement Power Factor Correction if it draws more than 75 watts from the AC Mains. The PFC circuitry draws input current in phase with input voltage, and the Total Harmonic Distortion (THD) of the input current should be less than 5%. The PFC provides a fixed DC high-output voltage, which needs to be converted to lower output Direct Current (DC) voltage and isolated with an input mains supply. Figure 1-2 shows a high-level block diagram of the SMPS AC/DC Reference Design. Figure 1-2 shows a detailed block diagram.

The SMPS AC/DC Reference Design operates on universal input voltage and produces multiple DC output voltages. The front-end PFC boost circuit converts universal AC input voltage to 405 VDC bus voltage. The phase-shift Zero Voltage Transition (ZVT) circuit produces 12 VDC output voltage from a 405 VDC bus. The phase-shift ZVT converter also provides output voltage isolation from the input AC mains. The multi-phase synchronous buck converter produces 3.3 VDC @ 69 Amps from the 12 VDC bus. The single-phase buck converter produces 5 VDC @ 23 Amps from the 12 VDC bus.

The following sections in this chapter provide an overview and background of the main power conversion blocks implemented in the SMPS AC/DC Reference Design.
1.2.1 Power Factor Correction (PFC)

Most power conversion applications consist of an AC-to-DC conversion stage immediately following the AC source. The DC output obtained after rectification is subsequently used for further stages. Current pulses with high peak amplitude are drawn from a rectified voltage source with sine wave input and capacitive filtering. Regardless of the load connected to the system, the current drawn is discontinuous and of short duration. Because many applications demand a DC voltage source, a rectifier with a capacitive filter is necessary. However, this results in discontinuous, short-duration current spikes.

1.2.1.1 OVERVIEW AND BACKGROUND INFORMATION

Two factors that provide a quantitative measure of the power quality in an electrical system are Power Factor (PF) and Total Harmonic Distortion (THD). The amount of useful power being consumed by an electrical system is predominantly decided by the PF of the system.

To understand PF, it is important to know that power has two components:

- **Working (or Active Power)**
  
  Working Power is the power that is actually consumed and registered on the electric meter at the consumer's location. Working power is expressed in kilowatts (kW), which register as kilowatt hour (kWh) on an electric meter.

- **Reactive Power**
  
  Reactive Power does no useful work, but is required to maintain and sustain the electromagnetic field associated with the industrial inductive loads such as induction motors driving pumps or fans, welding machines, and many more. Reactive Power is measured in kilovolt ampere reactive (kVAR) units. The total required power capacity, including Working Power and Reactive Power, is known as Apparent Power, expressed in kilovolt ampere (kVA) units.

Power Factor is a parameter that gives the amount of working power used by any system in terms of the total apparent power. Power Factor becomes an important measurable quantity because it often results in significant economic savings. Typical waveforms of current with and without PFC are shown in Figure 1-3.
These waveforms illustrate that PFC can improve the input current drawn from the mains supply and reduce the DC bus voltage ripple. The objective of PFC is to make the input to a power supply look like a simple resistor. The power factor correction circuitry provides power factor nearly equal to unity with very low current THD (< 5%).

This is an AC-to-DC converter stage, which converts the AC input voltage to a DC voltage and maintains sinusoidal input current at a high input Power Factor. As indicated in the Figure 1-4, three input signals are required to implement the control algorithm.

The Power Factor can be achieved with various basic topologies like buck topology, boost topology and buck-boost topology.

The input rectifier converts the alternating voltage at power frequency into unidirectional voltage. This rectified voltage is fed to the chopper circuit to produce a smooth and constant DC output voltage to the load. The chopper circuit is controlled by the PWM switching pulses generated by the dsPIC DSC device, based on three measured feedback signals:

- Rectified input voltage
- DC bus current
- DC bus voltage
1.2.1.2 PFC TOPOLOGIES

1.2.1.2.1 Buck PFC Circuit

In a buck PFC circuit, the output DC voltage is less than the input rectified voltage. Large filters are needed to suppress switching ripples and this circuit produces considerable Power Factor improvement. The switch (MOSFET) is rated to \( V_{IN} \) in this case. Figure 1-5 shows the circuit for the buck PFC stage. Figure 1-6 shows the buck PFC input current shape.
1.2.1.2.2 Boost PFC Circuit

The boost converter produces a voltage higher than the input rectified voltage, thereby giving a switch (MOSFET) voltage rating of \( V_{OUT} \). Figure 1-7 shows the circuit for the boost PFC stage. Figure 1-8 shows the boost PFC input current shape.

1.2.1.2.3 Buck/Boost PFC Circuit

In the buck/boost PFC circuit, the output DC voltage may be either less or greater than the input rectified voltage. High Power Factor can be achieved in this case. The switch (MOSFET) is rated to \( (V_{IN} + V_{OUT}) \). Figure 1-9 shows the circuit for the buck/boost PFC stage. Figure 1-10 shows the boost PFC input current shape.
Regardless of the input line voltage and output load variations, input current drawn by the buck converter and the buck boost converter is always discontinuous. However, when the boost converter operates in Continuous Conduction mode, the current drawn from the input voltage source is always continuous and smooth as shown in the Figure 1-8. This feature makes the boost converter an ideal choice for the Power Factor Correction (PFC) application. In PFC, the input current drawn by the converter should be continuous and smooth enough to meet Total Harmonic Distortion specifications for the input current (ITHD) of the input current such that it is close to unity. In addition, input current should follow the input sinusoidal voltage waveform to meet displacement factor such that it is close to unity.

### 1.2.2 Phase Shift ZVT Converter

A full-bridge converter is a transformer isolated buck converter. The basic schematic and switching waveform is shown in Figure 1-11. The transformer primary is connected between the two legs formed by the switches Q1,Q4 and Q3,Q2. The switches Q1,Q4 and Q3,Q2 create a pulsating AC voltage at the transformer primary. The transformer is used to step down the pulsating primary voltage, as well as to provide isolation between the input voltage source and the output voltage $V_{OUT}$. A full-bridge converter configuration retains the voltage properties of the half-bridge topology, and the current properties of push-pull topology. The diagonal switch pairs, Q1,Q4 and Q3,Q2, are switched alternately at the selected switching period. Since the maximum voltage stress across any switch is $V_{IN}$, and with the complete utilization of magnetic core and copper, this combination makes the full-bridge converter an ideal choice for high input voltage, high-power range SMPS applications.
In the full-bridge converter, four switches are used, thereby increasing the amount of switching device loss. The conduction loss of a MOSFET can be reduced by using a MOSFET with a low $R_{DS(ON)}$ rating. Switching losses can be reduced by using Zero Voltage Transition (ZVT), Zero Current Switching (ZCS) or both techniques. At high power output and high input voltage, the ZVT technique is preferred for the MOSFET. In a Phase Shift ZVT converter, the output is controlled by varying the phase of the switch Q3 with respect to Q1.

In this topology, the parasitic output capacitor of the MOSFETs and the leakage inductance of the switching transformer are used as a resonant tank circuit to achieve zero voltage across the MOSFET at the turn-on transition. There are two major differences in the operation of a phase-shift ZVT and simple full-bridge topology. In a phase-shift ZVT converter, the gate drive of both of the diagonal switches is phase shifted. In addition, both halves of the bridge switch network are driven through the complementary gate pulse with a fixed 50% duty cycle. The phase difference between the two half-bridge switching network gate drives control the power flow from primary to secondary, which results in the effective duty cycle.

Power is transferred to the secondary only when the diagonal switches are ON. If either the top or bottom switches of both legs are ON simultaneously, zero voltage is applied across the transformer primary. Therefore, no power is transferred to the secondary during this period. When the appropriate diagonal switch is turned OFF, primary current...
flows through the output capacitor of the respective MOSFETs causing switch drain voltage to move toward to the opposite input voltage rail. This creates zero voltage across the MOSFET to be turned ON next, thus creating zero voltage switching when it turns ON. This is possible when enough circulating current is provided by the inductive storage energy to charge and discharge the output capacitor of the respective MOSFETs. Figure 1-12 shows the gate pulse required, and the voltage and current waveform across the switch and transformer.

The operation of the phase-shift ZVT can be divided into different time intervals. Assuming that the transformer was delivering the power to the load, the current flowing through primary is IPK, and the diagonal switch Q1,Q2 was ON, at t = t0, the switch Q2 is turned OFF as shown in Figure 1-12.

**FIGURE 1-12:** REQUIRED GATE PULSES AND VOLTAGE AND CURRENT ACROSS PRIMARY

(A) = Gate pulse for all switches for phase-shift ZVT converter
(B) = Voltage across primary
(C) = Current across primary
1.2.2.1 TIME INTERVALS

- **Interval1: \( t_0 < t < t_1 \)**
  The switch Q2 is turned OFF, beginning the resonant transition of the right leg. Primary current is maintained constant by the resonant inductor LLK. This primary current charges the output capacitor of switch Q2 (\( \text{Coss}_2 \)) to the input voltage \( \text{Vin} \), which results in the output capacitance of Q3 (\( \text{Coss}_3 \)) being discharged to zero potential. This creates zero potential across the switch Q3 prior to turn-on, resulting in zero voltage switching. During this transition period, the transformer primary voltage decreases from \( \text{Vin} \) to zero, and the primary no longer supplies power to the output. Inductive energy stored in the output inductor and zero voltage across the primary cause both output rectifiers to share the load current equally.

- **Interval2: \( t_1 < t < t_2 \)**
  After charging \( \text{Coss}_2 \) to \( \text{Vin} \), the primary current starts flowing through the body diode of Q3. Now Q3 can be turned on any time after \( t_1 \) and have a zero voltage turn-on transition.

- **Interval3: \( t_2 < t < t_3 \)**
  At \( t = t_2 \), Q1 was turned OFF and the primary was maintained by the resonant inductor LLK. In addition, at \( t = t_2 \), \( IP \) is slightly less than the primary peak current \( IPK \) because of finite losses. The primary resonant current charges the output capacitor of switch Q1 (\( \text{Coss}_1 \)) to input voltage \( \text{Vin} \), which discharges the output capacitor of Q4 (\( \text{Coss}_4 \)) to zero potential, thus enabling zero voltage turn-on switching for Q4. During this transition, the primary current decays to zero. ZVS of the left leg switches depends on the energy stored in the resonant inductor, conduction losses in the primary switches, and the losses in the transformer winding. Since this left leg transition depends on leakage energy stored in the transformer, it may require an external series inductor if the stored leak energy is not enough for ZVS. Now, when Q4 is turned ON, voltage \( \text{Vin} \) is applied across the primary in the reverse direction.

- **Interval: \( t_3 < t < t_4 \)**
  The two diagonal switches Q3, Q4 are ON, applying full input voltage across the primary. During this period, the magnetizing current, plus the reflected secondary current into the primary flows through the switch. The exact diagonal switch-on time \( T_{ON} \) depends on the input voltage, the transformer turns ratio, and the output voltage. After the \( T_{ON} \) period of the diagonal switch, Q3 is turned OFF.
  One switching cycle is completed when the switch Q3 is turned OFF. The primary current charges \( \text{Coss}_3 \) to a potential of input voltage \( \text{Vin} \) and discharges \( \text{Coss}_2 \) to zero potential, thereby enabling ZVS for the switch Q2. The identical analysis is required for the next half cycle.

In the Phase-Shift ZVT Converter shown in Figure 1-11, the maximum transition time occurs for the left leg at minimum load current and maximum input voltage, and minimum transition time occurs for the right leg at maximum load current and minimum input voltage. Therefore, to achieve ZVT for all switches, enough inductive energy must be stored to charge and discharge the output capacitance of the MOSFET in the specified allocated time. Energy stored in the inductor must be greater than the capacitive energy required for the transition. The MOSFET output capacitance varies as applied drain-to-source voltage varies. Thus, the output capacitance of the MOSFET should be multiplied by a factor of \( 4/3 \) to calculate the equivalent output capacitance.
1.2.3 Buck Converter Description and Background

A buck converter, as its name implies, can only produce lower average output voltage than the input voltage. The basic schematic of a buck converter is shown in Figure 1-13. The switching waveforms for a buck converter are shown in Figure 1-14.

**FIGURE 1-13: BUCK CONVERTER**

In a buck converter, a switch (Q1) is placed in series with the input voltage source VIN. The input source VIN feeds the output through the switch and a low-pass filter, implemented with an inductor and a capacitor.

In a steady state of operation, when the switch is ON for a period of TON, the input provides energy to the output as well as to the inductor (L). During the TON period, the inductor current flows through the switch and the difference of voltages between VIN and VOUT is applied to the inductor in the forward direction, as shown in Figure 1-13. Therefore, the inductor current IL rises linearly from its present value IL1 to IL2.

During the TOFF period, when the switch is OFF, the inductor current continues to flow in the same direction, as the stored energy within the inductor continues to supply the load current. The diode D1 completes the inductor current path during the Q1 OFF period (TOFF); thus, it is called a freewheeling diode. During this TOFF period, the output voltage VOUT is applied across the inductor in the reverse direction, as shown in Figure 1-14. Therefore, the inductor current decreases from its present value IL2 to IL1.

**FIGURE 1-14: BUCK CONVERTER SWITCHING WAVEFORM**
The inductor current is continuous and never reaches zero during one switching period (Ts); therefore, this mode of operation is known as Continuous Conduction mode. In Continuous Conduction mode, the relation between the output and input voltage is given by Equation 1-1. The duty cycle is given by Equation 1-2.

**EQUATION 1-1:**

\[ V_{OUT} = D \cdot V_{IN} \]

where \( D \) is the duty cycle

**EQUATION 1-2:**

\[ D = \frac{t_{on}}{T_S} \]

where \( t_{on} \) is the ON time and \( T_S \) is the switching time period

When the output current requirement is high, the excessive power loss inside the freewheeling diode D1, limits the minimum output voltage that can be achieved. To reduce the loss at high current and to achieve lower output voltage, the freewheeling diode is replaced by a MOSFET with a very low ON state resistance (R\(_{DS(ON)}\)). This MOSFET is turned on and off synchronously with the buck MOSFET. Therefore, this topology is known as a synchronous buck converter. A gate drive signal, which is the complement of the buck switch gate drive signal, is required for this synchronous MOSFET.

A MOSFET can conduct in either direction; which means the synchronous MOSFET should be turned off immediately if the current in the inductor reaches zero because of a light load. Otherwise, the direction of the inductor current will reverse (after reaching zero) because of the output LC resonance. In such a scenario, the synchronous MOSFET acts as a load to the output capacitor, and dissipates energy in the \( R_{DS(ON)} \) (ON state resistance) of the MOSFET, resulting in an increase in power loss during discontinuous mode of operation (inductor current reaches zero in one switching cycle). This may happen if the buck converter inductor is designed for a medium load, but needs to operate at no load and/or a light load. In this case, the output voltage may fall below the regulation limit, if the synchronous MOSFET is not switched off immediately after the inductor reaches zero.
1.3 MULTI-PHASE SYNCHRONOUS BUCK CONVERTER

If the load current requirement is more than 35-40 amps, more than one converter is connected in parallel to deliver the load. To optimize the input and output capacitors, all the parallel converters operate on the same time base and each converter starts switching after a fixed time/phase from the previous one. This type of converter is called a multi-phase synchronous buck converter. Figure 1-15 shows the multi-phase synchronous buck converter. Figure 1-16 shows gate pulse timing relation of each leg and the input current drawn by the converter. The fixed time/phase is given by Time period/n or 300/n, where “n” is the number of the converters connected in parallel.

The design of input and output capacitors is based on the switching frequency of each converter multiplied by the number of parallel converters. The ripple current seen by the output capacitor reduces by “n” times. As shown in Figure 1-17, the input current drawn by a multi-phase synchronous buck converter is continuous with less ripple current as compared to a single converter. Therefore, a smaller input capacitor meets the design requirement in case of a multi-phase synchronous buck converter.

FIGURE 1-15: MULTI-PHASE SYNCHRONOUS BUCK CONVERTER

FIGURE 1-16: SWITCHING WAVEFORM OF SYNCHRONOUS BUCK CONVERTER
1.3.1 Auxiliary Supply Description

Auxiliary power supply is based on flyback topology. It generates voltage source for all the control circuitry and MOSFETs drivers for both sides of isolation boundary. Multiple output flyback converter is controlled by a TNY277G switch; the block diagram is shown in the Figure 1-17. Auxiliary power supply generates four isolated output, one low voltage for controller and one high voltage for MOSFETs drivers on either side of isolation barrier.

A flyback converter is a transformer-isolated converter based on the basic buck boost topology. In a flyback converter, a switch is connected in series with the transformer primary. The transformer is used to store the energy during the ON period of the switch, and provides isolation between the input voltage source VIN and the output voltage VOUT. During the TOFF period, the energy stored in the primary of the flyback transformer transfers to secondary through the flyback action. This stored energy provides energy to the load, and charges the output capacitor. Since the magnetizing current in the transformer cannot change instantaneously at the instant the switch is turned OFF, the primary current transfers to the secondary, and the amplitude of the secondary current will be the product of the primary current and the transformer turns ratio.

At the end of the ON period, when the switch is turned OFF, there is no current path to dissipate the stored leakage energy in the magnetic core of the flyback transformer. There are many ways to dissipate this leakage energy. One such method is shown in Figure 1-18 as a snubber circuit consisting of D, R and C. In this method, the leakage flux stored inside the magnetic core induces a positive voltage at the non-dot end primary winding, which forward-biases the diode D and provides the path to the leakage energy stored in the core, and clamps the primary winding voltage to a safe value. Because of the presence of the secondary reflected voltage on the primary winding and the leakage stored energy in the transformer core, the maximum voltage stress VDS of the switch is ~1.6 times the input voltage.
1.4 LISTING OF I/O SIGNALS FOR EACH BLOCK, TYPE OF SIGNAL AND EXPECTED SIGNAL LEVELS

1.4.1 PFC Boost Converter

As indicated in the block diagram in Figure 1-18, three input signals are required to implement the control algorithm. The only output from the dsPIC DSC device is firing pulses to the boost converter switch to control the nominal voltage on the DC bus, in addition to presenting a resistive load to the AC line. Table 1-1 shows the dsPIC DSC resources used by the PFC application.

FIGURE 1-18: RESOURCES REQUIRED FOR DIGITAL PFC

TABLE 1-1: RESOURCES REQUIRED FOR DIGITAL PFC

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Type of Signal</th>
<th>dsPIC DSC Resources Used</th>
<th>Expected Signal Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOUT</td>
<td>Analog</td>
<td>AN5</td>
<td>4.45V (nominal)</td>
</tr>
<tr>
<td>IPFC</td>
<td>Analog</td>
<td>AN4</td>
<td>2.4V (maximum)</td>
</tr>
<tr>
<td>VAC</td>
<td>Analog</td>
<td>AN6</td>
<td>4.56V (maximum)</td>
</tr>
<tr>
<td>PFC Gate Drive</td>
<td>PFC Drive Output, Digital</td>
<td>PWM4L</td>
<td>—</td>
</tr>
</tbody>
</table>
1.4.2 Phase-Shift ZVT converter

As indicated in the block diagram in Figure 1-19, three input signals are required to implement the control algorithm. The only output from the dsPIC DSC device is firing pulses to the full-bridge phase-shift ZVT and synchronous MOSFETs switch to control the nominal voltage on VOUT.

Table 1-2 shows the dsPIC DSC resources used by Phase-Shift ZVT application.

**TABLE 1-2: RESOURCES REQUIRED FOR DIGITAL PHASE-SHIFT ZVT**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Type of Signal</th>
<th>dsPIC DSC Resources Used</th>
<th>Expected Signal Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{ZVT1}$</td>
<td>Analog</td>
<td>AN0</td>
<td>4.45V (maximum)</td>
</tr>
<tr>
<td>$I_{ZVT2}$</td>
<td>Analog</td>
<td>AN2</td>
<td>2.4V (maximum)</td>
</tr>
<tr>
<td>VOUT</td>
<td>Analog</td>
<td>AN5</td>
<td>4.56V (maximum)</td>
</tr>
<tr>
<td>12V_Bus_ERROR_F/B</td>
<td>Analog</td>
<td>AN8</td>
<td>2.5V (maximum)</td>
</tr>
<tr>
<td>ZVT Gate Drive</td>
<td>Full bridge Drive Outputs, Digital</td>
<td>PWM1H, PWM1L, PWM2H, PWM2L</td>
<td>—</td>
</tr>
<tr>
<td>Synchronous Rectifier Gate Drive</td>
<td>Sync FET Drive Outputs, Digital</td>
<td>PWM3H, PWM3L</td>
<td>—</td>
</tr>
</tbody>
</table>
Table 1-2 shows the dsPIC DSC resources common for PFC and Phase-Shift ZVT converter.

TABLE 1-3: COMMON RESOURCES FOR PFC AND PHASE-SHIFT ZVT CONVERTER

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Type of Signal</th>
<th>dsPIC DSC Resources Used</th>
<th>Expected Signal Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Live_MCLR</td>
<td>Digital</td>
<td>MCLR</td>
<td>—</td>
</tr>
<tr>
<td>Live_PGC</td>
<td>Digital</td>
<td>PGC</td>
<td>—</td>
</tr>
<tr>
<td>Live_PGD</td>
<td>Digital</td>
<td>PGD</td>
<td>—</td>
</tr>
<tr>
<td>Live_Fault_Reset</td>
<td>Digital</td>
<td>SFLT4</td>
<td>—</td>
</tr>
<tr>
<td>Live_Fault</td>
<td>Digital</td>
<td>SFLT3</td>
<td>—</td>
</tr>
<tr>
<td>Live_RS232_RX</td>
<td>Digital</td>
<td>UART1 Receive</td>
<td>—</td>
</tr>
<tr>
<td>Live_Temp_Sense</td>
<td>Analog</td>
<td>AN9</td>
<td>2.5V</td>
</tr>
<tr>
<td>Live_RD1</td>
<td>Digital</td>
<td>RD1</td>
<td>—</td>
</tr>
<tr>
<td>Live_RA8</td>
<td>Digital</td>
<td>RA8</td>
<td>—</td>
</tr>
<tr>
<td>Live_SCL</td>
<td>Digital</td>
<td>SCL</td>
<td>—</td>
</tr>
<tr>
<td>Live_SDA</td>
<td>Digital</td>
<td>SDA</td>
<td>—</td>
</tr>
<tr>
<td>Live_RF15</td>
<td>Digital</td>
<td>RF15</td>
<td>—</td>
</tr>
<tr>
<td>Live_RF14</td>
<td>Digital</td>
<td>RF14</td>
<td>—</td>
</tr>
</tbody>
</table>
1.4.3 Synchronous Buck Converters

As indicated in the block diagram in Figure 1-20, the input signals are required to implement the control algorithm. The output from the dsPIC DSC device is firing pulses to the multi-phase as well as single-phase synchronous buck converter to the nominal voltages.

**FIGURE 1-20: RESOURCES REQUIRED FOR DIGITAL SYNCHRONOUS BUCK CONVERTERS**

Table 1-4 shows the dsPIC DSC resources used by multi-phase as well as single-phase synchronous buck converters.
### TABLE 1-4: RESOURCES REQUIRED FOR SYNCHRONOUS BUCK CONVERTERS

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Type of Signal</th>
<th>dsPIC DSC Resources Used</th>
<th>Expected Signal Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{5V}</td>
<td>Analog</td>
<td>CMP1A</td>
<td>2.4V (maximum)</td>
</tr>
<tr>
<td>5V Output</td>
<td>Analog</td>
<td>AN1</td>
<td>4.12V (nominal)</td>
</tr>
<tr>
<td>I_{3.3V_1}</td>
<td>Analog</td>
<td>AN2</td>
<td>2.4V (maximum)</td>
</tr>
<tr>
<td>I_{3.3V_2}</td>
<td>Analog</td>
<td>AN4</td>
<td>2.4V (maximum)</td>
</tr>
<tr>
<td>I_{3.3V_3}</td>
<td>Analog</td>
<td>AN6</td>
<td>2.4V (maximum)</td>
</tr>
<tr>
<td>3.3V Output</td>
<td>Analog</td>
<td>AN3</td>
<td>3.3V (nominal)</td>
</tr>
<tr>
<td>5V Buck Gate Drive</td>
<td>Single-Phase Synchronous Buck Drive</td>
<td>PWM4H, PWM4L</td>
<td>—</td>
</tr>
<tr>
<td>3.3V Buck Gate Drive</td>
<td>Multi-Phase Synchronous Buck Drive</td>
<td>PWM1H, PWM1L, PWM2H, PWM2L, PWM3H, PWM3L</td>
<td>—</td>
</tr>
<tr>
<td>Sense</td>
<td>Analog</td>
<td>AN5</td>
<td>4.285V</td>
</tr>
<tr>
<td>12V Digital Feedback</td>
<td>Digital</td>
<td>UART1 Transmit</td>
<td>—</td>
</tr>
<tr>
<td>Temperature Sense</td>
<td>Analog</td>
<td>AN8</td>
<td>2.4V</td>
</tr>
<tr>
<td>MCLR</td>
<td>Digital</td>
<td>MCLR</td>
<td>—</td>
</tr>
<tr>
<td>PGC</td>
<td>Digital</td>
<td>PGC</td>
<td>—</td>
</tr>
<tr>
<td>PGD</td>
<td>Digital</td>
<td>PGD</td>
<td>—</td>
</tr>
<tr>
<td>Fault</td>
<td>Digital</td>
<td>SFLT3</td>
<td>—</td>
</tr>
<tr>
<td>Fault_Reset</td>
<td>Digital</td>
<td>SFLT4</td>
<td>—</td>
</tr>
<tr>
<td>RD1</td>
<td>Digital</td>
<td>PortD1</td>
<td>—</td>
</tr>
<tr>
<td>RA8</td>
<td>Digital</td>
<td>PortA8</td>
<td>—</td>
</tr>
<tr>
<td>SCL</td>
<td>Digital</td>
<td>SCL</td>
<td>—</td>
</tr>
<tr>
<td>SDA</td>
<td>Digital</td>
<td>SDA</td>
<td>—</td>
</tr>
<tr>
<td>RF15</td>
<td>Digital</td>
<td>RF15</td>
<td>—</td>
</tr>
<tr>
<td>RF14</td>
<td>Digital</td>
<td>RF14</td>
<td>—</td>
</tr>
</tbody>
</table>
Chapter 2. Hardware Design

This chapter provides a functional overview of the SMPS AC/DC Reference Design and identifies the major hardware components. Topics covered include:

- PFC Boost Converter
- Full-Bridge ZVT Converter
- Single-Phase Synchronous Buck Converter
- 3-Phase Synchronous Buck Converter
- Auxiliary Power Supply

2.1 PFC BOOST CONVERTER

The conventional single-phase factor correction circuit is a standard boost converter topology operating from the full wave rectified mains input, as shown in Figure 2-1. The converter controller has an inner current control loop and outer voltage control loop. The current reference waveform is the input rectified mains voltage, so that the resultant current drawn from the mains is essentially sinusoidal and in-phase with the mains voltage. The amplitude of the current is controlled by the duty cycle of the fixed frequency PWM of the MOSFET, and is controlled by the PWM reference, which is the product of the current reference and the output of the DC link voltage error amplifier. Refer to Chapter 1. “Introduction” for details on the operation of this converter.

FIGURE 2-1: PFC POWER CONVERTER

EQUATION 2-1:

\[ D(t) = 1 - \frac{V_{ac}(t)}{V_{dc}} \]

EQUATION 2-2:

\[ THD = 100 \sqrt{\frac{I_{2}^2 - I_{1}^2}{I_{1}^2}} \]
2.1.1 Power-Train Design

The target specification for the PFC converter is as follows:

- Input voltage, $V_{IN} = 85 - 265$ Vrms
- Input frequency, $f_{in} = 45 - 65$ Hz
- Switching frequency, $f_{sw} = 125$ kHz
- Maximum Output voltage, $V_O = 400$ VDC
- Maximum Output power, $P_O = 450$ W
- Current THD < 5%

EMC standards for conducted, radiated and line current harmonics:

- FCC Class B
- EN55022 (CISPR 22) Class B
- EN61000-3-2 A14 Class A
- EN61000-3-3
- IEEE519

2.1.1.1 MOSFETS AND GATE DRIVE

MOSFETs are the preferred technology for the boost converter power switch because of the high operating frequency. The selected device must operate below its maximum junction temperature, so the losses need to be estimated. The rms current in the MOSFET switch can be approximated using Equation 2-3:

$$i_{\text{rms}} = \frac{P_o}{V_{ac} \sqrt{2}} \sqrt{2 - \frac{16V_{ac} \sqrt{2}}{3\pi V_{dc}}}$$

The maximum rms current occurs at minimum mains voltage, so the maximum normal operating MOSFET current is 4.6 Arms. Therefore, two TO-220 Infineon CoolMOS™ SPP11N60CFD 500V, 0.44Ω MOSFETs are connected in parallel, with each dissipating 2.3W of conduction loss. The MOSFET output capacitance is 390 pF so the switching loss is estimated at about 0.4W each. The actual loss in practice will be layout dependent and will probably be a factor of 2 higher, but still low in order to achieve high system efficiency.

The gate drive circuitry is a low-side Microchip TC1412N gate-drive IC, which drives the MOSFET gates directly. A single dsPIC DSC PWM module pin interfaces with the gate-drive IC via an inverting open-collector transistor stage which provides immunity against noise voltage differences between the boost converter common and dsPIC DSC signal common (ground bounce).

2.1.1.2 OUTPUT DIODE

The output diode must be rated for the mean output current, which is given by Equation 2-4:

$$\bar{i}_{\text{diode}} = \frac{P_o}{V_{dc}}$$
In this design, the diode must rated for 1.2A, so a STMicroelectronics STTH5R06D 600V, 5A TO-220 ultra-fast high-voltage rectifier has been selected. The typical forward voltage drop at high junction temperature is 1.4V, which means that the device will run cool with only 1.7W dissipation. There will be additional switching losses due to the high switching frequency and diode recovery characteristics. For a lower cost solution, a smaller axial diode may be used. Alternatively, if switching losses are an issue, then the recently introduced SiC Schottky diode looks like an attractive option.

2.1.1.3 PFC CHOKE

The target THD of the input current is 5%, which means the non-fundamental (50 Hz nominal) rms current component must be only 1% of input rms current. This component is the high-frequency ripple current in the boost inductor, and is dependent on the inductance. If it is assumed that on average, the duty cycle is 0.5. The ripple current rms of a triangular waveform is given by Equation 2-5:

\[ I_{rms} = \sqrt{\frac{I_{pk-pk}^2}{12}} \]

Therefore, for a 5.3 Arms input current we can only allow a maximum of 0.2A peak-to-peak, which will entail a rather large inductor size. However, the high frequency capacitor placed across the output terminals of the bridge rectifier will shunt-off most of the high frequency current, so that a larger component of ripple can be tolerated in a smaller inductor. Note that too large a capacitance will cause distortion in the current waveform, so a design compromise must be reached. The inductor current peak-to-peak ripple in a PFC boost converter varies over the whole cycle-mains cycle and depends on the input voltage, as shown in Equation 2-6:

\[ i_{ripple} = \frac{D\hat{V}_{ac}}{Lf_{sw}} \]

However, the absolute maximum value is independent of input voltage and is found from Equation 2-7:

\[ \hat{i}_{ripple} = \frac{V_{dc}}{4Lf_{sw}} \]

In this design, the ripple current is chosen to be 25% of the minimum voltage peak mains current; therefore, inductance of about 400 μH is required. The boost choke uses a Kool Mu 77548 core, which has an outside diameter of 33 mm. The \( L \) value for this core is 127. A single layer of 58 turns of 0.9 mm (19 AWG) enameled copper fits on the core giving an un-saturated inductance of 427 μH. From the Magnetics Inc. published wire-core tables, this results a predicted winding resistance of 77 mΩ at 100ºC. The variation of ripple current for a selection of input voltages is shown in Figure 2-2 and Figure 2-3.

The core loss can roughly estimated from the mean flux density over a complete mains cycle. The worst case condition occurs at roughly 180 Vrms, and the mean flux density is 180 mT which equates to a loss of xW.
FIGURE 2-2: INPUT VOLTAGE RIPPLE CURRENT VARIATION

FIGURE 2-3: CORE LOSSES FOR PFC CHOKE
2.1.1.4 PFC OUTPUT CAPACITOR

The PFC output capacitor provides bulk capacitance on the output of the PFC boost converter and smooths the DC voltage input to the ZVT full-bridge converter. The size of the capacitor is dictated by the hold-up requirements of the SMPS, its AC ripple current, and thermal life-time under normal operating conditions.

The capacitance must be high enough to maintain the PFC output voltage within acceptable bounds under normal peak power operating conditions and when a mains brown-out occurs. The required hold-up time, \( t_{\text{hold}} \), at the minimum mains frequency is 22 ms, therefore the conditions of Equation 2-8 must be met.

**EQUATION 2-8:**

\[
C > \frac{2t_{\text{hold}}P_o}{(V_{dc}^2 - V_{dc(\text{min})}^2)}
\]

For a minimum DC link voltage of 300V, a 330 \( \mu \)F is required. The actual capacitor selected is a Panasonic EET-ED2W331EA 35 x 40 mm electrolytic capacitor rated to 450 VDC and 105°C. The ESR at 20 kHz is 0.181\( \Omega \) and the maximum ripple current rating at 105°C is 2.64 Arms.

2.1.1.5 EMI FILTER

The SMPS AC/DC Reference Design has been designed to meet international standards for conducted EMC. The EMI filter between the mains input terminals and the PFC is a two-stage design because of the high switching frequency of the different stages in the SMPS. The circuit is shown in Figure 2-4. The two common-mode chokes are rated to 6 Arms and the 2.2 mH inductance forms a filter with the capacitors to Earth for common-mode noise. The leakage inductance of the chokes together with the capacitors across the live and neutral terminals, filter the differential-mode noise.

The six capacitors connected to Earth are 2.2 nF Y2-class capacitors meeting the CATII overvoltage category. The two X2-class capacitors are 220 nF. A transient spike voltage protection MOV is also fitted across the mains input, and a 330 k\( \Omega \) discharging resistor is fitted across the input to the SMPS to ensure that the filter capacitors discharge within one second.

**FIGURE 2-4: EMI FILTER**
2.2 FULL-BRIDGE ZVT CONVERTER

The main power circuit for a ZVT full-bridge converter is shown in Figure 2-5. It is a standard full-bridge converter; but, with additional series resonant inductance, which limits the rate of rise of current at switching transitions and can eliminate turn-off switching power dissipation in the MOSFETs. The stray leakage inductance of the transformer forms part of the series resonant inductor and in this particular design is large enough to ensure quasi-resonant operation over 80% of the operating power range without the need for an additional inductor. The secondary-side high-frequency rectification is normally done by using ultrafast recovery rectifiers or Schottky diodes. Alternatively, lower loss rectification can be achieved by using MOSFETs operating as synchronous rectifiers with primary-side commutation control, and this is the preferred solution in this reference design.

ZVT operation occurs when the stored energy in the inductor is transferred to the capacitor in parallel with the MOSFET. In this design, the stray output capacitance of the MOSFET is large enough not to require additional capacitors in parallel. From Reference 3 (see Appendix C. “References”), the equation relating energy in the MOSFET output capacitance and the series inductance for ZVT operation is given by Equation 2-9:

\[
\frac{1}{2} L_R I_{\text{pri}}^2 \geq \frac{4}{3} C_R V_{\text{in}}^2
\]

This ensures that there is more than enough energy to charge the MOSFET output capacitance and maintain ZVT operation. Note that at low output power, there will be far less energy stored in the resonant inductance and so ZVT operation will be lost. The inductor is therefore selected based on the minimum operating output power for ZVT switching.

The modulation control scheme required for ZVT operation of a full-bridge converter is phase-shifted PWM. The ideal power stage waveforms for the circuit are shown in Figure 2-6. The ZVT transition in the switch is short in comparison with the primary current transition time. This time, \( \Delta t \), is dictated by the resonant inductance, \( L_R \), and can be found from Equation 2-10:

\[
\Delta t = 2 \frac{L_R I_{\text{pri}}}{V_{\text{in}}}
\]

The control duty cycle is limited in a ZVT due to the time taken for the current to rise/fall during switching transitions. The maximum duty cycle, \( D_{\text{max}} \), achievable under ZVT operating conditions is given by Equation 2-11:

\[
D_{\text{max}} = 1 - \frac{2\Delta t}{T}
\]

The transformer turns ratio, \( n \), for the current doubling synchronous rectifier topology can then be selected for the required operating input and output voltages using the following ideal relationship shown in Equation 2-12:
EQUATION 2-12:

\[ n = D_{\text{max}} \frac{V_{in}}{2V_o} \]

The above equations governing the ZVT operation and resonant circuit component selection are also dependent on the peak primary current. If the output inductor magnetizing current is ignored, then the primary peak current is given by Equation 2-13:

EQUATION 2-13:

\[ I_{pri} = \frac{I_{o.in}}{n^2 V_o} \]

FIGURE 2-5: ZVT FULL-BRIDGE POWER CONVERTER WITH SYNCHRONOUS RECTIFICATION
FIGURE 2-6: ZVT WAVEFORMS

- $Q_1$
- $Q_4$
- $Q_2$
- $Q_3$
- $V_{pri}$
- $I_{pri}$
- $V_{sec}$
2.2.1 Full-Bridge ZVT Power-Train Design

The target specification for the ZVT full-bridge converter is as follows:

- Input voltage, $V_{IN} = 390 - 410$V
- Switching frequency, $f_{SW} = 250$ kHz
- Maximum output voltage, $V_O = 12$V
- Maximum output current, $I_O = 33$A

2.2.1.1 MOSFETS AND GATE DRIVE

Care must be taken when selecting the MOSFET switch for the ZVT full-bridge since there are potential failure modes associated with the diode characteristic and timing control at light loads (see Reference 4 in Appendix C. “References”). For this reference design, an Infineon CoolMOS CFD device has been selected because of its optimized diode characteristic. The SPA11N60CFD is a 600V, 0.44Ω MOSFET in a TO-220 package, and is a good compromise between cost and efficiency for this output power rating. The output capacitance, $C_{oss}$, is 45 pF and will form the resonant capacitor for ZVT operation.

Gate driving is typically achieved with either a proprietary high- and low-side high-voltage driver IC, or using a small transformer. These circuit techniques provide level-shifting of the dsPIC DSC gate firing signals and ensure that adequate voltage creepage and clearance distances are maintained in the layout. Given the high switching frequency in this application, the transformer isolated gate drive approach has been adopted. This is because of thermal concerns in standard gate driver ICs, although there are potential candidates from a number of manufacturers available on the market.

A single drive transformer with two secondary windings manufactured by Sirio Elettronica is used for each half-limb, and the turn-on switching time is controlled by a single resistor in each MOSFET gate. Turn-off is much faster due to the diode across the gate resistor. The drive for each transformer primary is provided by a Microchip TC1404, which is a dual high-speed CMOS driver IC. The dead-time for each MOSFET half-limb is inserted by the dsPIC DSC PWM peripheral module and is selected to avoid any possible shoot-through condition based on the timing delays inherent in the transformer gate drive circuitry.

2.2.1.2 TRANSFORMER

The following section describes a basic procedure for designing the ZVT full-bridge transformer. The optimum choice of ferrite core and winding turns/construction is dependent on many factors in the overall converter and may well involve a number of design optimization iterations.

The transformer turns ratio must be selected to ensure that voltage regulation is maintained at the maximum duty limit. As a starting point, $D_{max}$ is assumed to be 0.85, so for the minimum DC link voltage (390V) and the output voltage (12.5V), which includes the voltage drop across the synchronous rectifiers and output chokes the required transformer turns ratio is 13.3 or less (see Equation 2-12).

An ungapped ETD29 ferrite core pair is selected for the transformer. Table 2-1 lists the various parameters for ETD29 cores made of N87 material.

<table>
<thead>
<tr>
<th>TABLE 2-1: TRANSFORMER CORE DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_L$ (nH/Turn$^2$)</td>
</tr>
<tr>
<td>-----------------</td>
</tr>
<tr>
<td>ETD29</td>
</tr>
</tbody>
</table>
To compute the operating flux density and decide on the number of turns, it is assumed that the maximum allowable transformer temperature rise is 80ºC. The power converter will have forced air cooling from a lid mounted fan so the actual thermal resistance will be about a third less at around 10ºC/W. This means that the total power dissipation can be as much as 8W, with the losses split equally in the copper windings and the ferrite cores. From the core loss curves shown in Figure 2-7, the operating AC peak-to-peak flux density can be as high as 150 mT. The minimum number of turns at the given maximum operating duty is given by Equation 2-14:

\[
N_{\text{min}} = \frac{V_{\text{in}} D_{\text{max}} T}{2 A_e B_{\text{max}}}
\]

Therefore \(N_{\text{min}}\) is 58, which means that the secondary winding must have either four or five turns to give the required turns ratio computed above. A good solution is therefore 64 turns on the primary and five turns on the secondary with a turns ratio, \(n\), of 12.8.

\[\text{FIGURE 2-7: N87 POWER LOSS CURVES}\]

With the selected turns ratio from Equation 2-12, the actual operating duty, \(D\), is 0.82. Therefore the operating peak-to-peak flux density is 130 mT at 250 kHz. The core loss in a N87 core can be computed by Equation 2-15:

\[
P_{\text{core}} = 1.36 \times 10^{-4} f_{\text{sw}}^{1.59} B^{2.74} V_e
\]

where \(f_{\text{sw}}\) is in kHz and \(B\) is in mT.
Therefore, the predicted core loss is actually 2.9W. The next stage is now to optimize the winding designs to minimize the losses especially the high-frequency AC losses due to skin-effect and the proximity effect in multilayer windings (see Reference 5 and Reference 6 in Appendix C. “References”). The available winding width, $b_w$, must be reduced to accommodate a 3 mm creepage border on each side of the bobbin, leaving around 13 mm available for the windings. The total height of the two windings must be less than 4.5 mm which takes into account the layers of 0.05 mm inter-winding tape.

The secondary transformer winding rms current for the current-doubler synchronous rectifier, ignoring inductor ripple current, is given by the relationship shown in Equation 2-16:

**EQUATION 2-16:**

$$\bar{I}_{sec} = \frac{I_o}{2}$$

The secondary rms current is therefore 16.5A, but will be slightly higher in practice due to the magnetizing ramp component of current in the output inductors. For high current windings, copper foil is better suited to utilize the available winding area, and minimize AC copper losses. The secondary winding is a 5 turn strip of copper and the ideal foil height, $h_{id}$, in mm is given by Equation 2-17:

**EQUATION 2-17:**

$$h_{id} = \sqrt{\frac{9.74 \times 10^3}{N_s f_{sw}}}$$

So $h_{id}$ at 250 kHz is 0.088 mm. The resistance factor, $F_R$, is given by Equation 2-18:

**EQUATION 2-18:**

$$F_R = 1 + \frac{1}{3} \left( \frac{h}{h_{id}} \right)^4$$

when $\frac{h}{h_{id}} < 1.4$

So, for a practical foil thickness, $h$, of 0.1 mm, $F_R = 1.56$. The total resistance including AC effects is given by Equation 2-19:

**EQUATION 2-19:**

$$r = \frac{F_R I_m}{45 \times 10^6 b_w h}$$

where $I_m$ is the mean turn length and $b_w$ is the foil width.

The realistic foil width for the ETD29 is 13.0 mm. This means that the secondary resistance is 1.4 mΩ, which leads to a secondary winding copper loss of about 0.5 W. The current density is actually 14A/mm$^2$, although very high, the power loss is acceptable.
There is no requirement to reduce leakage inductance in the transformer design so the primary winding can be a single winding block. This may also reduce the inter-winding capacitance between primary and secondary and have an impact on EMC. For the low current primary with the large number of turns, round conductors are preferred. Equation 2-20 can be used to identify the ideal wire diameter at the operating frequency, which takes into account skin and proximity effects, and was derived through experimental work by Dowell in the 1960s (see Reference 7 in Appendix C. “References”).

**EQUATION 2-20:**

\[
d_{id} = 1.01 \left( \frac{17.1b_w}{SNf_{sw}} \right)^{\frac{1}{3}}
\]

where \( S \) is the number of strands and \( N \) is number of turns in winding portion.

The resistance factor for round conductors can then be computed from Equation 2-21:

**EQUATION 2-21:**

\[
F_R = 1 + \frac{1}{2} \left( \frac{d}{d_{id}} \right)^{6}
\]

The best fill factor is achieved by using seven-stranded Litz wire, so this is a starting point. Also assume four layers as an initial starting point with 16 turns per layer. So the ideal optimum wire diameter is 0.2 mm (32 AWG), giving a resistance factor of 1.5. A commercially available Litz wire has eight strands of 0.2 mm with an OD of 0.75 mm. The DC resistance per meter for single 0.2 mm strand at 100°C is 0.7074 Ω/m, so the resistance for one mean turn of eight strands is 4.7 mΩ. Therefore, the total adjusted AC resistance of the primary winding is 0.45 Ω. The primary current is 1.3 Arms for the estimated secondary current and selected transformer turns ratio, which leads to a primary winding loss of 0.8W. Therefore, the total transformer losses are estimated to be 4.2W in the ETD29 transformer, and will limit the total temperature rise to less than 80°C with forced air-cooling.

The primary Litz wire has a total OD of around 0.7 mm, so the four-layer primary winding height is about 3 mm. The secondary five-layer foil winding height, including inter-turn insulation, will be around 0.75 mm height, and this design will easily fit in the available 4.85 mm maximum winding window height. The final winding construction is shown in Figure 2-8. The primary winding start and finish are terminated to bobbin pins, while the secondary winding has flying leads which are soldered directly into the PCB.
The last check is to assess whether an additional inductor is needed for ZVT operation. The leakage inductance (Reference 8 in Appendix C. “References”) for a standard construction transformer is given by Equation 2-22:

**EQUATION 2-22:**

\[
L_L = \frac{4\pi \times 10^{-4} I_m N_p^2}{b_w} \left( c + \frac{h_p + h_s}{3} \right) \mu H
\]

where \( c \) is the space between the primary and secondary. All dimensions are in mm.

The ideal computed leakage inductance is 32 \( \mu H \), and so this meets the criteria of Equation 2-9 with the MOSFET output capacitance without requiring an additional resonant inductor. Provision has been made on the reference design PCB for an external inductor and parallel capacitors across the MOSFETs if the ZVT operation needs tuning.

### 2.2.2 Synchronous Rectifier Design

Synchronous rectification is the technique used for reducing the power loss in the output stage of switched mode power supplies (Reference 9 in Appendix C. “References”). The conventional diode is replaced by a MOSFET and is controlled so that current will flow in the third quadrant in the direction source to drain when the equivalent ISRDS(ON) voltage drop is lower than the intrinsic diode voltage drop. This means that with very low RDS(ON) MOSFETs, the power supply efficiency can be significantly increased. This is especially true in low output voltage power supplies.

In push-pull type power converters, there are a number of synchronous rectifier topologies. In this particular reference design, a current-doubler form has been used (see Reference 10 in Appendix C. “References”). Figure 2-9 illustrates the current paths for the four operating modes of the rectifier. The MOSFET commutation is
synchronized to the ZVT full-bridge switching and gate control signals are generated by the primary-side dsPIC DSC device and fed to the secondary-side via high-speed opto-isolators.

The operating waveforms for the synchronous rectifier are shown in Figure 2-10. As shown in the figure, switch $Q_6$ is gated when the primary current is positive, which coincides with the gating of switch $Q_4$, and $Q_5$ is synchronized with the primary bridge MOSFET $Q_3$ gate signal.

**FIGURE 2-9: CURRENT-DOUBLER SYNCHRONOUS RECTIFIER OPERATING MODES**

Note: Dotted lines with arrows indicate current polarity.
2.2.2.1 MOSFET SYNCHRONOUS RECTIFIERS AND GATE DRIVES

The MOSFET rectifiers selected for the synchronous rectifier are International Rectifier IRF2804SPBF 40V, 2 mΩ devices. They are packaged in a D²Pak and mounted directly onto the PCB. The minimum blocking voltage required is equal to the peak applied transformer secondary voltage. With the turns ratio of 12:8 and at the maximum input voltage of 410V, this is 32V. There will be very little overshoot voltage due to the compact layout achieved through mounting on the PCB, and the RC snubber across the secondary winding. The junction to ambient thermal resistance is 40ºC/W when mounted on a 25.4 mm² (1 inch²) PCB copper pad (see Reference 11 in Appendix C. “References”).

The MOSFETs internal diode voltage characteristic is 0.6V at 30A, 175ºC, which is significantly above the voltage drop across the 2 mΩ ON state resistance, and the benefits of synchronous rectification are maintained over the whole operating power region.

The gate-drive circuit employs a Microchip MCP1403 gate driver. The gate control signals are generated by the primary-side dsPIC DSC device so that they are synchronized with the ZVT full-bridge commutation. Isolation is achieved by high-speed opto-isolators.
2.2.2.2 OUTPUT CHOKE

There are two output chokes in the current-doubler synchronous rectifier. Each inductor's mean current is half the output current, and the fluxing voltage period occurs in only half of the cycle. Therefore the ripple current is given by Equation 2-23:

**EQUATION 2-23:**

\[
I_{\text{ripple}} = \frac{DT}{2L} \left( \frac{V_n}{n} - V_o \right)
\]

The choke is designed to have a 20% current ripple component, and the inductance is selected to give 3.3A at the nominal input voltage 400V. Therefore, the inductance needs to be 9 \( \mu \)H and the winding rated for a current of around 18A.

The Magnetics Kool Mu core iron loss can be computed from Equation 2-24:

**EQUATION 2-24:**

\[
P_c = \left( \frac{DT}{2N_A e} \left( \frac{V_n}{n} - V_o \right) \right)^2 f_{\text{cw}}^{1.46} \text{ W/m}^3
\]

The peak flux density is computed from Equation 2-25:

**EQUATION 2-25:**

\[
B_{pk} = \frac{LI_{pk}}{N_A e} \text{ T}
\]

Taking the 20.3 mm OD core No. 77848 with an \( A_L = 32 \) with \( A_e = 22.6 \text{ mm}^2 \), the required number of turns, \( N \), is 17. Therefore, the peak-to-peak AC flux density is 77 mT and the core loss is 0.5W. According to the single-layer winding data, 1.6 mm OD wire (14 AWG) will fit on the core so that the 13 x 0.315 mm will fit. The copper cross-sectional area is 1.01 mm\(^2\), so the current density is 17.7A/mm\(^2\). The resistance is estimated to be 7 m\( \Omega \) (double the 14 AWG resistance) and so the copper loss is 2.2W. With forced air-cooling this is acceptable.

2.2.2.3 OUTPUT CAPACITOR

The main output capacitor is a 2200 \( \mu \)F, 25V electrolytic with two 10 \( \mu \)F, 25V multilayer ceramic capacitors in parallel. The larger bulk capacitance provides the main energy storage while the small ceramic capacitors with very low ESR provide the high frequency ripple current decoupling capability. The capacitor ripple current is the combined AC components of the two output inductors plus the AC component of the synchronous buck loads. In the case of the inductor currents, this is lower compared to a conventional output rectifier due to the 50% phase shift in the inductor currents, and is dominated by current supplied to the synchronous buck regulators. The capacitor must also provide enough energy during a step load transient to maintain the 12V output voltage within the required regulated limits.
2.3 SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER

The synchronous buck converter uses the same basic topology as the standard step-down buck converter, but replaces the free-wheel diode with a MOSFET. Figure 2-11 shows the main power circuitry. The two switches are operated as a complementary pair with a dead-time inserted by the PWM controller to avoid shoot-through. The low-side MOSFET is operated in the third quadrant with current flowing from source to drain when the current is required to free-wheel, and due to the very lower ON state resistance of the MOSFET, higher efficiency is achieved compared with a conventional Schottky diode.

![FIGURE 2-11: SINGLE-PHASE SYNCHRONOUS BUCK CONVERTER](image)

2.3.1 Single-Phase Buck Converter Power-Train Design

The target specification for the single-phase buck converter is as follows:

- Input voltage, \( V_{IN} = 12 \text{ VDC} \)
- Switching frequency, \( f_{sw} = 500 \text{ kHz} \)
- Output voltage, \( V_O = 5 \text{ VDC} \)
- Output current, \( I_O = 23A \)
- Voltage ripple < 2%
- Output slew rate > 5 A/\( \mu \text{s} \)

2.3.1.1 MOSFETS AND GATE DRIVE

The equation governing the duty cycle of a buck converter is shown in Equation 2-26:

**EQUATION 2-26:**

\[
D = \frac{V_o}{V_{bus}}
\]

The rms currents in the high- and low-side MOSFETs, assuming a low inductor ripple current are as follows in Equation 2-27 and Equation 2-28:

**EQUATION 2-27:**

\[
\tilde{i}_{high} = I_o \sqrt{D}
\]
The nominal duty cycle is 0.42 ignoring stray voltage drops and inductor current ripple. This equates to a high-side MOSFET on-time, \( t_{\text{on}} \), of 840 ns. Therefore, the high-side MOSFET is rated for 14.9 Arms and the low-side MOSFET is rated for 17.5A.

The selected MOSFETs are International Rectifier IRL7833SPBF, 30V, 3.8 m\( \Omega \) devices in a D2PAK package, and are mounted directly onto the PCB. The intrinsic reverse diode of the MOSFET is relatively slow in switching, so a fast Schottky diode is placed in parallel across the MOSFET to reduce switching loss. The conduction losses of the high- and low-side MOSFETs are estimated at 0.85W and 1.2W respectively. It is possible in some designs to optimize the efficiency performance by selecting different devices for the high- and low-side switches.

The switching loss in the MOSFETs can be estimated by assuming ideal linear switching transitions using Equation 2-29:

\[
P_{\text{sw}} = \frac{1}{6} V_{\text{bus}} I_{\text{on}} t_{\text{on}} f_{\text{sw}}
\]

The estimated switching transition time is 50 ns, so that the switching loss for each device is 2.4W.

The gate drive circuitry is a dual Microchip MCP1404 gate-drive IC, which drives the MOSFET gates directly. The maximum gate threshold of each MOSFET is 4V, so the drive circuit for the high-side MOSFET is provided by the auxiliary SMPS power rail, which is higher than the gate threshold and source voltage combined. The PWM module pin of the dsPIC DSC device interfaces with the gate-drive IC via an inverting open-collector transistor stage which provides immunity against ground bounce.

### 2.3.1.2 OUTPUT CHOKES

The ripple current is given by the relationship shown in Equation 2-30:

\[
\Delta i = \frac{t_{\text{on}} (V_{\text{bus}} - V_0)}{L}
\]

The ripple current needs to be less than 25% of the output current so each output choke is a 1 \( \mu \)H Coilcraft SER1360-102KL surface mount. A smaller inductor would improve the output transient response, but at the expense of higher ripple current and consequently, higher output voltage ripple. The DC resistance is 2.5 m\( \Omega \) and the power loss is 1.3W for the maximum 23A output current. The peak-to-peak ripple current is 5.9A.
2.3.1.3 OUTPUT CAPACITOR

The output capacitor ripple current is fairly low in a buck converter due to the continuous inductor current, and is only dependent on the amplitude of ripple current in the inductor. The relationship for capacitor rms current is given by Equation 2-31:

\[
\tilde{i}_{cap} = \frac{\Delta i}{\sqrt{12}}
\]

Therefore, the total capacitor ripple current is 1.7 Arms. Another important design consideration for the bulk capacitors is the transient load requirements, so low ESR/ESL parts are required to meet the specification (see Reference 12 in Appendix C. “References”). Two Rubycon 10ZL1000M8X20 1000 µF, 10V electrolytic capacitors, plus four 10 µF, 16V multilayer ceramics in parallel. The electrolytic capacitors are each rated to 1.25 Arms at 105°C, which can easily handle the ripple current on their own.
2.4 3-PHASE SYNCHRONOUS BUCK CONVERTER

Multiple synchronous buck converters can be connected in parallel to increase the power handling of a step-down voltage stage. Performance improvements and a reduction in output capacitor size can be achieved by phase-shifting the PWM modulation in each stage. In this reference design, a 3-phase synchronous buck converter has been designed. The power circuit is shown in Figure 2-12 and illustrates the switching cycle 120 degree PWM phase-shifting in the output choke currents.

FIGURE 2-12: 3-PHASE SYNCHRONOUS BUCK CONVERTER
2.4.1 Multi-Phase Buck Converter Power-Train Design

The target specification for the multi-phase buck converter is as follows:

- Input voltage, \( V_{\text{IN}} = 12 \text{ VDC} \)
- Switching frequency, \( f_{\text{SW}} = 500 \text{ kHz} \)
- Output voltage, \( V_{O} = 3.3 \text{ VDC} \)
- Output power, \( I_{O} = 69 \text{ A} \)
- Voltage ripple < 2%
- Output slew rate > 50A/\mu s

2.4.1.1 MOSFETS AND GATE DRIVE

The output current for each phase buck stage is 23A and nominal duty cycle is 0.275 ignoring stray voltage drops and inductor current ripple. This equates to a high-side MOSFET on-time, \( t_{\text{on}} \), of 550 ns. Therefore, the high-side MOSFET is rated for 12 Arms and the low-side MOSFET is rated for 19.6A.

The selected MOSFETs are International Rectifier IRL7833SPBF, 30 V, 3.8 m\( \Omega \) devices in a D\(^2\)PAK package, and are mounted directly onto the PCB. The conduction losses of the high- and low-side MOSFETs are estimated at 0.55W and 1.5W respectively. The estimated switching transition time is 50 ns, so that the switching loss for each device is 1.2W.

The gate drive circuitry is a dual Microchip MCP1404 gate-drive IC, which drives the MOSFET gates directly. The maximum gate threshold of each MOSFET is 4V, so the drive circuit for the high-side MOSFET is provided by the auxiliary SMPS power rail, which is higher than the gate threshold and source voltage combined. The PWM module pin of the dsPIC DSC device interfaces with the gate-drive IC via an inverting open-collector transistor stage which provides immunity against ground bounce.

EQUATION 2-32:

\[
D = \frac{V_{O}}{V_{\text{bus}}}
\]

\[
i_{\text{high}} = I_{O} \sqrt{D}
\]

\[
i_{\text{low}} = I_{O} \sqrt{1-D}
\]

\[
P_{\text{sw}} = \frac{1}{6} V_{\text{bus}} I_{O} t_{\text{on}} f_{\text{SW}}
\]

2.4.1.2 OUTPUT CHOKES

The ripple current in each inductor is given by the relationship shown in Equation 2-33:

EQUATION 2-33:

\[
\Delta i = \frac{t_{\text{sw}} (V_{\text{bus}} - V_{0})}{L}
\]

The ripple current needs to be about 20% of the output current; therefore, each output choke is a 1 \( \mu \)H Coilcraft SER1360-102KL surface mount. The DC resistance is 2.5 m\( \Omega \) and the power loss is 1.3W. The peak-to-peak ripple current is 4.8A.
2.4.1.3 OUTPUT CAPACITOR

The output capacitor ripple current is very low due to the continuous inductor currents with phase-shifting. The relationship for capacitor rms current is given by Equation 2-34:

\[ i_{\text{cap}} = \frac{\Delta i}{\sqrt{3} \cdot \sqrt{12}} \]

Therefore, the total capacitor ripple current is 1.0 Arms. The output capacitor is made up of two Rubycon 6.3ZL1500M10X20 1500 \( \mu \)F, 6.3V electrolytic capacitors plus three 10 \( \mu \)F, 16V multilayer ceramics in parallel. The electrolytic capacitors are each rated to 1.82 Arms at 105ºC, and can easily handle the ripple current on their own.
2.5 **AUXILIARY POWER SUPPLY**

The supply voltages for the primary and secondary side dsPIC DSC device and gate drive circuitry are generated by a simple low-power flyback SMPS. Figure 2-13 illustrates the main components in the design. The integrated high-voltage proprietary controlled switch feeds a high-frequency transformer, and multiple secondary windings tapped-off via a diode/capacitor circuit. The SMPS operates in discontinuous flyback mode, so that energy is stored in the magnetizing inductance of the transformer during the switch on-period, and transferred to the secondary circuits during the off-period. A snubber arrangement is required across the transformer primary to dissipate the transformer parasitic leakage energy and ensure that the switch voltage does not exceed its maximum rating. The typical flyback MOSFET waveforms are shown in Figure 2-14.

**FIGURE 2-13: AUXILIARY FLYBACK SMPS**

![Auxiliary Flyback SMPS Diagram](image-url)
2.5.1 Basic Design Methodology

The target specification for the auxiliary flyback SMPS is as follows:
- Input voltage, $V_{IN} = 120 - 400 \text{ Vdc}$
- Primary Output Rail 1 = 7V @ 0.3A
- Primary Output Rail 2 = 13V @ 0.15A
- Secondary Output Rail 1 = 7V @ 0.3A
- Secondary Output Rail 2 = 17V @ 0.45A

2.5.1.1 HVIC TECHNOLOGY

The total output power rating of the SMPS is 13.8W; therefore, a Power Integrations TinySwitch (see Reference 13 in Appendix C. “References”) was selected for the main power switch. These devices are intended specifically for low-cost high-efficiency designs and operate with simple ON/OFF control rather than more sophisticated PWM common to higher power SMPS. The TNY277G is a suitably rated part for this wide input voltage application, and can be mounted directly onto the PCB without any additional cooling requirements.

2.5.1.2 TRANSFORMER

Based on the operating frequency and power throughput requirement, an EF20 ferrite core pair is selected for the transformer design. The first step in the design is to select the number of primary turns and transformer air-gap. A discontinuous flyback SMPS output power is dictated by the energy stored in the primary magnetizing inductance of the transformer and the switching frequency. The basic equation, ignoring losses, is shown in Equation 2-35:
EQUATION 2-35:

\[ P_o = \frac{1}{2} L_p I_p^2 f_{sw} \]

The peak current in the primary is fixed for a given output power and the switch on-time varies as a function of DC input voltage, as shown in Equation 2-36:

EQUATION 2-36:

\[ t_{on} = \frac{L_p I_p}{V_{DC}} \]

From the TNY277 data sheet, the maximum switching frequency is 140 kHz, and a sensible maximum on-time is 4.5 μs. The minimum DC voltage is 120V, and the power at the transformer primary is 17W, assuming ~ 80% efficiency. It is worth noting that this is only a transient requirement, since once the dsPIC DSC device rails are established, the PFC will boost the DC input voltage to 400V. Equation 2-35 and Equation 2-36 can be rearranged to find the required primary magnetizing inductance of the transformer, as shown in Equation 2-37:

EQUATION 2-37:

\[ L_p = \frac{t_{on}^2 V_{DC}^2 f_{sw}}{2 P_o} \]

Therefore, the target primary inductance is 1.2 mH and the peak primary current is 0.45A. The primary turns must be selected to ensure that the ferrite core losses are around 0.5W for thermal reasons. The EF20 core has a cross-sectional area of 32 mm² and a volume of 1490 mm³.

The core loss can be computed from Equation 2-38:

EQUATION 2-38:

\[ B = \left( \frac{P_{core}}{1.36 \times 10^{-4} f_{sw}^{1.59} V_c} \right)^{0.365} \]

where \( f_{sw} \) is in kHz and \( B \) is in mT.

Therefore, the peak flux density is about 150 mT. The required number of primary turns can be computed using Equation 2-39:

EQUATION 2-39:

\[ B = \frac{L_p I_p}{N_p A_c} \]

Using the above formula, \( N_p \) is set at 110 turns, which requires a 0.5 mm air-gap in the EF20 core to give 1.2 mH inductance. To minimize the leakage inductance of the transformer, and hence the loss in the snubber/clamp, the primary winding is split into two layers of 55 turns each. The rms current in the primary is given by Equation 2-40:
EQUATION 2-40:

$$i_p = \sqrt{\frac{D}{3}} I_p$$

From Equation 2-36, the on-time for the switch at 400V is 1.35 $\mu$s and the duty cycle is 0.19. Therefore, the rms current in the primary is 0.11 Arms. A suitable winding wire diameter is 0.16 mm with 5.5 A/mm$^2$. The 100ºC resistance of this wire is 1.1 $\Omega$mm$^{-1}$, and from the mean turn length of the bobbin (41.2 mm), the predicted primary resistance is 5Ω. Therefore, the primary copper loss is 60 mW.

The secondary turns must be selected to ensure that the referred voltage across the TNY277 does not exceed its maximum blocking voltage rating and for discontinuous current operation given the operating duty cycle. The peak voltage across the TNY277 when energy is transferred to the secondary is given by Equation 2-41:

EQUATION 2-41:

$$V_p = V_{DC} \frac{N_p}{N_s} V_o$$

A sensible limit on the maximum switch voltage is 540V, so for the main 17V secondary output, including a 0.8V diode forward voltage drop, the required turns ratio is 7.86. Therefore, the secondary turns on the 17V winding is 14. A separate tapping at six turns on this winding can be used for the 7V secondary. The secondary winding is constructed using TEX-E wire to give the required 2500 Vrms galvanic voltage isolation.

The time taken for the flyback transformer to be de-fluxed is given by Equation 2-42:

EQUATION 2-42:

$$t_{off} = \frac{N_s L_p I_p}{N_p V_o}$$

Therefore, the off-period is 3.9 $\mu$s, which is lower than the maximum available period to ensure discontinuous operation under normal operating conditions.

The secondary peak and rms currents in the winding are given by the following formulae in Equation 2-43 and Equation 2-44:

EQUATION 2-43:

$$I_s = \frac{2TI_o}{t_{off}}$$

EQUATION 2-44:

$$\tilde{i}_s = 2\sqrt{\frac{T}{3t_{off}}} I_o$$

Therefore, the secondary current in the main 17V output is 0.7 Arms. The secondary winding resistance is 0.1Ω and the total copper loss in the secondary winding is estimated to be 50 mW. Keeping a similar winding current density as the primary means that a 0.4 mm wire gauge can be chosen for the secondary windings. The two
auxiliary supply windings on the primary side follow directly from the chosen transformer turns ratio. The total transformer power dissipation is dominated by the iron loss and is roughly 0.8W. This will lead to a temperature rise of 40ºC, based on the published thermal characteristics of an EF20 transformer. Figure 2-15 illustrates the flyback transformer construction.

**FIGURE 2-15: FLYBACK TRANSFORMER CONSTRUCTION**

<table>
<thead>
<tr>
<th>3 layers 0.05 mm Melinex</th>
<th>8 turns of 0.4 mm</th>
<th>6 turns of 0.4 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 layers 0.05 mm Melinex</td>
<td>5 turns of 0.5 mm</td>
<td>6 turns of 0.5 mm</td>
</tr>
<tr>
<td>3 layers 0.05 mm Melinex</td>
<td>55 turns of 0.16 mm</td>
<td></td>
</tr>
</tbody>
</table>

### 2.5.1.3 OUTPUT CAPACITORS

The capacitors selected for outputs are 100 µF, 25V and 470 µF, 10V, for gate drive voltage rails and the dsPIC DSC device voltage rails, respectively. The ripple current rating for United Chemi-Con electrolytic capacitors are 0.34 Arms and 0.64 Arms, respectively.
Chapter 3. Software Design

3.1 OVERVIEW

The SMPS AC/DC Reference Design is controlled using two dsPIC DSCs as shown in the block diagram in Figure 3-1.

The dsPIC DSC on the primary side (on the left of the isolation barrier in Figure 3-1) controls the PFC Boost Converter and the Phase-Shift ZVT Converter. The dsPIC DSC on the secondary side (on the right of the isolation barrier in Figure 3-1) controls the Multi-Phase Buck Converter and the Single-Phase Buck Converter.

The secondary side dsPIC DSC also performs the function of measuring the output voltage of the Phase-Shift ZVT Converter, and feeding back to the primary side dsPIC DSC as a digital feedback signal.

FIGURE 3-1: BLOCK DIAGRAM OF SMPS AC/DC REFERENCE DESIGN
3.2 STRUCTURE OF THE CONTROL SOFTWARE

The control software for the SMPS AC/DC Reference Design essentially follows a single basic structure as shown in Figure 3-2.

FIGURE 3-2: FLOWCHART OF CONTROL SOFTWARE

The control software uses a mixture of C programming and assembly programming. All time-critical functions are written in assembly language. The main loop, peripheral setup routines, initialization routines and non-critical functions are all written using the C programming language.

The SMPS AC/DC Reference Design comprises of two separate projects, namely:

- **PFC_ZVT**: This project contains the complete code for the primary side of the SMPS AC/DC Reference Design. This includes the control software for the PFC Boost Converter and the Phase-Shift ZVT Converter.

- **DC_DC**: This project contains the complete code for the secondary side of the SMPS AC/DC Reference Design. This includes the control software for the Single-Phase Buck Converter and Multi-Phase Buck Converter, and also includes code for the ZVT output voltage measurement and digital voltage feedback.

All the functional blocks shown in Figure 3-2 are common to both projects. A brief description of each functional block is given below.
3.2.1 Initialization Routine

The initialization routines are called from the main program at the start of execution. All peripherals including PWM, ADC, Analog Comparator, UART, I2C and Timers are configured in this step. It is important that none of the peripherals are enabled before the entire peripheral configuration is completed.

In addition to configuring the peripherals, all required interrupts and interrupt priorities are configured in the initialization step. Memory allocation for control loop variables is also done during the initialization stage.

3.2.2 Peripheral Enable Routine

After configuring all peripheral modules that are used in the project, we enable them in the correct sequence. Since the PWM output directly affects the output of the system, it is important to enable it after all other peripherals have been enabled.

3.2.3 Idle Loop (Normal Operation)

The Idle loop is the main while loop in the program. All routines that are not time-critical must be performed in this loop. Typically these are tasks that need to be performed at a relatively slow speed compared to the system control loops. Some examples of these low-priority tasks are soft-start routines, temperature measurement, and power management routines.

3.2.4 Fault Loop

The Fault loop is used to handle any faults that have occurred in the system. This fault handling routine must only be used to process any information after a fault has occurred, and the system has been shut down.

The PWM module on the dsPIC30F2023 has built-in fault inputs that ensure a fast PWM shutdown in order to prevent damage to the system and downstream electronics. After the PWM is shutdown, a software flag causes the program execution to jump to the Fault loop.

Note: The critical part of fault handling (detection and PWM shutdown) is handled by the PWM module. The fault loop is a low priority fault handling routine to determine the course of action after the fault has been detected and the outputs have been turned OFF.

3.2.5 ADC Interrupt Service Routine

The ADC Interrupt Service Routine is the heart of the control software. All control loops are executed in the interrupt service routine. Since faster control loop execution is desired for the best system performance, functions executed in this routine are written in assembly language. The ADC Interrupt service routine has the highest priority of execution.

The ADC module is configured to generate interleaved interrupt requests in order to execute multiple control loops within the same interrupt service routine.

The implementation of the control software for each stage of the SMPS AC/DC Reference Design contains all the blocks described above. However, there are subtle differences in the implementation for each stage.

Specific details for each stage of the design are covered in subsequent sections of this user’s guide.
3.3 PRIMARY SIDE CONTROL SOFTWARE (PFC_ZVT)

The PFC Boost Converter and Phase-Shift ZVT Converter follow a similar control scheme. However, there are significant differences in the operation of these two converters. These differences will be explained in the description of the control software for each converter.

3.3.1 PFC Boost Converter Control Software

3.3.1.1 PFC CONTROL SCHEME

The control scheme implemented for the PFC Boost Converter is shown in Figure 3-3.

The PFC Boost Converter uses an outer voltage loop and inner current loop control scheme. The output of the voltage error compensator is multiplied by a function of the rectified AC mains voltage to generate a sinusoidal current reference.

An additional feed-forward term is introduced at the output of the voltage error compensator to make the control loop immune to fluctuations in the AC input voltage. This feed-forward term ensures that the PFC Boost Converter always delivers the correct output power for the entire input voltage range.

The PFC voltage and current error compensators are both implemented as PI (Proportional-Integral) systems with excess error compensation. The compensator functions are math intensive routines and utilize the DSP engine of the dsPIC DSC. The output of the PFC Current compensator modifies the PWM duty cycle to maintain a constant output voltage and also a sinusoidal input current waveform.

Both the current and voltage compensators are executed in the ADC interrupt service routine. The current control loop is executed at a much faster rate compared to the voltage control loop.
3.3.1.1.1 Digital PFC Implementation Using the dsPIC DSC

Figure 3-4 shows the hardware resources utilized on the primary side dsPIC DSC for Power Factor Correction.

**FIGURE 3-4: dsPIC® DSC RESOURCE ALLOCATION FOR PFC BOOST CONVERTER**

Table 3-1 lists the resources used on the dsPIC DSC for implementing the PFC control scheme shown in Figure 3-3.

**TABLE 3-1: dsPIC® DSC RESOURCES FOR PFC BOOST CONVERTER**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Type of Signal</th>
<th>dsPIC DSC Resource Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vout</td>
<td>Analog Input</td>
<td>AN5</td>
</tr>
<tr>
<td>IPFC</td>
<td>Analog Input</td>
<td>AN4</td>
</tr>
<tr>
<td>[VAC]</td>
<td>Analog Input</td>
<td>AN6</td>
</tr>
<tr>
<td>MOSFET Gate Drive</td>
<td>Drive Output</td>
<td>PWM4L</td>
</tr>
</tbody>
</table>

The control of the PFC Boost Converter is obtained by varying the duty cycle of the PWM signal. Only one pin of the PWM is utilized for the PFC control scheme, and therefore the PWM module is configured for independent output mode. The frequency of the PWM is determined by the hardware design. It is configured to be approximately 125 kHz.

The Analog Inputs AN4 and AN5 are configured to sample simultaneously. A conversion is triggered on both AN4 and AN5 once every 3 PWM cycles, and the current loop is executed on every conversion. The voltage loop is executed only once in 30 current loop executions.

The Analog Input AN6 measures the AC Input voltage, which is used for generating a sinusoidal current reference. In the SMPS AC/DC Reference Design, the current reference value is calculated once in six current loop executions.
3.3.2 Phase-Shift ZVT Control Scheme

3.3.2.1 ZVT RESOURCE ALLOCATION

The control scheme for the Phase-Shift ZVT Converter is shown in Figure 3-5.

FIGURE 3-5: PHASE-SHIFT ZVT CONVERTER CONTROL SCHEME

The ZVT converter uses current mode control to maintain a constant output voltage. The circuit configuration of the ZVT converter has the output voltage (the parameter to be controlled) on the secondary side of the isolation barrier (refer to Figure 3-8).

The SMPS AC/DC Reference Design implements the ZVT voltage feedback by measuring the output voltage using the secondary side dsPIC DSC. This 10-bit voltage data is transmitted back to the primary side dsPIC DSC through a UART communication channel.

The data received by the primary side dsPIC DSC is compared with the voltage reference to produce the voltage error. The voltage error compensator is then executed in the ADC interrupt service routine. The output of the voltage error compensator is the current reference value.

The measured current is compared with the calculated current reference from the voltage compensator to produce the current error. The current error compensator is executed and to produce the new PWM phase-shift value. The Phase-Shift ZVT converter uses the unique phase-shifting capability of the PWM module in the dsPIC30F2023. The phase of the PWM signal can be modified by simply writing the new value in the appropriate special function register in the PWM module.
Current sensing for the Phase-Shift ZVT Converter uses two dedicated analog inputs to measure the primary transformer current in both directions. The two analog inputs are tied to the same current signal, but are sampled at opposite current peaks. The precise triggering instants are in Figure 3-6 along with the expected current waveform. The current in the positive and negative directions must be measured and checked for any imbalance. If the currents in the two directions are not balanced, it may cause a phenomenon called “flux walking” in the ZVT transformer. Flux walking must be prevented because it may lead to transformer saturation and subsequent damage to the system hardware.

**FIGURE 3-6: ZVT FULL-BRIDGE CONVERTER**
The current and voltage compensators are implemented as Proportional-Integral-Derivative (PID) functions. Both functions are executed in the ADC interrupt service routine. The current control loop is executed at a faster rate compared to the voltage control loop.
3.3.2.2 PHASE-SHIFT ZVT IMPLEMENTATION USING THE dsPIC DSC

FIGURE 3-8: dsPIC® DSC RESOURCE ALLOCATION FOR PHASE-SHIFT ZVT CONVERTER

Table 3-2 lists the resources used on the primary side dsPIC DSC for the different feedback and control signals required for the Phase-Shift ZVT Converter control scheme. Table 3-3 lists resources used on the secondary side dsPIC DSC, also required for the Phase-Shift ZVT Converter control scheme.

**TABLE 3-2: PRIMARY SIDE dsPIC® DSC RESOURCES FOR PHASE-SHIFT ZVT CONVERTER**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Type of Signal</th>
<th>dsPIC DSC Resource Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>IZVT1</td>
<td>Analog Input</td>
<td>AN0</td>
</tr>
<tr>
<td>IZVT2</td>
<td>Analog Input</td>
<td>AN2</td>
</tr>
<tr>
<td>Vout</td>
<td>UART Input</td>
<td>U1RX</td>
</tr>
<tr>
<td>Vout Feedback</td>
<td>UART Output</td>
<td>U1TX</td>
</tr>
<tr>
<td></td>
<td>(secondary side)</td>
<td></td>
</tr>
<tr>
<td>Full-Bridge Gate Drive</td>
<td>Drive Output</td>
<td>PWM1H, PWM1L, PWM2H, PWM2L</td>
</tr>
<tr>
<td>Synchronous Rectifier Gate Drive</td>
<td>Drive Output</td>
<td>PWM3H, PWM3L</td>
</tr>
</tbody>
</table>

**TABLE 3-3: SECONDARY SIDE dsPIC® DSC RESOURCES FOR PHASE-SHIFT ZVT CONVERTER**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Type of Signal</th>
<th>dsPIC DSC Resource Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vout</td>
<td>Analog Input</td>
<td>AN5</td>
</tr>
<tr>
<td>Vout Feedback</td>
<td>UART Output</td>
<td>U1TX</td>
</tr>
</tbody>
</table>
The Phase-Shift ZVT Converter is controlled by modifying the phase of the PWM drive signals of one leg of the full-bridge relative to the drive signals of the other leg of the full-bridge.

As specified in Table 3-2, PWM1H, PWM1L, PWM2H and PWM2L are the PWM signals used for switching the full-bridge MOSFETs. PWM1H and PWM1L control one leg of the full-bridge, while PWM2H and PWM2L control the second leg of the full-bridge.

Both PWM1 and PWM2 are configured to operate in the complementary PWM mode and approximately 250 kHz switching frequency. The duty cycle of these PWM signals is fixed at 50%. Some dead time is also inserted to prevent shoot-through.

PWM3 is used for driving the synchronous rectifier MOSFETs on the secondary side of the ZVT Transformer. PWM3 is also configured as a complementary mode PWM signal with dead time. The PWM3 signal is configured identical to PWM1. The output of the control loop directly modifies the phase of PWM2 to accomplish the control of the output.

AN0 and AN2 both measure the ZVT current, but the each input is sampled on opposite peaks of the current signal. The conversion result of AN0 is used for the ZVT current loop. The voltage feedback is received on the U1RX pin of the primary side dsPIC DSC. The ZVT current is sampled once every six PWM cycles.

The voltage loop is executed at the same rate as the current loop, but the measured voltage is only updated every time a byte of data is received by the UART. This UART data reception is asynchronous to the PWM drive signals.

3.3.3 Primary Side Software Time Management

Both the PFC and ZVT converters are controlled using a single dsPIC DSC. The execution rates are carefully chosen to effectively utilize the available processing bandwidth of the dsPIC DSC. The flexible PWM-ADC trigger feature of the dsPIC30F2023 enables precise sampling of analog signals and interleaved control loop execution.

Figure 3-8 shows the interleaved control loop execution as implemented on the primary side control software on the SMPS AC/DC Reference Design.
FIGURE 3-9: INTERLEAVED CURRENT LOOP EXECUTION

- **PFC Current Trigger:** Once every 3 PFC Cycles
- **ZVT Current Trigger 1:** Once every 6 ZVT Cycles
- **PFC Current Trigger:** Once every 3 PFC Cycles

- **ZVT Current Trigger 2:** Once every 8 ZVT Cycles

- **Sample and Convert:** AN0, AN1 and Hold Values
- **Sample and Convert:** AN4, AN5
3.4 SECONDARY SIDE CONTROL SOFTWARE (DC_DC)

3.4.1 Single-Phase Buck Converter

3.4.1.1 SINGLE-PHASE BUCK CONVERTER CONTROL SCHEME

The Single-Phase Buck Converter on the SMPS AC/DC Reference Design uses peak current mode control. The control scheme is shown in Figure 3-10.

The control loop is implemented by utilizing the Analog Comparator module. The buck MOSFET current is sensed using a current transformer and fed directly to the analog comparator input.

FIGURE 3-10: SINGLE-PHASE BUCK CONVERTER CONTROL SCHEME

The measured output voltage is compared with the reference to produce the voltage error. The voltage error compensator is then executed and a current reference value is obtained.

The Analog Comparators on the dsPIC30F2023 have built-in programmable Digital-to-Analog Converters (DACs) that determine the comparator threshold. The calculated current reference is used to set a new threshold for the analog comparator.

When the inductor current signal exceeds the programmed threshold, the comparator terminates the PWM pulse. This termination of the PWM pulse effectively modifies the ON time for the PWM signal to control the output voltage.

The Voltage Error Compensator is implemented as a PID function. It is called from the ADC Interrupt Service Routine. The current control loop is implemented on the dsPIC DSC using the Analog Comparator by varying the programmable threshold in software.

3.4.1.2 SINGLE-PHASE BUCK CONVERTER IMPLEMENTATION USING THE dsPIC DSC

The resources used on the secondary side dsPIC DSC for the Single-Phase Buck Converter are summarized in Table 3-4.

TABLE 3-4: dsPIC® DSC RESOURCE ALLOCATION FOR SINGLE-PHASE BUCK CONVERTER

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Type of Signal</th>
<th>dsPIC DSC Resource Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isingle_buck</td>
<td>Analog Comparator Input</td>
<td>CMP1A</td>
</tr>
<tr>
<td>Vout_single_buck</td>
<td>Analog Input</td>
<td>AN1</td>
</tr>
<tr>
<td>Single-Phase Synchronous Buck Gate Drive</td>
<td>Drive Output</td>
<td>PWM4H, PWM4L</td>
</tr>
</tbody>
</table>
The output voltage is measured using analog input AN1. The Analog Comparator input CMP1A is connected to the output of the current transformer. The output voltage is controlled by varying the duty cycle of PWM4.

PWM4 pair is operated in the complementary mode with dead time. The switching frequency is approximately 500 kHz. The duty cycle is controlled directly by the built-in cycle-by-cycle Current-Limit mode and the Analog Comparator.

When the current-sense signal at the input of the Analog Comparator exceeds the programmed comparator threshold, the PWM output is immediately terminated for the remainder of the PWM cycle.

The Single-Phase Buck Converter circuitry is designed to operate in continuous conduction mode at load currents greater than approximately 3A. If the Single-Phase Buck Converter is operated in the discontinuous conduction mode, the freewheeling MOSFET is disabled through software.

At no load and light load current (< 3A), the PWM output may enter a “burst” mode. This is caused by a low demand for load current by the converter in this range load current.

The voltage control loop is executed in the ADC Interrupt Service Routine once in four PWM cycles.

### 3.4.2 Multi-Phase Buck Converter

#### 3.4.2.1 MULTI-PHASE BUCK CONVERTER CONTROL SCHEME

Voltage Mode control is used for controlling the output of the Multi-Phase Buck Converter on the SMPS AC/DC Reference Design. As shown in Figure 3-11, the control scheme only implements a single control loop.

![Multi-Phase Buck Converter Control Scheme Diagram](image)

The output voltage is compared with the reference and results in a voltage error, which is fed as an input to the voltage error compensator. The output of the voltage error compensator modifies the duty cycle of all phases of the Multi-Phase Buck Converter. The voltage error compensator is implemented as a PID function that is called in the ADC interrupt service routine.
The converter comprises 3 individual phases, but the output is controlled by a single duty cycle that identically drives the 3 phases. The PWM drive signals for each phase are phase shifted by 120° using the built-in PWM phase-shifting feature available on the dsPIC30F2023. The PWM drive signals for the Multi-Phase Buck Converter are shown in Figure 3-12.

FIGURE 3-12: MULTI-PHASE BUCK CONVERTER PWM DRIVE SIGNALS

3.4.2.2 MULTI-PHASE BUCK CONVERTER IMPLEMENTATION USING THE dsPIC DSC

Table 3-5 summarizes the resource allocation for the Multi-Phase Buck Converter.

TABLE 3-5: dsPIC® DSC RESOURCE ALLOCATION FOR MULTI-PHASE BUCK CONVERTER

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Type of Signal</th>
<th>dsPIC DSC Resource Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>Imulti_buck1</td>
<td>Analog Comparator Input</td>
<td>CMP2A</td>
</tr>
<tr>
<td>Imulti_buck2</td>
<td>Analog Comparator Input</td>
<td>CMP3A</td>
</tr>
<tr>
<td>Imulti_buck3</td>
<td>Analog Comparator Input</td>
<td>CMP4A</td>
</tr>
<tr>
<td>Vout_multi_buck</td>
<td>Analog Input</td>
<td>AN3</td>
</tr>
<tr>
<td>Multi-Phase Synchronous Gate Drive</td>
<td>Drive Outputs</td>
<td>PWM1H, PWM1L, PWM2H, PWM2L, PWM3H, PWM3L</td>
</tr>
</tbody>
</table>

The output voltage is measured from the analog input AN3. As this converter uses voltage mode control, there is no need for current measurement. However, over-current protection must be provided for each individual phase. Over-current protection is implemented using the Analog Comparators on the dsPIC30F2023. CMP2A, CMP3A and CMP4A are used for the over-current sensing for the Multi-Phase Buck Converter.
Each of the three phases is driven by a pair of complementary PWM signals. The PWM module on the dsPIC30F2023 provides a built-in mode to generate a pair of complementary PWM outputs with dead-time insertion. The PWM module also has a feature to generate a Master Period and Master Duty Cycle for multiple outputs. PWM1, PWM2 and PWM3 are all configured for a PWM switching frequency of approximately 500 kHz, and complementary mode operation with dead time.

PWM2 is phase advanced by 120° from PWM1, and PWM3 is phase advanced by 120° from PWM2 (or 240° from PWM1). The voltage control loop is executed once in 4 PWM cycles. The control loop is called from the ADC interrupt service routine.

The output of the voltage control loop is used to directly modify the PWM Master Duty Cycle to control the output voltage.

### 3.4.3 Secondary Side Software Time Management

The Single-Phase Buck Converter and Multi-Phase Buck Converter are both controlled digitally by the same dsPIC DSC. Both converters operate at the same switching frequency.

The two control loops are executed in an interleaved manner as shown in Figure 3-13. The execution rate for each control loop is once every four PWM cycles. The execution rate is determined by the execution times of each control loop.

The ADC Interrupt Service Routine assumes the highest priority of all user software. Other interrupts are assigned lower priority than the ADC interrupt, and all auxiliary software functions are performed in the “Idle loop” (when the ADC interrupt not being serviced).

**FIGURE 3-13:** INTERLEAVED CONTROL LOOP EXECUTION FOR SINGLE-PHASE AND MULTI-PHASE BUCK CONVERTERS
3.5 AUXILIARY SOFTWARE ROUTINES

3.5.1 Output Sequencing

Many applications require specific turn-on and turn-off sequencing of power supplies to ensure correct operation of the down-stream electronics. The SMPS AC/DC Reference Design implements power-on sequencing in the following order:

1. Initial start-up delay (allows all circuitry to stabilize after power-up).
2. PFC Converter ramps to around 405V.
3. Phase-Shift ZVT Converter ramps to 12V.
4. Single-Phase Buck Converter ramps to 5V.
5. Multi-Phase Buck Converter ramps to 3.3V.

Turn-off sequencing is only implemented on the Buck Converter outputs. If the output of the Phase-Shift ZVT Converter drops below 10V, both the Buck Converter outputs are configured to turn OFF simultaneously.

The sequencing software is implemented simply by polling the input voltage of the respective converter in the idle loop. If the measured input voltage is above the turn-on voltage, the appropriate soft-start flag is set, and the soft-start routine is executed. Similarly, if the input voltage drops below the turn-off voltage, the appropriate soft-shutdown flag is set and the soft-shutdown routine is executed.

3.5.2 Soft Start and Soft Shutdown

Each individual stage of the SMPS AC/DC Reference Design employs a controlled soft-start routine. At power up, all reference set-points are configured to produce 0V output. Once the power-on delay has lapsed, the respective soft-start flag is set and the reference set-point is incremented in the idle loop.

Every time the program execution arrives in the idle loop, the status of the soft-start flag is checked again. If soft-start is still active, the reference set-point is incremented again. This process continues until the final reference set-point is reached, and the soft-start flag is cleared.

A similar algorithm is implemented for soft-shutdown of the Buck Converters. When the input voltage drops below the turn-off voltage, the soft-shutdown flag is set. When program execution arrives in the idle loop, the reference set-point is decremented in small steps until the reference becomes zero.

3.5.3 Overtemperature Protection

Temperature sensors are provided on the SMPS AC/DC Reference Design in two positions. Overtemperature protection must be enabled to prevent damage to the system in the event of:

• Insufficient airflow in the system caused by failure of the cooling fan
• Operation of the system at a high ambient temperature

The implementation detail for each sensor is described in the following sections.

3.5.3.1 METAL ENCLOSURE OVERTEMPERATURE PROTECTION

This sensor is a digital temperature sensor. Temperature is transmitted digitally to the primary side dsPIC DSC using an I2C interface. The dsPIC DSC is configured as an I2C Master device. The temperature sensor is an I2C Slave device.

The dsPIC DSC requests data from the temperature sensor in the idle loop. The data received is compared with the maximum temperature set-point. The set-point is configured to approximately 60°C. If the measured temperature is above the maximum set-point, then a fault is generated and the PWM outputs are turned OFF.
3.5.3.2 PCB OVERTEMPERATURE PROTECTION

The PCB temperature sensor is located on the secondary side at the middle of the four buck phases. An analog temperature sensor is chosen that outputs an analog voltage proportional to the measured temperature.

The output of the temperature sensor is connected to analog input AN8 on the secondary side dsPIC DSC. The measured temperature is polled in the idle loop. The maximum temperature set-point is configured to approximately 90°C. If the measured temperature exceeds the maximum set-point, then a fault is generated and the PWM outputs are turned OFF.

3.5.4 Input AC Undervoltage Protection

The PFC Boost Converter is designed to operate normally for input voltages in the range 85V – 265V. In the event of an under-voltage condition, the circuit components will undergo excessive stress due to the additional current drawn by the system to deliver maximum output power. An undervoltage shutdown scheme must therefore be implemented to prevent damage to the system and load.

There are instances when the power grid may exhibit momentary voltage fluctuations, which must be ignored by the system.

The Input AC under-voltage protection is implemented in software by polling the average input voltage in the idle loop. The average input voltage is calculated as a part of the PFC control scheme, and is polled in the idle loop to detect a sustained undervoltage condition.

When an undervoltage condition is detected the first time, a counter is incremented. If the under-voltage condition remains for an extended period of time, a fault is generated and the outputs are turned OFF.

3.5.5 Fault Source Identification

If a fault condition is detected, it is often required that the system be turned OFF to prevent damage. The PWM module on the dsPIC30F2023 has a built-in latched fault mode. Using this latched fault mode, the PWM outputs can be immediately turned OFF with no software overhead. Once the PWM outputs are turned OFF, it is safe to process the fault in the fault loop as described in Section 3.2.4 “Fault Loop”.

Once the fault is detected, a software flag is set that indicates the source of the fault. The idle loop polls the state of the fault flag and calls the fault loop if the fault flag is set.

The fault flag is assigned a Fault ID to indicate the source of the last fault that occurred. A visual indication is also provided using LEDs on both the primary and secondary side of the SMPS AC/DC Reference Design.

The LED switches the same number of times as the Fault ID of the source that caused the fault. The source of the fault can be decoded using the values in Table 3-6 and Table 3-7.

<table>
<thead>
<tr>
<th>TABLE 3-6: FAULT SOURCE INDICATION ON PRIMARY SIDE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fault ID</td>
</tr>
<tr>
<td>----------</td>
</tr>
<tr>
<td>11</td>
</tr>
<tr>
<td>12</td>
</tr>
<tr>
<td>13</td>
</tr>
<tr>
<td>14</td>
</tr>
<tr>
<td>15</td>
</tr>
<tr>
<td>16</td>
</tr>
<tr>
<td>17</td>
</tr>
<tr>
<td>18</td>
</tr>
<tr>
<td>Fault ID</td>
</tr>
<tr>
<td>---------</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>5</td>
</tr>
<tr>
<td>6</td>
</tr>
<tr>
<td>7</td>
</tr>
<tr>
<td>8</td>
</tr>
</tbody>
</table>
Chapter 4. System Operation

This chapter describes the system setup and operating of the SMPS AC/DC Reference Design.

4.1 SYSTEM SETUP

4.1.1 Recommended Test Equipment

The following list of Test Equipment is recommended for complete evaluation of the SMPS AC/DC Reference Design and/or development of software.

- Oscilloscope
- High voltage probe (100:1 attenuation ratio)
- 10A AC Current Probe
- Power Quality Meter
- DC Electronic Load (350W or higher, and should have capability to load three outputs simultaneously)
- 0V-265V Variac or Programmable AC Source (500W or higher)
- 2 Digital multimeters

4.1.2 Functional Blocks of the System

Figure 4-1 shows a block diagram of the SMPS AC/DC Reference Design. Table 4-1 describes the inputs and outputs of the system and also displays the location of the isolation barrier. To assist in identifying each functional block on the SMPS AC/DC Reference Design, Figure 4-2 shows a top-view of the system with each block called out with dotted lines.

**FIGURE 4-1: SMPS AC/DC REFERENCE DESIGN BLOCK DIAGRAM**

- EMI Filter and Bridge Rectifier
- Rectified Sinusoidal Voltage
- 85-265 VAC 45-65 Hz
- PFC Boost Converter
- Phase Shift ZVT Converter
- ZVT Full-Bridge Converter
- Synchronous Rectifier
- Opto-Coupler
- dsPIC 30F2023
- Isolation Barrier
- 400 Vdc
- 12 Vdc
- Multi-Phase Buck Converter
- Single-Phase Buck Converter
- 3.3 Vdc 69A
- 5 Vdc 23A
4.1.3 Safety Isolation Information

The SMPS AC/DC Reference Design provides safety isolation to protect users and downstream electronics from the input AC Mains voltage. The location of the isolation boundary on the SMPS AC/DC Reference Design is displayed with a dotted line in Figure 4-3.

TABLE 4-1: INPUT AND OUTPUT ELECTRICAL SPECIFICATIONS

<table>
<thead>
<tr>
<th>Functional Block</th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>EMI Filter</td>
<td>85-265V AC, 45-65 Hz</td>
<td>85-265V AC, 45-65 Hz</td>
</tr>
<tr>
<td>Bridge Rectifier</td>
<td>85-265V AC, 45-65 Hz</td>
<td>120-374V DC (unregulated)</td>
</tr>
<tr>
<td>PFC Boost Converter</td>
<td>120-374V DC (unregulated)</td>
<td>400V DC</td>
</tr>
<tr>
<td>Full-Bridge Converter</td>
<td>400V DC</td>
<td>N/A</td>
</tr>
<tr>
<td>Synchronous Rectifier</td>
<td>N/A</td>
<td>12V DC</td>
</tr>
<tr>
<td>Multi-Phase Buck Converter</td>
<td>12V DC</td>
<td>3.3V DC</td>
</tr>
<tr>
<td>Single-Phase Buck Converter</td>
<td>12V DC</td>
<td>5V DC</td>
</tr>
</tbody>
</table>
Table 4-2 lists the location where each functional block resides with respect to the isolation barrier.

TABLE 4-2: LOCATION OF FUNCTIONAL BLOCK WITH RESPECT TO ISOLATION BARRIER

<table>
<thead>
<tr>
<th>Functional Block</th>
<th>Live or Isolated Side?</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Power Circuit</td>
</tr>
<tr>
<td>EMI Filter</td>
<td>Primary (Live)</td>
</tr>
<tr>
<td>Bridge Rectifier</td>
<td>Primary (Live)</td>
</tr>
<tr>
<td>PFC Boost Converter</td>
<td>Primary (Live)</td>
</tr>
<tr>
<td>Full-Bridge Converter</td>
<td>Primary (Live)</td>
</tr>
<tr>
<td>Synchronous Rectifier</td>
<td>Secondary (Isolated)</td>
</tr>
<tr>
<td>Multi-Phase Buck Converter</td>
<td>Secondary (Isolated)</td>
</tr>
<tr>
<td>Single-Phase Buck Converter</td>
<td>Secondary (Isolated)</td>
</tr>
</tbody>
</table>
4.1.4 System Connections

4.1.4.1 INPUT CONNECTIONS

The AC input connector (J) is shown in Figure 4-4. The SMPS AC/DC Reference Design has a transparent lid (not shown in pictures) with a 12V fan mounted on it. There are three holes provided in the lid to fasten the connection screws on the AC input connector (J).

Ensure that the power chord is not connected to the Variac or programmable AC source (or AC Mains). Connect the AC chord with terminal lugs to the AC input connector in the configuration shown in Figure 4-4.

FIGURE 4-4: SMPS AC/DC REFERENCE DESIGN INPUT CONNECTIONS

This is the minimum connection required to power up the SMPS AC/DC Reference Design. However, other connections are recommended for detailed testing and evaluation of the system.

4.1.4.2 OUTPUT CONNECTIONS

Ensure that the SMPS AC/DC Reference Design is not powered. Connect DC Electronic Loads (if available) to the 5V and 3.3V output terminals shown in Figure 4-5.

FIGURE 4-5: SMPS AC/DC REFERENCE DESIGN OUTPUT CONNECTIONS

A DC Electronic Load can be used to adjust the output power delivered by the SMPS AC/DC Reference Design. If a DC Electronic load is not available, a rheostat or resistors with sufficient power ratings may also be used for loading the SMPS AC/DC Reference Design.
4.1.4.3 PROGRAMMING CONNECTIONS

The SMPS AC/DC Reference Design comes pre-programmed with the control software and does not require a programmer to be connected to the system. However, ICSP headers are provided on the primary and secondary side for software development and testing.

Figure 4-6 shows the location of the primary side programming header (J2 on the control board).

FIGURE 4-6: PRIMARY SIDE PROGRAMMING HEADER

![Primary Side ICSP Header](image)

**CAUTION**

The primary side ICSP header (J2) is not isolated from the AC Mains. An isolated USB cable must be used to connect the programmer to the computer's USB port. Do not connect the programmer directly to the USB port of a computer.

Figure 4-7 shows the location of the secondary side programming header (J on the control board).

FIGURE 4-7: SECONDARY SIDE PROGRAMMING HEADER

![Secondary Side ICSP Header](image)

The software provided on the SMPS AC/DC Reference Design implements a ZVT voltage feedback failure fault. If a programmer is connected to the secondary side ICSP header while the system is running, the primary side controller generates a fault.

**CAUTION**

The ZVT voltage feedback failure fault must be enabled during software development. Refer to Chapter 3. “Software Design” and the source code provided with the SMPS AC/DC Reference Design.
4.2 SYSTEM OPERATION

4.2.1 System Power-Up

Once the input and output connections as described in Section 4.1.4 “System Connections” are completed, the mains voltage can be applied to the SMPS AC/DC Reference Design.

There are three power-ON indicator LEDs on the system. One LED (D__) on the power board near the AC input terminals and two more on the control board (one on the primary side (D___), and one on the secondary side (D__)).

There will be a short delay before the 12V, 5V and 3.3V outputs are ON because of the soft-start routines and output sequencing scheme implemented on each stage each stage of the SMPS AC/DC Reference Design. Details of the soft-start routine and output sequencing are provided in Chapter 3. “Software Design”.

As soon as the 12V output is ON, the cooling fan mounted on the lid will start running. LEDs are provided near each output terminal to indicate that the output is ON.

There are four more LEDs on the control board used for indicating which control loop is being executed at any given time. Due to the high speed of execution, these LEDs appear continuously ON with the naked eye.

Faults are indicated on the control board with two LEDs (one on the primary side (D__) and one on the secondary side (D__)). Details of faults are provided in Chapter 3. “Software Design”.

4.2.2 System Evaluation and Testing

4.2.2.1 INPUT PERFORMANCE TESTING

The input specifications of the SMPS AC/DC Reference Design can be tested by using a power meter. The voltage is measured directly across the Live and Neutral terminals on the SMPS AC/DC Reference Design. The input current is measured by sensing the current through either the Live or Neutral line. Figure 4-8 shows two separate power meter connections depending on the type of power meter used.
A power meter is capable of measuring the input Power Factor of the SMPS AC/DC Reference Design and also the Total Harmonic Distortion (THD) on the current drawn by the system.

Using a programmable AC source will enable the user to evaluate the system performance over the entire range of input voltage (85V - 265V, 45Hz - 65Hz).

4.2.2.2 OUTPUT PERFORMANCE TESTING

The SMPS AC/DC Reference Design can be loaded using DC Electronic Loads. A number of output parameters can be tested by connecting oscilloscope probes to the output terminals. Some of the parameters that can be tested are:

- Output Ripple Voltage
- Load Regulation
- Transient Response
- Step-Load Response
- Fault Shutdown Delay
Appendix A. Board Layouts and Schematics

A.1 INTRODUCTION

This appendix contains the schematics and layouts for the SMPS AC/DC Reference Design. Diagrams included in this appendix:

- SMPS AC/DC Reference Design Layout
- SMPS AC/DC Reference Design Schematics

A.2 SMPS AC/DC REFERENCE DESIGN LAYOUT

FIGURE A-1: SMPS AC/DC REFERENCE DESIGN LAYOUT (POWER BOARD)
A.3 SMPS AC/DC REFERENCE DESIGN SCHEMATICS

FIGURE A-3: SMPS AC/DC REFERENCE DESIGN POWER BOARD SCHEMATIC (SHEET 1 OF 8)
Connect Resistor and Transformer Directly to Source and then connect to -HV_BUS.

Fire signals are on Page 8.
FIGURE A-8: SMPS AC/DC REFERENCE DESIGN POWER BOARD SCHEMATIC (SHEET 6 OF 8)
FIGURE A-10: SMPS AC/DC REFERENCE DESIGN POWER BOARD SCHEMATIC (SHEET 8 OF 8)
FIGURE A-11: SMPS AC/DC REFERENCE DESIGN SIGNAL BOARD SCHEMATIC (SHEET 1 OF 7)
FIGURE A-12: SMPS AC/DC REFERENCE DESIGN SIGNAL BOARD SCHEMATIC (SHEET 2 OF 7)

Live

Isolated

U21 is to shut down AC side from DC side fault.
Assuming 10mOhm shunt for PFC. Ans 9A peak
Therefore a gain of 26.8 for 2.5V

ZVT CT output will be about 0.466V for a nominal max current. Therefore a gain of 5.35 is about correct.
FIGURE A-15: SMPS AC/DC REFERENCE DESIGN SIGNAL BOARD SCHEMATIC (SHEET 5 OF 7)
When using the Maxim part:

- Remove R100, R105, R65, R60
- Replace 0R at the following locations:
  - R101, R102, R103, R104, R61, R62, R63, R64

Probably use 2 or 3 mV per turns. So need a gain of about 850.
FIGURE A-17: SMPS AC/DC REFERENCE DESIGN SIGNAL BOARD SCHEMATIC (SHEET 7 OF 7)
Appendix B. Source Code

Any libraries and source files associated with SMPS AC/DC Reference Design are available by request from your local Microchip sales office. See the Microchip Web site, or the last page of this document for contact information.
NOTES:
Appendix C. References

This section provides the list of references used throughout this document.


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