OS81210
Intelligent Network Interface Controller for 50 Mbit/s
Automotive Networks Product Brief

Features
• Complete 50 Mbit/s synchronous network interface
• Embedded network management functions
  - Network protection mode
  - Hardware & application watchdog timer
  - Intelligent muting
  - Diagnostics
  - Emergency Response System (eCall)
• IEEE MAC addressing and Ethernet channel
• Universal Serial Bus (USB) Port supports USB 2.0
  High-speed upstream data transfers using either:
  - USB 2.0 physical layer
  - High-Speed Inter-Chip (HSIC) physical layer
• Media Local Bus (MediaLB®) Port
  - Eases inter-chip communication and streaming
  - MediaLB 3-pin interface at speeds up to 1024xFs
• I²C™ Control Port inter-chip message exchange
• Streaming Port supports synchronous, fixed latency data exchange for a variety of serial audio formats including time-division multiplex (TDM) and pulse density modulation (PDM)
• SPI Port supports asynchronous and control packets
• General Purpose I/O (GPIO) Port
• Remote control and configuration for operation without a local External Host Controller.
  - I²C (master) message tunneling
  - GPIO port control
• Operating voltages 3.3 V/1.8 V (and 1.2 V for HSIC)
• Available in 64-pin QFN package with exposed pad
• -40 to +125 °C junction temperature

Applications
• Automotive infotainment network nodes including head unit, instrument cluster, amplifier, and rear seat entertainment.

General Description
The OS81210 is a highly integrated Intelligent Network Interface Controller (INIC) for 50 Mbit/s INICnet-based automotive networks with a transformer-less balanced media physical layer (bPHY) optimized for unshielded twisted pair (UTP) copper wire.

The INIC provides encapsulation of all low-level functions necessary to develop a network-compliant device, significantly simplifying network implementation in a node. Integration of the INIC Software Stack into the INIC provides network-compliant real-time behavior. The INIC Software Stack significantly relieves the External Host Controller (EHC) from real-time processing tasks. Supervision of the application is also provided, including a protection mode that is entered when an application is not present (i.e. start-up) or the EHC malfunctions. This protection mode prevents application malfunctions from influencing the integrity of the network and the system.

When the EHC is engaged, a message-based interface, as opposed to a register-based interface, is available for communication with INIC. A unified and centralized network management software stack (UNICENS) is available for the EHC to build a complete, lean, system solution.

The INIC can also support a fully compliant MOST® network.

Conformity
• This document applies to hardware revision B1A

FIGURE: OS81210 BLOCK DIAGRAM
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To determine if an errata sheet exists for a particular device, please check with one of the following:

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• Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

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# 1.0 PINOUT

## FIGURE 1-1: OS81210 PIN DIAGRAM

![OS81210 Pin Diagram](image)

## TABLE 1-1: OS81210 PIN ALLOCATION TABLE

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>HW Port</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MLBCLK</td>
<td>MediaLB</td>
<td>Singled-ended Clock line for MediaLB 3-pin Interface</td>
</tr>
<tr>
<td>2</td>
<td>MLBSIG</td>
<td>MediaLB</td>
<td>Singled-ended Signal line for MediaLB 3-pin Interface</td>
</tr>
<tr>
<td>3</td>
<td>MLBDAT</td>
<td>MediaLB</td>
<td>Singled-ended Data line for MediaLB 3-pin Interface</td>
</tr>
<tr>
<td>4</td>
<td>VDDP1</td>
<td></td>
<td>3.3 V periphery power supply (digital)</td>
</tr>
<tr>
<td>5</td>
<td>SDIN</td>
<td>SPI</td>
<td>Data In (MOSI - Master Out, Slave In)</td>
</tr>
<tr>
<td></td>
<td>GP3</td>
<td>GPIO</td>
<td>General Input/Output 3</td>
</tr>
<tr>
<td>6</td>
<td>SDOUT</td>
<td>SPI</td>
<td>Data Out (MISO - Master In, Slave Out)</td>
</tr>
<tr>
<td></td>
<td>GP4</td>
<td>GPIO</td>
<td>General Purpose Input/Output 4</td>
</tr>
<tr>
<td>7</td>
<td>SCLK</td>
<td>SPI</td>
<td>Clock</td>
</tr>
<tr>
<td></td>
<td>GP5</td>
<td>GPIO</td>
<td>General Purpose Input/Output 5</td>
</tr>
<tr>
<td>8</td>
<td>SINT</td>
<td>SPI</td>
<td>Interrupt (active low)</td>
</tr>
<tr>
<td></td>
<td>GP6</td>
<td>GPIO</td>
<td>General Purpose Input/Output 6</td>
</tr>
<tr>
<td>9</td>
<td>CS</td>
<td>SPI</td>
<td>Chip Select (active low)</td>
</tr>
<tr>
<td></td>
<td>GP7</td>
<td>GPIO</td>
<td>General Purpose Input/Output 7</td>
</tr>
<tr>
<td>10</td>
<td>VDDC1</td>
<td></td>
<td>1.8 V core power supply (digital)</td>
</tr>
<tr>
<td>11</td>
<td>TMS</td>
<td>JTAG</td>
<td>Test Mode Select</td>
</tr>
</tbody>
</table>

**Note 1:** Pull-up resistor required.

**Note 2:** Pull-down resistor required.
### TABLE 1-1: OS81210 PIN ALLOCATION TABLE (CONTINUED)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>HW Port</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>TDO 1</td>
<td>JTAG</td>
<td>Test Data Output</td>
</tr>
<tr>
<td></td>
<td>DINT 1</td>
<td></td>
<td>Debug Interrupt (active low)</td>
</tr>
<tr>
<td>13</td>
<td>TDI 1</td>
<td>JTAG</td>
<td>Test Data Input</td>
</tr>
<tr>
<td></td>
<td>DSDA 1</td>
<td></td>
<td>Debug Data</td>
</tr>
<tr>
<td>14</td>
<td>TCK 1</td>
<td>JTAG</td>
<td>Test Clock Input</td>
</tr>
<tr>
<td></td>
<td>DSCL 1</td>
<td></td>
<td>Debug Clock</td>
</tr>
<tr>
<td>15</td>
<td>RST</td>
<td></td>
<td>Hardware Reset Input (active low). (Pull-up resistor to VDDPn supply should be used when not driven high by an external device. A series resistor should be used in lieu of the pull-up when always driven by an external device.)</td>
</tr>
<tr>
<td>16</td>
<td>GP10</td>
<td>GPIO</td>
<td>General Purpose Input/Output 10</td>
</tr>
<tr>
<td>17</td>
<td>GP13</td>
<td>GPIO</td>
<td>General Purpose Input/Output 13</td>
</tr>
<tr>
<td>18</td>
<td>PWROFF 1</td>
<td></td>
<td>External Power Management Power-Down Indicator. This pin is driven low by INIC after initialization. When high, indicates the INIC Processor is ready to be shut down. A pull-up resistor is required when used. If not used, this pin may be left unconnected.</td>
</tr>
<tr>
<td>19</td>
<td>MUTE 1</td>
<td>GPIO</td>
<td>Mute Indicator Output. A pull-up resistor is required when used. If not used, this pin may be left unconnected.</td>
</tr>
<tr>
<td></td>
<td>GP8</td>
<td>GPIO</td>
<td>General Purpose Input/Output 8</td>
</tr>
<tr>
<td>20</td>
<td>ERR</td>
<td>Network</td>
<td>Network Error Indicator Output. This pin is driven high when the network is unlocked. When low, this pin indicates the INIC is locked to the network.</td>
</tr>
<tr>
<td></td>
<td>BOOT 1</td>
<td></td>
<td>Configuration Pin. This pin is attached to the configuration/debug header and used by the Microchip INICkit Tool to load initial configuration data into INIC. May also be connected to the EHC to allow in-system configuration of the INIC.</td>
</tr>
<tr>
<td>21</td>
<td>VDDC2</td>
<td></td>
<td>1.8 V core power supply (digital)</td>
</tr>
<tr>
<td>22</td>
<td>VDDP2</td>
<td></td>
<td>3.3 V periphery power supply (digital)</td>
</tr>
<tr>
<td>23</td>
<td>BTXP</td>
<td>Network</td>
<td>Positive (differential) bPHY network transmitter output</td>
</tr>
<tr>
<td>24</td>
<td>BTXN</td>
<td>Network</td>
<td>Negative (differential) bPHY network transmitter output</td>
</tr>
<tr>
<td>25</td>
<td>VDDAU1</td>
<td></td>
<td>3.3 V continuous power supply (analog)</td>
</tr>
<tr>
<td>26</td>
<td>VDDE18</td>
<td></td>
<td>1.8 V bPHY power supply (analog)</td>
</tr>
<tr>
<td>27</td>
<td>VDDE33</td>
<td></td>
<td>3.3 V bPHY power supply (analog)</td>
</tr>
<tr>
<td>28</td>
<td>BRST</td>
<td>Network</td>
<td>Hardware Reset Input (active low) for the Balanced Media Physical Layer. When asserted, the transmitter output is disabled.</td>
</tr>
<tr>
<td>29</td>
<td>BRXN</td>
<td>Network</td>
<td>Negative (differential) bPHY network receiver input</td>
</tr>
<tr>
<td>30</td>
<td>BRXP</td>
<td>Network</td>
<td>Positive (differential) bPHY network receiver input</td>
</tr>
<tr>
<td>31</td>
<td>NC</td>
<td></td>
<td>No Connect. This pin must be left open and floating.</td>
</tr>
<tr>
<td>32</td>
<td>VDDAU2</td>
<td></td>
<td>3.3 V continuous power supply (analog)</td>
</tr>
<tr>
<td>33</td>
<td>VDDA33</td>
<td></td>
<td>3.3 V power supply (analog)</td>
</tr>
<tr>
<td>34</td>
<td>VDDA18</td>
<td></td>
<td>1.8 V power supply (analog)</td>
</tr>
<tr>
<td>35</td>
<td>BSTATUS</td>
<td>Network</td>
<td>bPHY Network Activity Status Output:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Driven low when a valid signal is detected</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Driven high to VDDAUin when a qualified signal is not present</td>
</tr>
<tr>
<td>36</td>
<td>XTO</td>
<td></td>
<td>Crystal Oscillator Output</td>
</tr>
<tr>
<td>37</td>
<td>XTI</td>
<td></td>
<td>Crystal Oscillator Input or External CMOS Clock Input</td>
</tr>
<tr>
<td>38</td>
<td>PS0</td>
<td></td>
<td>External Power Management Status Bit 0</td>
</tr>
<tr>
<td></td>
<td>GP1</td>
<td>GPIO</td>
<td>General Purpose Input/Output 1</td>
</tr>
</tbody>
</table>

**Note 1:** Pull-up resistor required.  
**Note 2:** Pull-down resistor required.
### TABLE 1-1: OS81210 PIN ALLOCATION TABLE (CONTINUED)

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<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>HW Port</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>39</td>
<td>PS1</td>
<td></td>
<td>External Power Management Status Bit 1</td>
</tr>
<tr>
<td></td>
<td>GP2</td>
<td>GPIO</td>
<td>General Purpose Input/Output 2</td>
</tr>
<tr>
<td>40</td>
<td>GP12</td>
<td>GPIO</td>
<td>General Purpose Input/Output 12</td>
</tr>
<tr>
<td>41</td>
<td>GP14</td>
<td>GPIO</td>
<td>General Purpose Input/Output 14</td>
</tr>
<tr>
<td>42</td>
<td>VDDC3</td>
<td></td>
<td>1.8 V core power supply (digital)</td>
</tr>
<tr>
<td>43</td>
<td>VDDP3</td>
<td></td>
<td>3.3 V periphery power supply (digital)</td>
</tr>
<tr>
<td>44</td>
<td>STROBE</td>
<td>USB</td>
<td>Strobe line for HSIC physical interface. Connect to GND when HSIC is not used.</td>
</tr>
<tr>
<td>45</td>
<td>DATA</td>
<td>USB</td>
<td>Data line for HSIC physical interface. Connect to GND when HSIC is not used.</td>
</tr>
<tr>
<td>46</td>
<td>VDD12</td>
<td></td>
<td>1.2 V power supply for HSIC physical interface transceiver. Connect to GND through a 1 kΩ resistor when HSIC is not used.</td>
</tr>
<tr>
<td>47</td>
<td>DM</td>
<td>USB</td>
<td>Negative (differential) data line for USB physical interface. Connect to GND when the USB physical interface is not used.</td>
</tr>
<tr>
<td>48</td>
<td>DP</td>
<td>USB</td>
<td>Positive (differential) data line for USB physical interface. Connect to GND when the USB physical interface is not used.</td>
</tr>
<tr>
<td>49</td>
<td>VDDUSB33</td>
<td></td>
<td>3.3 V USB power supply (analog)</td>
</tr>
<tr>
<td>50</td>
<td>RBIAS ²</td>
<td>USB</td>
<td>Connect to GND through a 12 kΩ resistor (0.5 %, 1/16 W, ≤ ± 100 ppm). This pin may be left unconnected when both the USB and HSIC physical interfaces are not used.</td>
</tr>
<tr>
<td>51</td>
<td>VDDUSB18</td>
<td></td>
<td>1.8 V USB power supply (analog)</td>
</tr>
<tr>
<td>52</td>
<td>VBUS</td>
<td>USB</td>
<td>USB Bus Power State Indicator Input. The application should drive this pin high when an external USB Host Controller is present. Note that this pin is not 5 V tolerant and must not be connected directly to USB bus power. This signal is ignored when using the HSIC physical interface. Connect to GND when the USB physical interface is not used.</td>
</tr>
<tr>
<td>53</td>
<td>RMCK</td>
<td>RMCK</td>
<td>Recovered Master Clock Output</td>
</tr>
<tr>
<td>54</td>
<td>INT ¹</td>
<td>I²C</td>
<td>Interrupt (active low). Indicates a service request from the EHC when the Control Port is operating as an I²C slave.</td>
</tr>
<tr>
<td></td>
<td>GP0</td>
<td>GPIO</td>
<td>General Purpose Input/Output 0</td>
</tr>
<tr>
<td>55</td>
<td>SCL ¹</td>
<td>I²C</td>
<td>Clock</td>
</tr>
<tr>
<td>56</td>
<td>SDA ¹</td>
<td>I²C</td>
<td>Data</td>
</tr>
<tr>
<td>57</td>
<td>VDDC4</td>
<td></td>
<td>1.8 V core power supply (digital)</td>
</tr>
<tr>
<td>58</td>
<td>VDDP4</td>
<td></td>
<td>3.3 V periphery power supply (digital)</td>
</tr>
<tr>
<td>59</td>
<td>FSYA</td>
<td>Streaming</td>
<td>Frame Sync for Streaming Port A and B</td>
</tr>
<tr>
<td>60</td>
<td>SCKA</td>
<td>Streaming</td>
<td>Bit Clock for Streaming Port A and B</td>
</tr>
<tr>
<td>61</td>
<td>SRXA0</td>
<td>Streaming</td>
<td>Data I/O Signal 0 for Streaming Port A</td>
</tr>
<tr>
<td>62</td>
<td>SRXA1</td>
<td>Streaming</td>
<td>Data I/O Signal 1 for Streaming Port A</td>
</tr>
<tr>
<td>63</td>
<td>SRXB0</td>
<td>Streaming</td>
<td>Data I/O Signal 0 for Streaming Port B</td>
</tr>
<tr>
<td>64</td>
<td>SRXB1</td>
<td>Streaming</td>
<td>Data I/O Signal 1 for Streaming Port B</td>
</tr>
<tr>
<td>ePAD</td>
<td>GND</td>
<td></td>
<td>The exposed paddle on the bottom side of the QFN package is the primary ground for the OS81210 and must be connected to ground on the PCB for proper operation.</td>
</tr>
</tbody>
</table>

**Note 1:** Pull-up resistor required.  
**Note 2:** Pull-down resistor required.
2.0 BASIC APPLICATION INFORMATION

The OS81210 and OS81212/4/6 INICs are part of the OS8121x 50 Mbit/s INICnet product family that support point-to-point, simplex daisy chain, and ring topologies through an integrated balanced media physical layer (bPHY). The integrated INIC Software Stack can independently run the network and manage the low-level protocols such as startup, shutdown, error reporting, or Plug-and-Play node positioning. Alternatively, INIC can operate in conjunction with an External Host Controller (EHC) managing the mid- and high-level functions. Additionally the OS81210 provides power management capabilities and industry standard application interfaces such as a USB 2.0, MediaLB 3-Pin, Streaming Port, \( \text{I}^2\text{C} \) Port, SPI port, and GPIOs.

The OS81210 is optimized for high performance head unit applications with USB 2.0 or HSIC high-speed communication.

The OS81212 is targeted for audio / video streaming data applications with the dual Streaming Ports and MediaLB interface. It can operate with an EHC or it can exist remotely on the network.

The OS81214 is targeted for audio data applications using the Streaming Port or packets over the SPI Port. It can operate with an EHC or it can exist remotely on the network.

The OS81216 INIC is targeted for remotely configured microphone applications (without a local EHC).

FIGURE 2-1: OS8121x PRODUCT FAMILY OVERVIEW
Figure 2-2 depicts an example 50 Mbit/s INICnet application. Using a combination of OS81210 and OS81212/4/6 INICs, a system supporting audio, video, and packet data applications can be easily configured. The Head Unit INIC can communicate with an operating system (such as a GNU/Linux, QNX, Android Auto, etc.) to manage the network and control the remote nodes. The asynchronous channel on the INIC can be used for high-speed routing of application packet data such as graphics images, system information, or software downloads. The EHC can access both synchronous and packet data through the OS81210 USB interface. An Instrument Panel can be implemented with control and Ethernet packets sent over the OS81210/2 MediaLB Port. Without a local EHC, the microphones are configured remotely over I2C. Only a single INIC streaming pin is used to source a mono PDM bit stream from a MEMS microphone to the network. As shown in the Remote Amp, the amplifier is remotely controlled and configured. Synchronous audio data is routed over the network and is sourced/sinked through I2S to CODECs or DSPs. The Rear Seat Entertainment (RSE) can route synchronous streams or asynchronous data such as IP packets over the network Ethernet Channel.

**FIGURE 2-2: BASIC APPLICATION DIAGRAM**
3.0 PACKAGING INFORMATION

3.1 Package Marking

FIGURE 3-1: OS81210 TOP MARKING

The package designators are:
- xx - Device Identifier
- OS81210AF - Solderable Flank QFN
- rrr - Product Revision Code
- yy - last two digits of Assembly Year
- ww - Assembly Work Week
- nnn - Tracking Number
- cc - Country of Origin Abbreviation (optional - up to 2 characters)
- e³ - Pb Free Symbol
# PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>X</th>
<th>Package Type</th>
<th>Tape and Reel Flag</th>
<th>Device Revision Code</th>
<th>Firmware Revision Code</th>
<th>Firmware Service Release (optional)</th>
<th>Special Feature Code (optional)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
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<td>Grade</td>
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<td></td>
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<td></td>
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<td></td>
</tr>
</tbody>
</table>

Device OS81210 = 50 Mbit/s Automotive Intelligent Network Interface Controller with USB

Grade A = All Features

Package Type F = QFN with solderable flanks

Tape and Reel Flag (optional)

Product Revision Code mrr = 3 character code specifying product revision

Firmware Revision Code vvvvvv = 6 character code specifying firmware revision

Firmware Service Release (optional) ss = 2 character code specifying service release

Special Feature Code (optional) xxx = 3 character code for special requirements

Examples:

a) OS81210AF-rrr-vvvvvv-xxx
   64-pin solderable flank QFN package

b) OS81210AFR-rrr-vvvvvv-xxx
   64-pin solderable flank QFN package, Tape and Reel
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- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip’s Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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