Section 38. High/Low-Voltage Detect (HLVD)

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38.1 INTRODUCTION

The High/Low-Voltage Detect (HLVD) module is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

The HLVD module provides the following features:

- Detection of hysteresis
- Detection of low-to-high or high-to-low voltage changes
- Generation of Non-Maskable Interrupts (NMI)
- LVDIN pin to provide external voltage trip point

Figure 38-1 provides a typical block diagram of the HLVD module.

Figure 38-1: High/Low-Voltage Detect (HLVD) Module Block Diagram
### 38.2 CONTROL REGISTERS

HLVD operations are controlled using the following Special Function Register (SFR):

- **HLVDCON: High/Low-Voltage Detect Control Register**

  This register is used to enable the HLVD module and control the trip points and direction of event along with flag control.

Table 38-1 summarizes the related HLVD register. A corresponding register table appears after the summary, which includes a detailed description of the register.

Table 38-1: High/Low-Voltage Detect Register Map

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Bit Range</th>
<th>Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>HLVDCON</td>
<td>31:16</td>
<td></td>
</tr>
<tr>
<td></td>
<td>15:0</td>
<td>ON</td>
</tr>
<tr>
<td></td>
<td>31/15</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>30/14</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>29/13</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>28/12</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>27/11</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>26/10</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>25/9</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>24/8</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>23/7</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>22/6</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>21/5</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>20/4</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>19/3</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>18/2</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>17/1</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>16/0</td>
<td>—</td>
</tr>
</tbody>
</table>
Register 38-1: HLVDCON: High/Low-Voltage Detect Control Register

<table>
<thead>
<tr>
<th>Bit Range</th>
<th>Bit 31:24</th>
<th>Bit 23:16</th>
<th>Bit 15:8</th>
<th>Bit 7:0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>31/23/15/7</td>
<td>30/22/14/6</td>
<td>29/21/13/5</td>
<td>28/20/12/4</td>
</tr>
<tr>
<td></td>
<td>27/19/11/3</td>
<td>26/18/10/2</td>
<td>25/17/9/1</td>
<td>24/16/8/0</td>
</tr>
<tr>
<td>31:24</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>30:22/14/6</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>29/21/13/5</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>28/20/12/4</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>27/19/11/3</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>26/18/10/2</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>25/17/9/1</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
<tr>
<td>24/16/8/0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
<td>U-0</td>
</tr>
</tbody>
</table>

Legend:
- HS = Hardware Set
- HC = Hardware Cleared
- r = Reserved bit
- R = Readable bit
- W = Writable bit
- U = Unimplemented bit, read as ‘0’
- -n = Value at POR
- ‘1’ = Bit is set
- ‘0’ = Bit is cleared
- x = Bit is unknown

bit 31-16 **Unimplemented**: Read as ‘0’

bit 15 **ON**: LVD Module Enable bit
1 = LVD module is enabled
0 = LVD module is disabled

bit 14 **Unimplemented**: Read as ‘0’

bit 13 **SIDL**: Stop in Idle Mode bit
1 = Discontinue operation of LVD when device enters Idle mode
0 = Continue operation of LVD in Idle mode

bit 12 **Unimplemented**: Read as ‘0’

bit 11 **VDIR**: Voltage Change Direction Select bit
1 = Event occurs when voltage equals or exceeds the trip point (HLVDL<3:0>)
0 = Event occurs when voltage equals or falls below the trip point (HLVDL<3:0>)

bit 10 **BGVST**: Band Gap Reference Voltages Stable Status bit
1 = Indicates internal band gap voltage references is stable
0 = Indicates internal band gap voltage reference is not stable
This bit is readable when the HLVD module is disabled (ON = 0).

bit 9 **Reserved**: Read as ‘1’

bit 8 **HLEVT**: Low-Voltage Detection Event Status bit
1 = Indicates LVD Event interrupt is active
0 = Indicates LVD Event interrupt is not active

bit 7 **HLEVOUTEN**: High/Low-Voltage Detection Event Output bit
1 = Enables HLVD Event output
0 = Disable HLVD Event output

**Note**: Once this bit is set to ‘1’, it can only be cleared by disabling/enabling the HLVD module through the ON (HLVD<15>) bit or through the HLVDMD bit.

bit 6-4 **Unimplemented**: Read as ‘0’

**Note 1**: To avoid false LVD events, all LVD module setting changes should occur only when the module is disabled (ON = 0). See the “Electrical Characteristics” chapter of the specific device data sheet for the actual trip points.
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Register 38-1:  HLVDCON: High/Low-Voltage Detect Control Register  

bit 3-0  HLVDL<3:0>: Low-Voltage Detection Limit Select bits(1)  

- 1111 = Selects analog input on LVDIN  
- 1110 = Selects trip point 14  
- 1101 = Selects trip point 13  
- 1100 = Selects trip point 12  
- 1011 = Selects trip point 11  
- 1010 = Selects trip point 10  
- 1001 = Selects trip point 9  
- 1000 = Selects trip point 8  
- 0111 = Selects trip point 7  
- 0110 = Selects trip point 6  
- 0101 = Selects trip point 5  
- 0100 = Selects trip point 4  
- 0011 = Selects trip point 3  
- 0010 = Selects trip point 2  
- 0001 = Selects trip point 1  
- 0000 = Selects trip point 0  

Note 1:  To avoid false LVD events, all LVD module setting changes should occur only when the module is disabled (ON = 0). See the “Electrical Characteristics” chapter of the specific device data sheet for the actual trip points.
38.3  OPERATION

Certain PIC32 family devices have a programmable High/Low-Voltage Detection circuit (HLVD). The circuitry can be programmed to generate an interrupt on crossing the range of the VDD level in the selected direction.

When the HLVD module is enabled, a comparator uses an internally generated reference voltage as the set point. The set point is compared with the trip point, where each node in the resistor divider represents a trip point voltage. The “trip point” voltage is the voltage level at which the device detects a high or low-voltage event, depending on the configuration of the module. When the supply voltage is equal to the trip point, the voltage tapped off of the resistor array is equal to the internal reference voltage generated by the voltage reference module. The comparator then generates an interrupt signal. Refer to the “Interrupts” chapter in the specific device data sheet for more information on the generated interrupt.

The trip point voltage is software programmable and is selected by programming the HLVDL<3:0> bits (HLVDCON<3:0>).

The HLVD module has an additional feature that allows the user to supply the trip voltage to the module from an external source. This mode is enabled when bits, HLVDL<3:0>, are set to ‘1111’. In this state, the comparator input is multiplexed from the external input pin, LVDIN. This gives users flexibility because it allows them to configure the HLVD interrupt to occur at any voltage in the valid operating range.

38.3.1  HLVD Setup

To set up the HLVD module, follow these steps:

1. Ensure the HLVD module is disabled (ON = 0).
2. Write the value to the HLVDL<3:0> bits that selects the desired HLVD trip point.
3. Set the VDIR bit to detect high voltage (VDIR = 1) or low voltage (VDIR = 0). Refer to Figure 38-2 and Figure 38-2 for examples.
4. Enable the HLVD module by setting the ON bit.
5. Clear the HLVD Interrupt Flag in the Interrupt Controller, which may have been set from a previous interrupt. Refer to the “Interrupts” chapter in the specific device data sheet for HLVD interrupt-related information.
6. Enable the HLVD interrupt if interrupts are desired. An interrupt will not be generated until the BGVST bit (HLVDCON<10>) is set.
7. Set the HLEVTOUTEN bit (HLVDCON<7>) to ‘1’.

Figure 38-2:  High/Low-Voltage Detect Operation (VDIR = 0)

![Figure 38-2: High/Low-Voltage Detect Operation (VDIR = 0)](image)

Note 1: The hardware sets the HLVD interrupt flag back to ‘1’ if the condition is still true.
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Figure 38-3: High/Low-Voltage Detect Operation (VDIR = 1)

Note 1: The hardware sets the HLVD interrupt flag back to ‘1’ if the condition is still true.
38.4 APPLICATIONS

In many applications, the ability to detect a drop below or rise above a particular threshold is desirable. As an example, for general battery applications, Figure 38-4 displays a possible voltage curve. Over time, the device voltage decreases. When the device voltage reaches voltage, $V_A$, the HLVD logic generates an interrupt at time, $T_A$. The interrupt could cause the execution of an Interrupt Service Routine (ISR), which would allow the application to perform “housekeeping tasks” and perform a controlled shutdown before the device voltage exits the valid operating range at $T_B$. The HLVD, thus, would give the application a time window represented by the difference between $T_A$ and $T_B$ to safely exit.

Figure 38-4: Typical Low-Voltage Detect Application

Legend:
- $V_A$ = HLVD trip point
- $V_B$ = Minimum valid device operating voltage
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38.5 OPERATION IN POWER-SAVING MODES

38.5.1 Sleep Mode
When enabled, the HLVD circuitry continues to operate during Sleep mode. If the device voltage crosses the trip point, the HLVD interrupt flag will be set and the device will wake-up from Sleep mode. Device execution will continue from the interrupt vector address if interrupts have been globally enabled.

38.5.2 Idle Mode
When the device enters Idle mode, the HLVD clock source remain functional and the CPU is halted (stops executing code). The SIDL bit (HLVDCON<13>) selects whether the HLVD module stops operation or continues normal operation when the device enters Idle mode.

- If SIDL = 1, the module stops operation in Idle mode. The module performs the same procedures when stopped in Idle mode (SIDL = 1) as it does for Sleep mode.
- If SIDL = 0, the module continues operation in Idle mode.

38.5.3 Debug Mode
The behavior of the HLVD module is unaltered in Debug mode.

38.6 EFFECTS OF VARIOUS RESETS

38.6.1 Device Reset (MCLR)
A Device Reset forces all registers to their Reset state. This forces the HLVD module to be turned off.

38.6.2 Power-on Reset
The HLVD module is forced to its reset states when a Power-on Reset occurs. This forces the HLVD module to be turned off.

38.6.3 Watchdog Timer Reset
During a Watchdog Timer Reset, the HLVD module behaves as if a Device Reset has occurred and performs the same reset actions that are described in 38.6.1 “Device Reset (MCLR)”.
## 38.7 RELATED APPLICATION NOTES

This section lists application notes that are related to the HLVD module. These application notes may not be written specifically for the PIC32 device family, but the concepts are pertinent and could be used with modification and possible limitations. The current application notes related to High/Low-Voltage Detect (HLVD) include the following:

<table>
<thead>
<tr>
<th>Title</th>
<th>Application Note #</th>
</tr>
</thead>
<tbody>
<tr>
<td>No related application notes at this time.</td>
<td>N/A</td>
</tr>
</tbody>
</table>

**Note:** Please visit the Microchip web site ([www.microchip.com](http://www.microchip.com)) for additional application notes and code examples for the PIC32 family of devices.
38.8 REVISION HISTORY

Revision A (January 2017)
This is the initial released version of this document.
Note the following details of the code protection feature on Microchip devices:

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