PIC32WK2057GPX

32-bit MCU with Integrated Wi-Fi® Transceiver

MCU Features

- Operating frequency up to 120 MHz
- MIPS32® M14K 32-bit core with 5-stage execution pipeline
- MicroMIPS™ mode for reduced code size
- Multiple interrupt vectors with individually programmable priority
- Up to five external interrupt pins
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Peripheral Trigger Generator (PTG), programmable sequencer that synchronizes or triggers peripherals without utilizing the CPU
- Configurable Watchdog Timer (WDT) with on-Chip, Low-Power RC (LPRC) oscillator for reliable operation
  - Selectable windowed WDT feature

Memory

- 512 Kbytes static random-access memory (SRAM) for program code and data with additional 64 Kbytes data buffer
- 8 Kbytes one-time-programmable (OTP) non-volatile secure-boot and configuration memory
- Supports 2 Mbyte in-package SPI Flash for program code and data

Networking

- Integrated 802.11a/b/g/n MAC/Baseband/Radio Transceiver
- Requires external front end module (FEM) to meet the Tx power (2.4 GHz and 5 GHz) and Rx sensitivity (5 GHz) specifications
- Supports 20 MHz and 40 MHz channel bandwidth that provides physical (PHY) layer data rates up to MCS7
- AES-based CCMP and Temporal Key Integrity Protocol (TKIP) hardware for faster data encryption and 802.11i compatibility
- Supports Wi-Fi Protected Access (WPA™) and Wi-Fi Protected Access II (WPA2™) for powerful encryption and authentication
- Supports Concurrent mode of operation
- Supports Wi-Fi Protected Setup™ (WPS) and Wi-Fi Direct® (planned)
- Supports 802.11v-based timing synchronization
- Supports up to 150 Mbps PHY data rate
- Supports Wi-Fi and Bluetooth® coexistence over 3-wire Packet Traffic Arbitration (PTA)

Clock Management

- Supports the following system clock sources:
  - 40 MHz external Primary Crystal Oscillator (POSC)
  - 8 MHz Fast RC (FRC) oscillator
  - 32 kHz LPRC
  - 32.768 kHz external Secondary Crystal Oscillator (SOSC)
  - 96 MHz USB Phase-Locked Loop (PLL)
  - 10 MHz to120 MHz System PLL (SPLL)
- 26 MHz PLL for Bluetooth support
- Fail-Safe Clock Monitor (FSCM) mode
- Supports four reference clock outputs

Operating Conditions

- 1.2V (core), 2.5V (RF supply), 2V (RF ADC), 1.2V (RF supply) and 3.3V (analog and digital I/O)
- Operating temperature: -40ºC to +85ºC

Direct Memory Access (DMA)

- 8-channel hardware DMA controller with automatic data size detection:
  - Up to 64 Kbytes transfers
  - 32-bit Cyclic Redundancy Check (CRC) computed on buffer transfers

Advanced Analog Features

- 12-bit Analog-to-Digital Converter (ADC) module:
  - Two Successive Approximation Register (SAR) ADC analog cores (one dedicated and one shared)
  - Up to 2 Msps conversion data rate for each SAR ADC
  - Up to 16 analog inputs
- Flexible and independent ADC trigger sources

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Communication Interfaces

- Two UART Modules:
  - Supports RS-232, RS-485 and LIN 1.2 protocols
  - Supports IrDA® with on-chip hardware encoder and decoder
  - Supports up to 10 Mbps data rate over UART1
- One optional CAN port with dedicated DMA channels:
  - Supports CAN 2.0A and 2.0B
  - 16 buffers, 16 filters, and 3 masks
- One SQI interface
- Two Serial Peripheral Interface (SPI) ports with:
  - 3-wire SPI (supports four SPI modes)
  - 4-wire Framed SPI
  - 4 x 32-bit, 8 x16-bit or 8 x 8-bit FIFOs
- One SPI interface for the boot Flash code memory (for stacked-die Flash memory)
- Two I^2C master and slave with address masking
- One Full-Speed or Low-Speed USB 2.0 On-The-Go (OTG) port
- Peripheral Pin Select (PPS) to enable function remap
- High count of general purpose peripherals up to 52 GPIOs

Timers/Output Compare/Input Capture

- Up to 7 timers:
  - 16-bit timers/counters which can be paired to 32-bit timers/counters
- Up to four Input Capture (IC) modules
- Up to four Output Compare (OC) modules
- Cycle Time Register (CTR) timestamps the discrete events within the system

Debugger Development Support

- Two programming and debugging interfaces:
  - 2-wire interface with non-intrusive access and real time data exchange with application
  - 4-wire MIPS® Enhanced JTAG (EJTAG) interface
- IEEE 1149.2-compatible (JTAG) boundary scan

Software and Tools Support

- MPLAB® Harmony Integrated Software Framework
- Middlewares: TCP/IP, USB
- FreeRTOS™, OpenRTOS®, Micriμm® μC/OS™ and other popular RTOS kernels

Note: The software is based on the MPLAB Harmony Integrated Software Framework and it works with the MPLAB Harmony TCP/IP release. It uses an operating system abstraction layer (OSAL) for OS support, hence it functions with all MPLAB Harmony supported OS. The software demonstration is available to indicate how it works with FreeRTOS and without OS.

Package

Type	Double Row QFN (DQFN)
Pin Count	132
I/O Pins (up to)	52
Contact/Lead Pitch	0.5 mm
Dimensions	10 mm x 10 mm x 0.9 mm

Applications

- Internet of Things (IoT)
- Smart appliances
- Utility and smart energy
- Medical and health care
- Home and building automation
  - Fire and security
  - Comfort and control
- Bridge applications
  - USB to Wi-Fi bridge
  - CAN to Wi-Fi bridge

Description

The PIC32WK2057GPX SoC is integrated with IEEE 802.11a/b/g/n standard media access control (MAC), BBP and RF transceiver. The PIC32WK2057GPX features a MIPS32® M14K 32-bit core with 5-stage execution pipeline and MicroMIPS™ mode for reduced code size. The PIC32WK2057GPX contains WDT, POR, BOR, PLL, oscillators and JTAG. Table 1 provides the ordering information of the PIC32WK2057GPX SoC

TABLE 1: ORDERING INFORMATION

Part Number	Description
PIC32WK2057GPB132-I/NX	32-bit MCU, 2 Mbyte Flash, 576 Kbytes program+data RAM, 2.4/5 GHz Wi-Fi, 132-pin, USB
PIC32WK2057GPD132-I/NX	32-bit MCU, 2 Mbyte Flash, 576 Kbytes program+data RAM, 2.4/5 GHz Wi-Fi, 132-pin, USB, CAN

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Figure 1 illustrates a typical block diagram of the PIC32WK2057GPX SoC.

FIGURE 1: PIC32WK2057GPX SoC BLOCK DIAGRAM

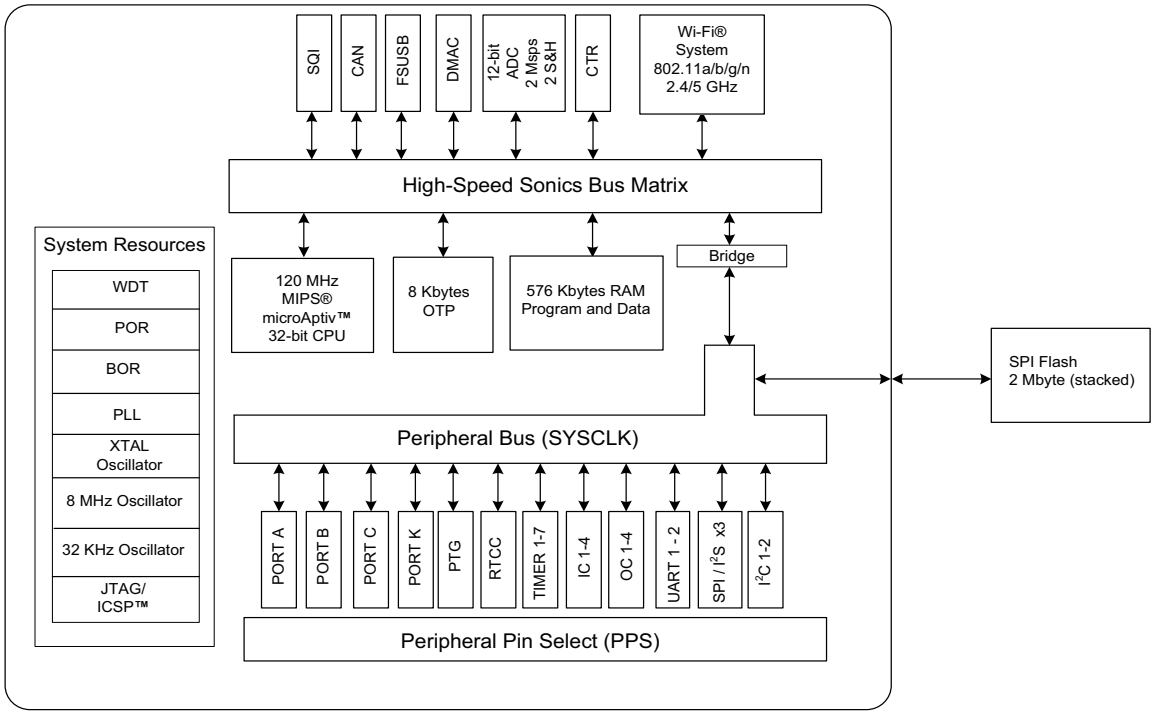

Figure 2 and Figure 3 illustrate pin diagram and package dimensions of the PIC32WK2057GPX SoC.

FIGURE 2: PIC32WK2057GPX PIN DIAGRAM

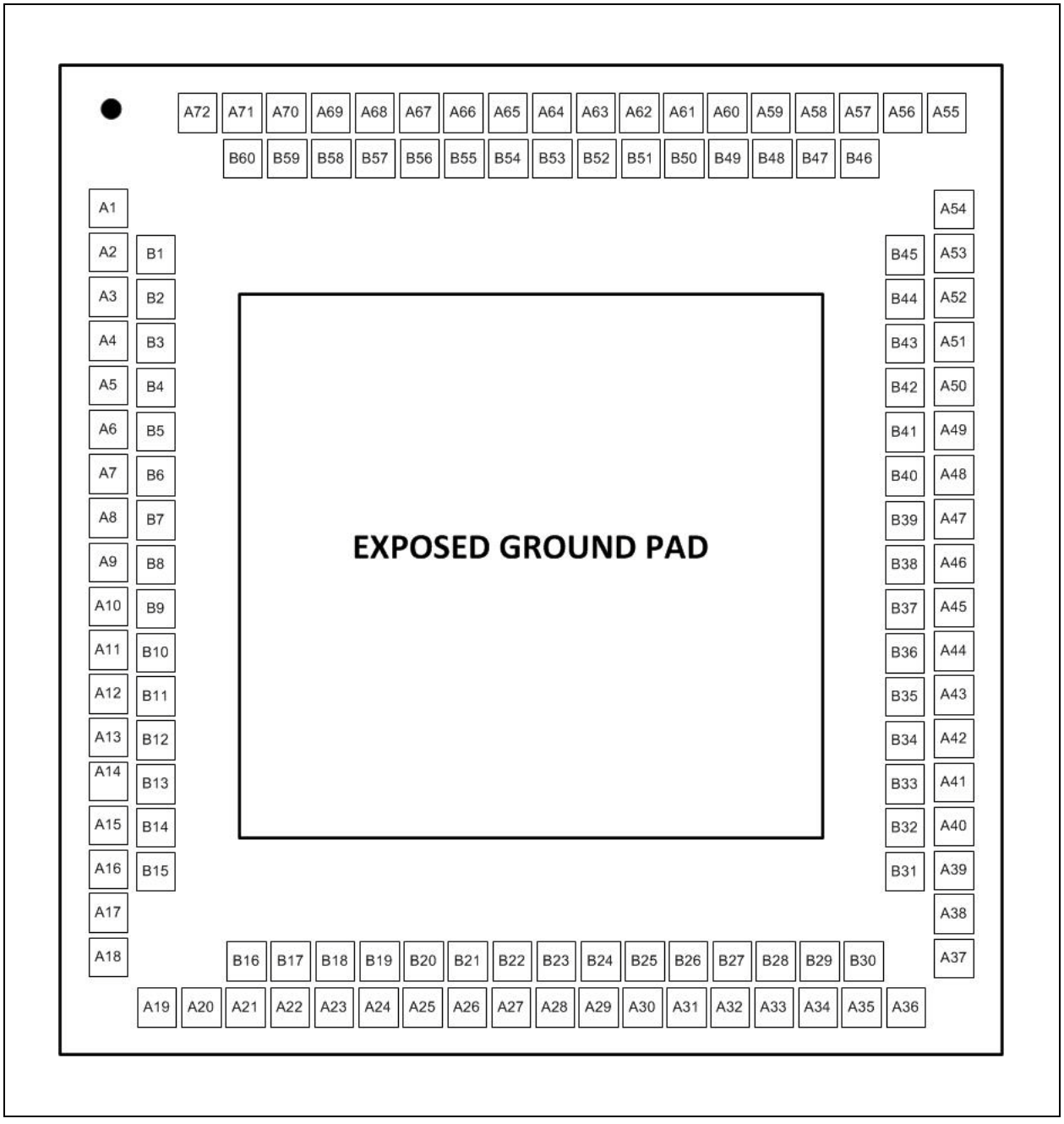

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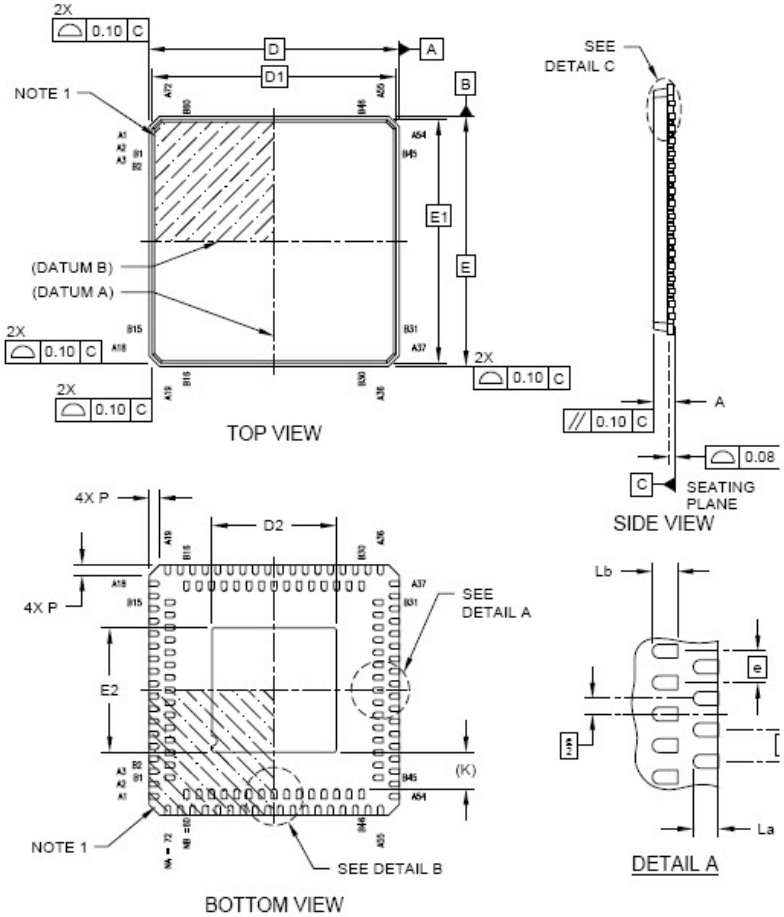
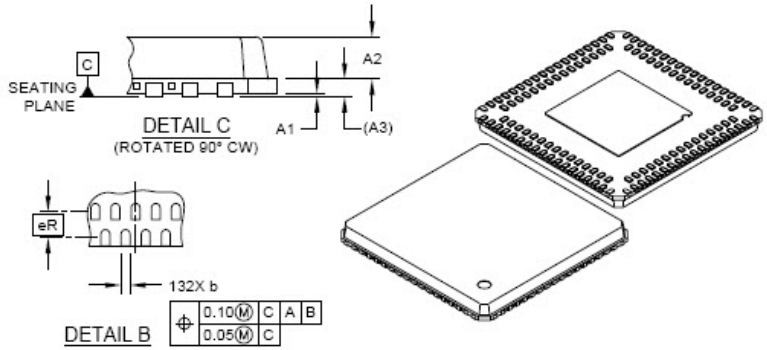
FIGURE 3: PIC32WK2057GPX PACKAGE DIMENSION

132-Lead Very Thin Plastic Quad Flat, No Lead Package (NX) - 10x10x0.9 mm Body Dual Row Terminals, Punch Singulated

Note: For the most current package drawings, please see the Microchip Packaging Specification located at: http://www.microchip.com/packaging





	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Number of Terminals	N		132	
Terminals in Outer Row A	NA		72	
Terminals in Inner Row B	NB		60	
Pitch	e		0.50 BSC	
Pitch Between Rows	eR		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.01	0.05
Mold Cap Height	A2	0.55	0.60	0.65
Base Thickness	A3		0.25 REF	
Overall Length	D		10.00 BSC	
Mold Cap Length	D1		9.73 BSC	
Exposed Pad Length	D2	4.87	4.97	5.07
Overall Width	E		10.00 BSC	
Mold Cap Width	E1		9.73 BSC	
Exposed Pad Width	E2	4.87	4.97	5.07
Terminal Length, Outer Row	La	0.30	0.40	0.50
Terminal Length, Inner Row	Lb	0.30	0.40	0.50
Terminal Width	b	0.18	0.22	0.30
Terminal-to-Exposed-Pad	K		0.20 MIN REF	
Corner Chamfer	P	0.24	0.42	0.60

Note 1: Pin 1 visual index feature may vary, and it must be located within the hatched area.

2: The package is punch singulated.

3: Dimensions and tolerances are per ASME Y14.5M: BSC: Basic Dimension. Theoretically the exact value is shown without tolerances. Dimensions (usually without tolerance) are for reference purposes only.

NOTES:

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